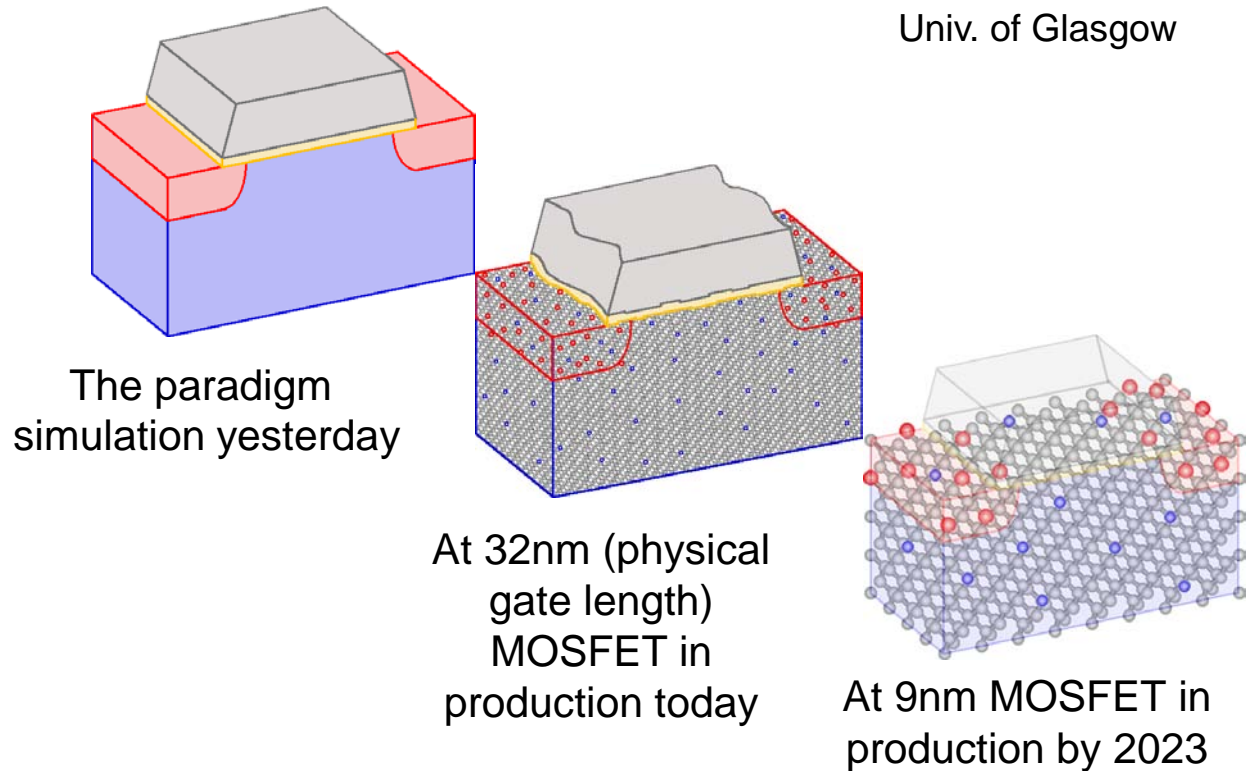


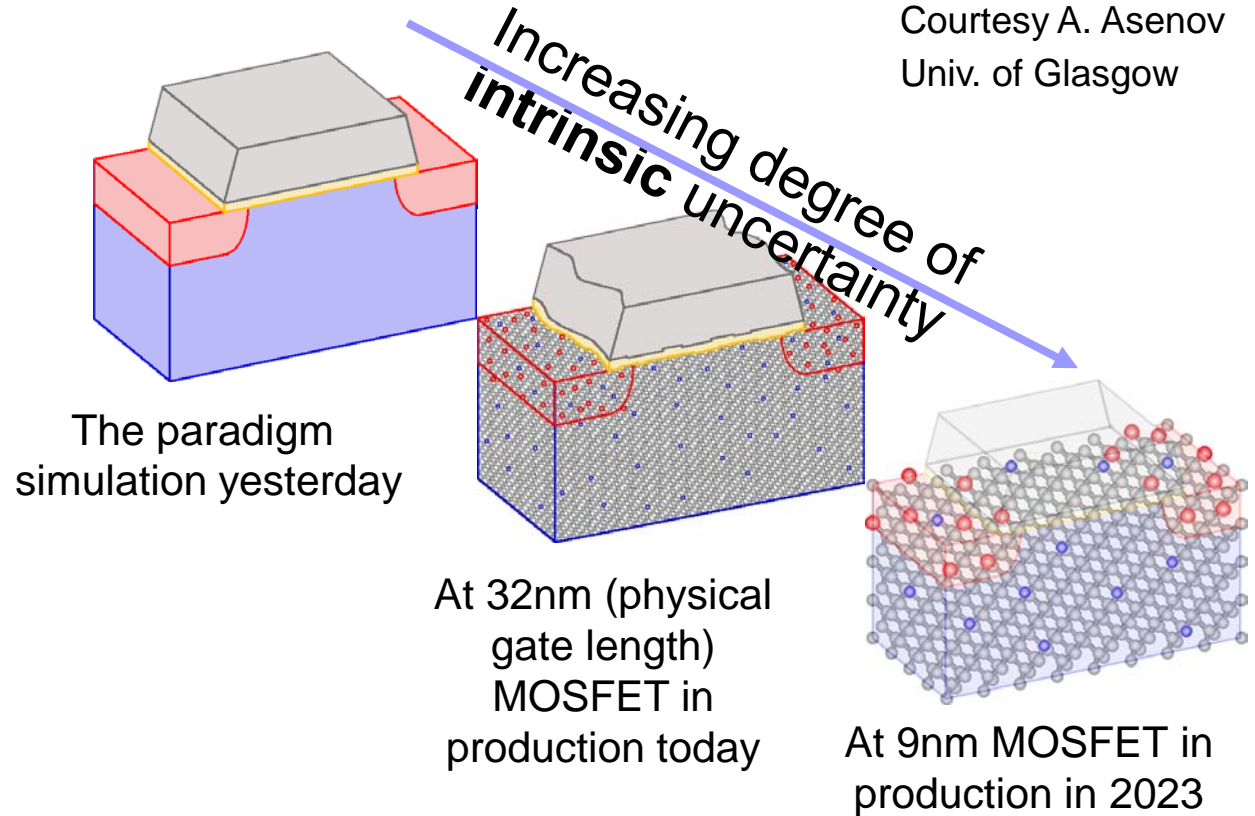
The next generation MOSFETs are atomic scale devices

Courtesy A. Asenov
Univ. of Glasgow



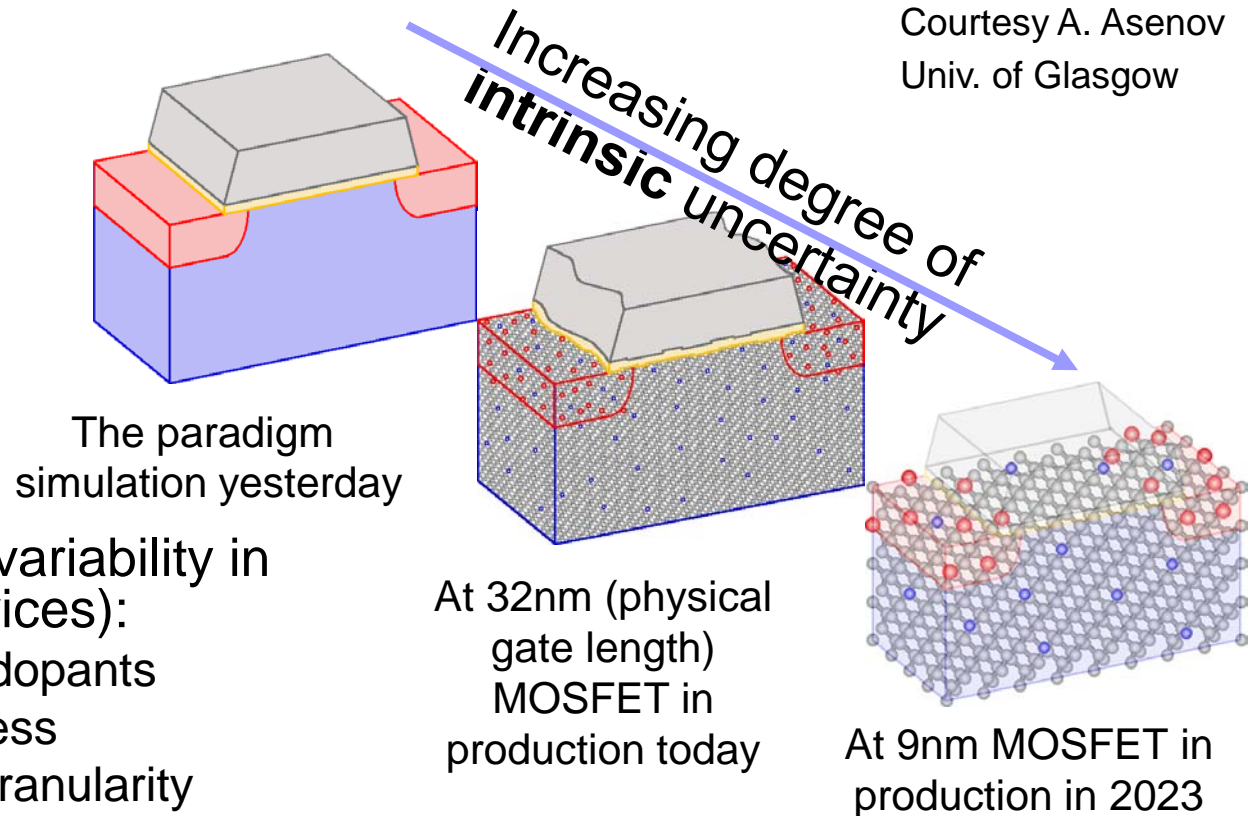
The next generation MOSFETs are atomic scale devices

Courtesy A. Asenov
Univ. of Glasgow



The next generation MOSFETs are atomic scale devices

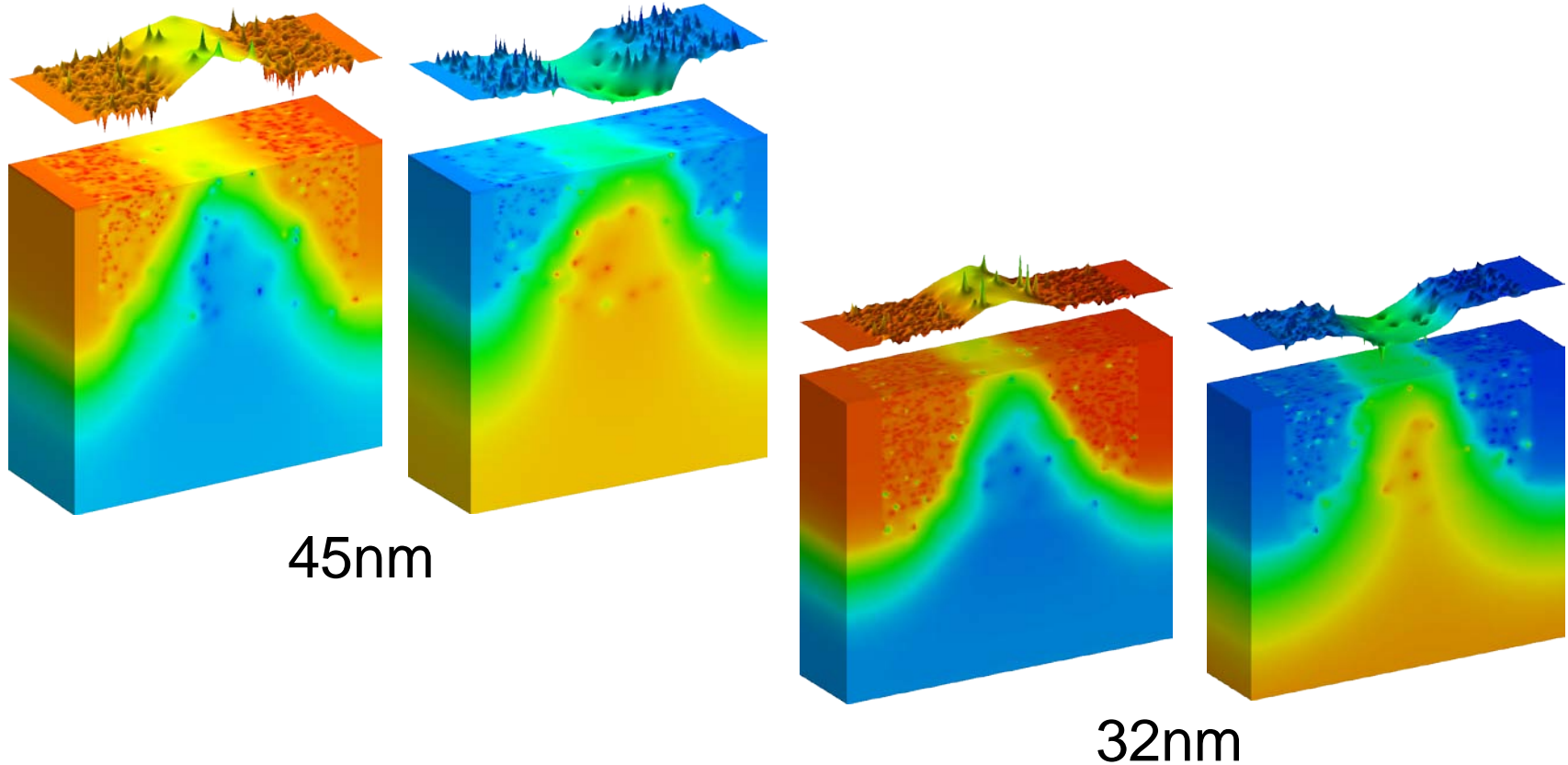
Courtesy A. Asenov
Univ. of Glasgow



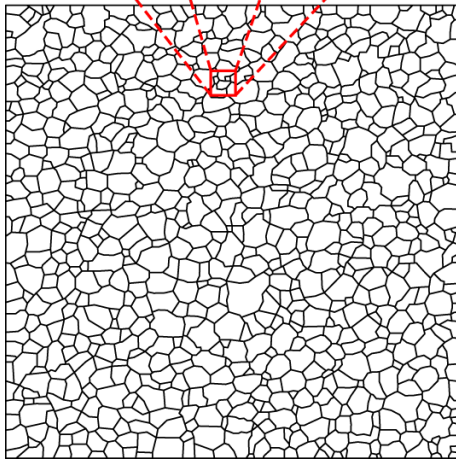
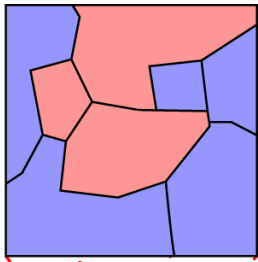
■ Sources of intrinsic variability in identical printed devices):

- Random discrete dopants
- Line edge roughness
- Poly silicon gate granularity
- Metal gate grain granularity
-

Process variability increases with technology node: smaller channel length yes but has also more uncertainty



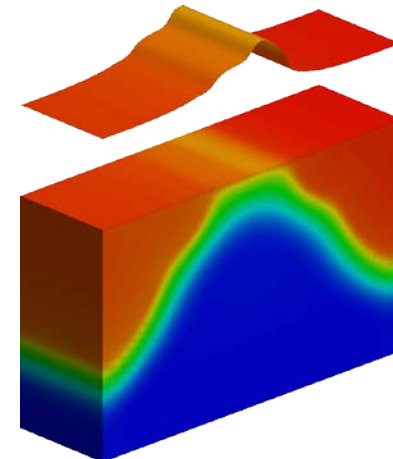
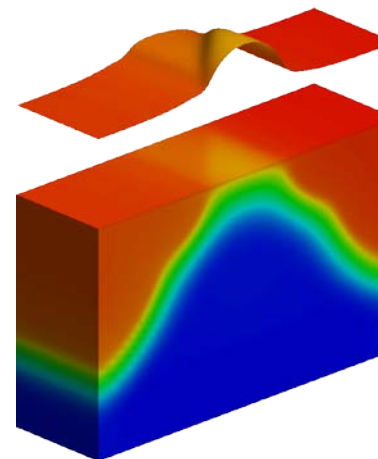
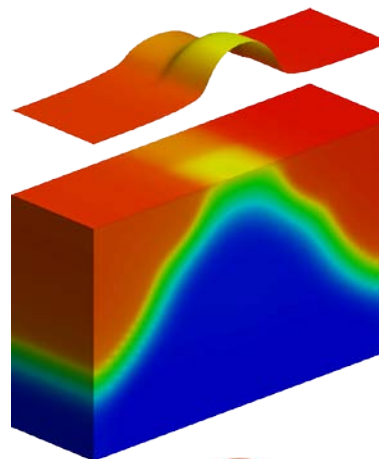
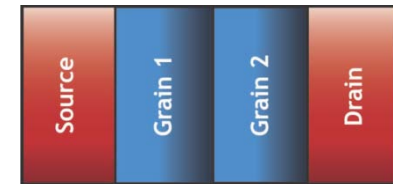
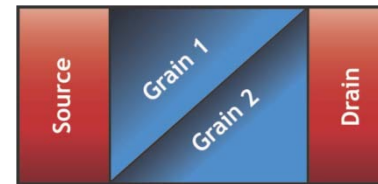
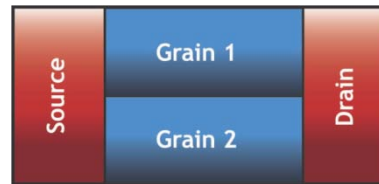
New materials = new sources of intrinsic variability: metal gate granularity



2 likely grain orientations with 2 likely metal working functions:

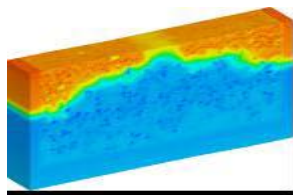
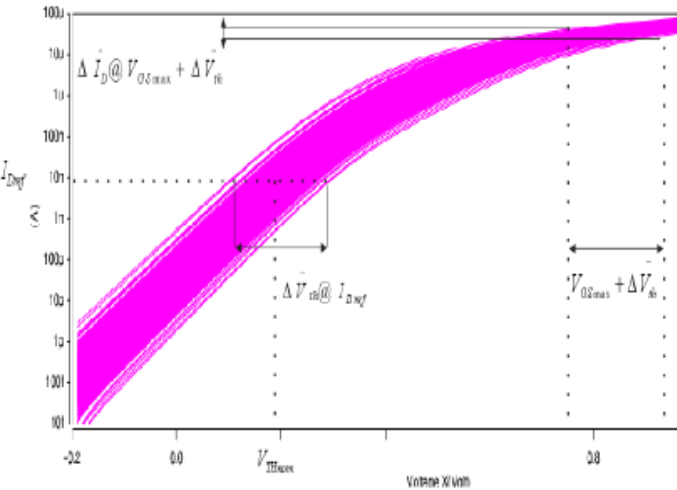
$\langle 111 \rangle$: 4.4 eV (40%)

$\langle 200 \rangle$: 4.6 eV (60%)



Idris, et. al. "Simulation Study of Workfunction Variability in MOSFETs with Polycrystalline Metal Gates", ULIS 2010,

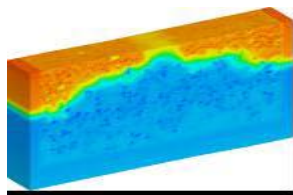
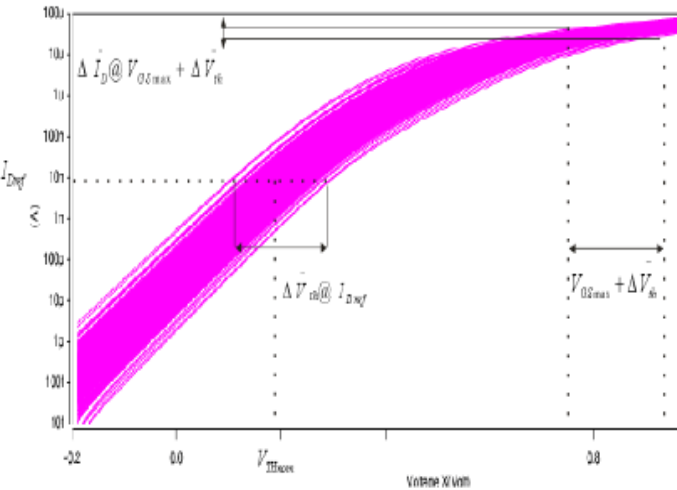
Need to understand impact of device variations into system design...



Courtesy
A.Asenov U. of
Glasgow

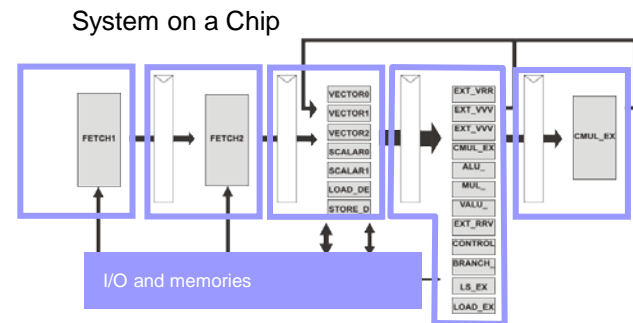
1 device

Need to understand impact of device variations into system design...



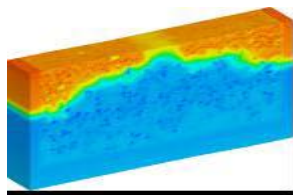
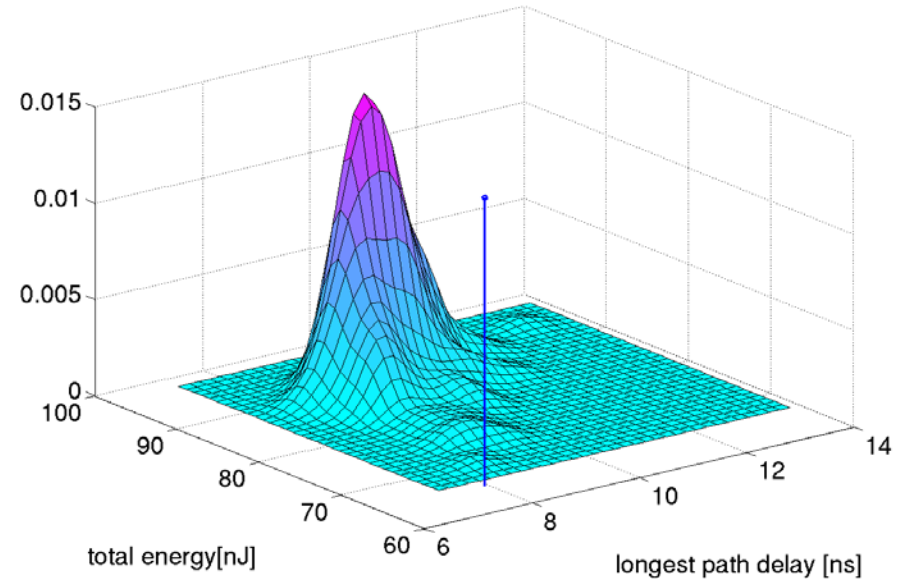
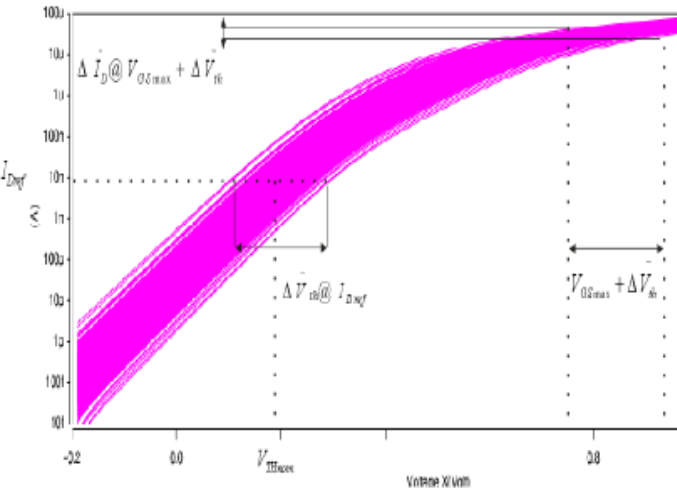
Courtesy
A.Asenov U. of
Glasgow

1 device



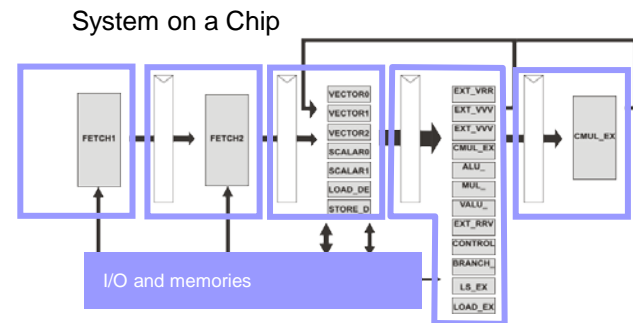
Millions of devices

Need to understand impact of device variations into system design...



Courtesy
A.Asenov U. of
Glasgow

1 device



Millions of devices

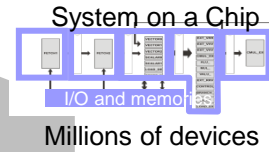
Overview

- General project objectives and innovation
- Work plan and status
- Conclusions

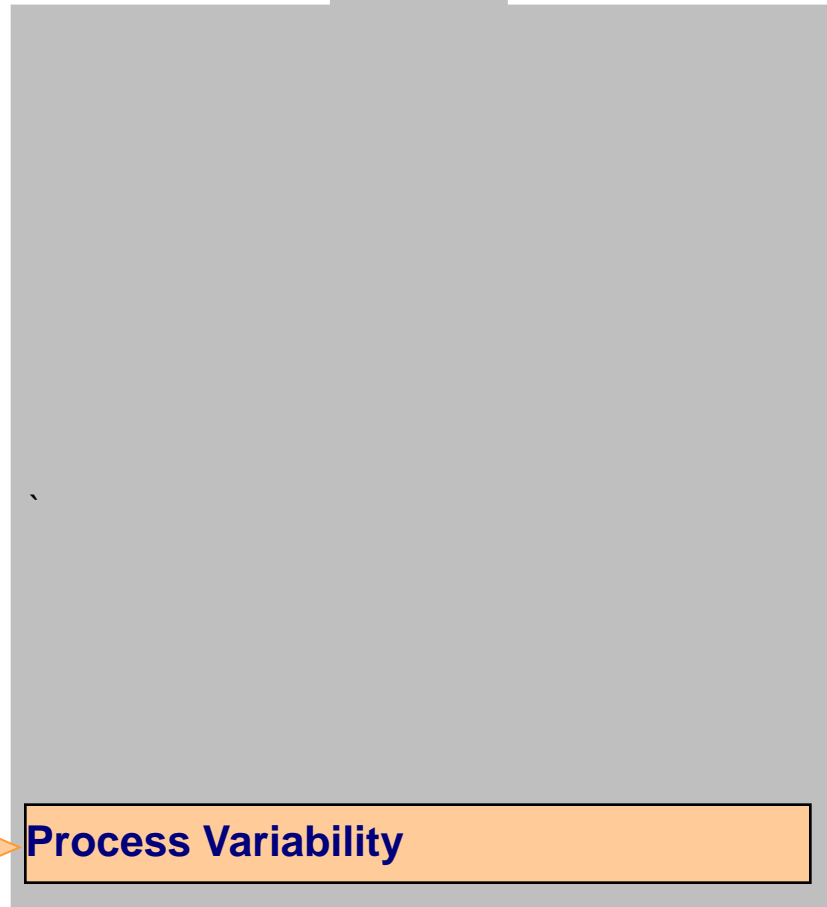
Overview

- General project objectives and innovation
 - General objectives
 - Project approach and structure
- Work plan and status
- Conclusions

...1) by building a variation aware percolation flow compatible with existing design flows...

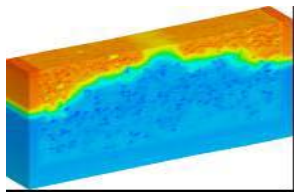


Millions of devices

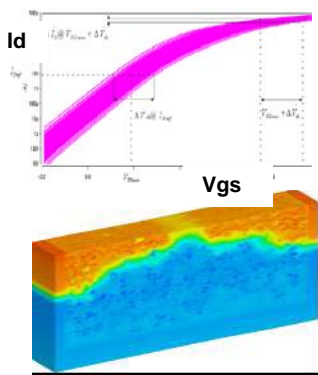
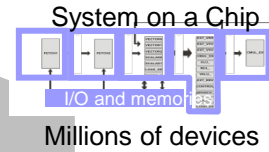


Variability =
Physical & chemical

Process Variability



...1) by building a variation aware percolation flow compatible with existing design flows...



Variability = electrical (V, I, R, C)

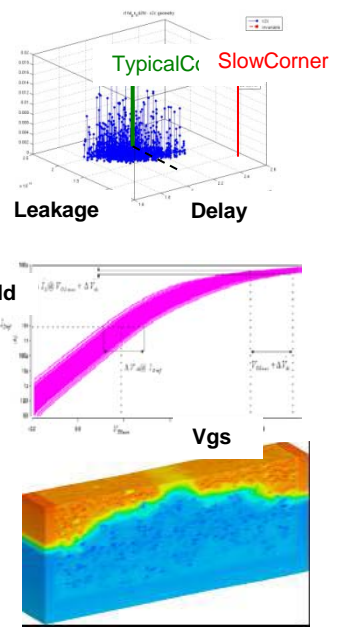
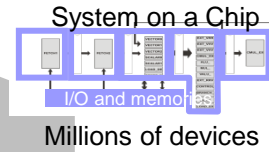
Variability = Physical & chemical

Statistical Device Compact Model

TCAD, foundry models, silicon

Process Variability

...1) by building a variation aware percolation flow compatible with existing design flows...



Variability = (.lib)
Leak, delay, power...

Variability =
electrical (V, I, R, C)

Variability =
Physical & chemical

“Liberty” format files (statistical .lib)

Standard cells

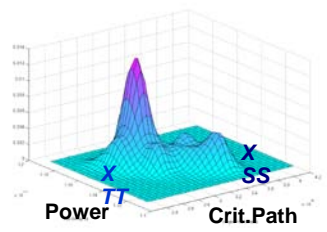
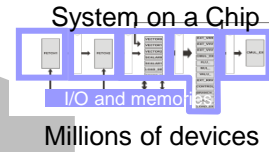
SRAMs, Reg. Files

Statistical Device Compact Model

TCAD, foundry models, silicon

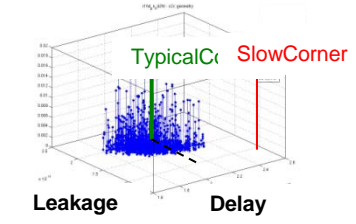
Process Variability

...1) by building a variation aware percolation flow compatible with existing design flows...



Variability =
Critical Path & Power

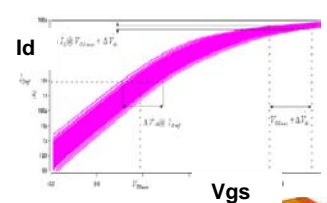
Statistical Timing & Power Reports



Variability = (.lib)
Leak, delay, power...

IP blocks (processors, controllers)

"Liberty" format files (statistical .lib)

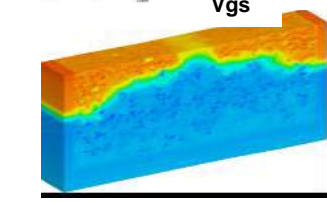


Variability =
electrical (V, I, R, C)

Standard cells

SRAMs, Reg. Files

Statistical Device Compact Model

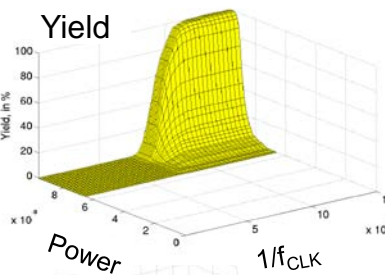
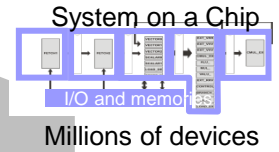


Variability =
Physical & chemical

TCAD, foundry models, silicon

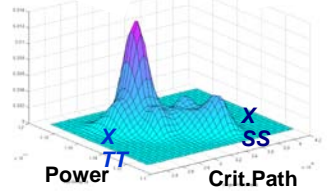
Process Variability

...1) by building a variation aware percolation flow e with existing design flows...



Variability =
Yield := Prob (timing, power are met)

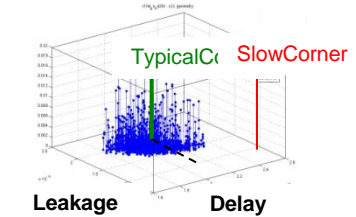
Yield vs power vs clock freq.



Variability =
Critical Path & Power

System On Chip

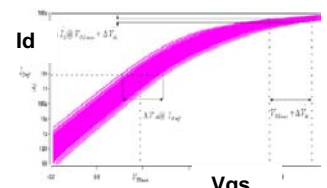
Statistical Timing & Power Reports



Variability = (.lib)
Leak, delay, power...

IP blocks (processors, controllers)

"Liberty" format files (statistical .lib)

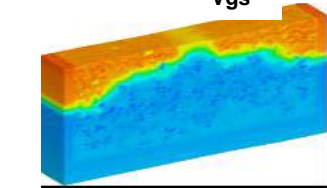


Variability =
electrical (V, I, R, C)

Standard cells

SRAMs, Reg. Files

Statistical Device Compact Model

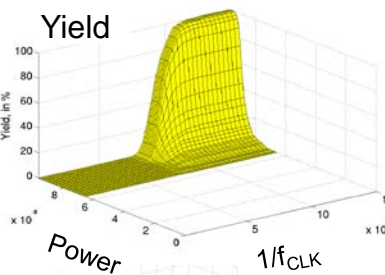
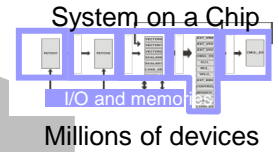


Variability =
Physical & chemical

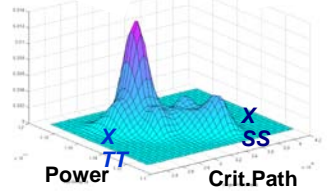
TCAD, foundry models, silicon

Process Variability

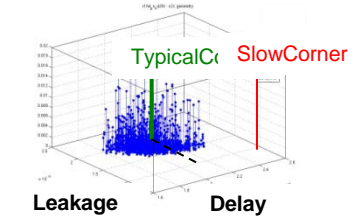
...1) by building a variation aware percolation flow e with existing design flows...



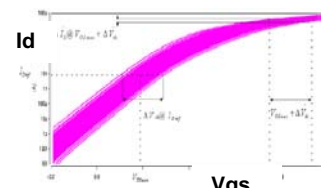
Variability =
Yield := Prob (timing, power are met)



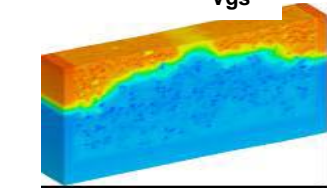
Variability =
Critical Path & Power



Variability = (.lib)
Leak, delay, power...



Variability =
electrical (V, I, R, C)

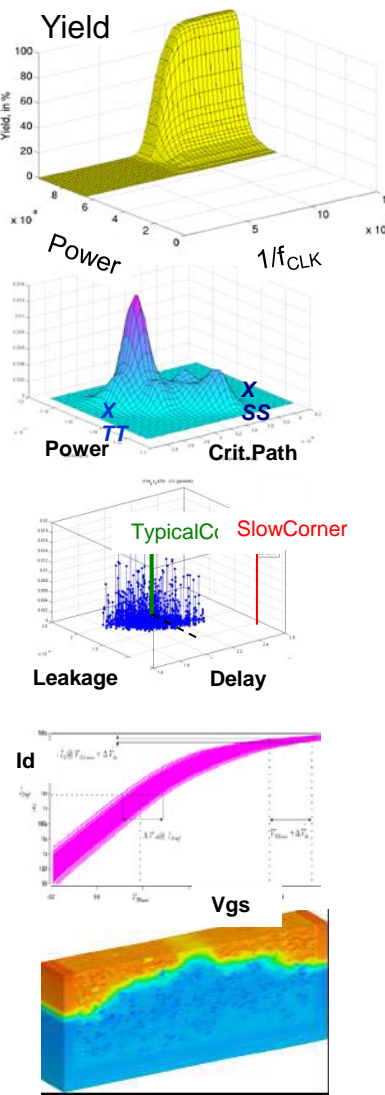
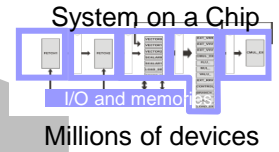


Variability =
Physical & chemical

Variability Information Format

- Yield vs power vs clock freq.**
- System On Chip**
- Statistical Timing & Power Reports**
- IP blocks (processors, controllers)**
- “Liberty” format files (statistical .lib)**
- Standard cells** **SRAMs, Reg. Files**
- Statistical Device Compact Model**
- TCAD, foundry models, silicon**
- Process Variability**

...1) by building a variation aware percolation flow e with existing design flows...



Variability =
 Yield := Prob (timing, power are met)

Variability =
 Critical Path & Power

Variability = (.lib)
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Variability =
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Variability Information Format

Yield vs. power vs. clock freq.

System Chip

Statistical Timing & Power Reports

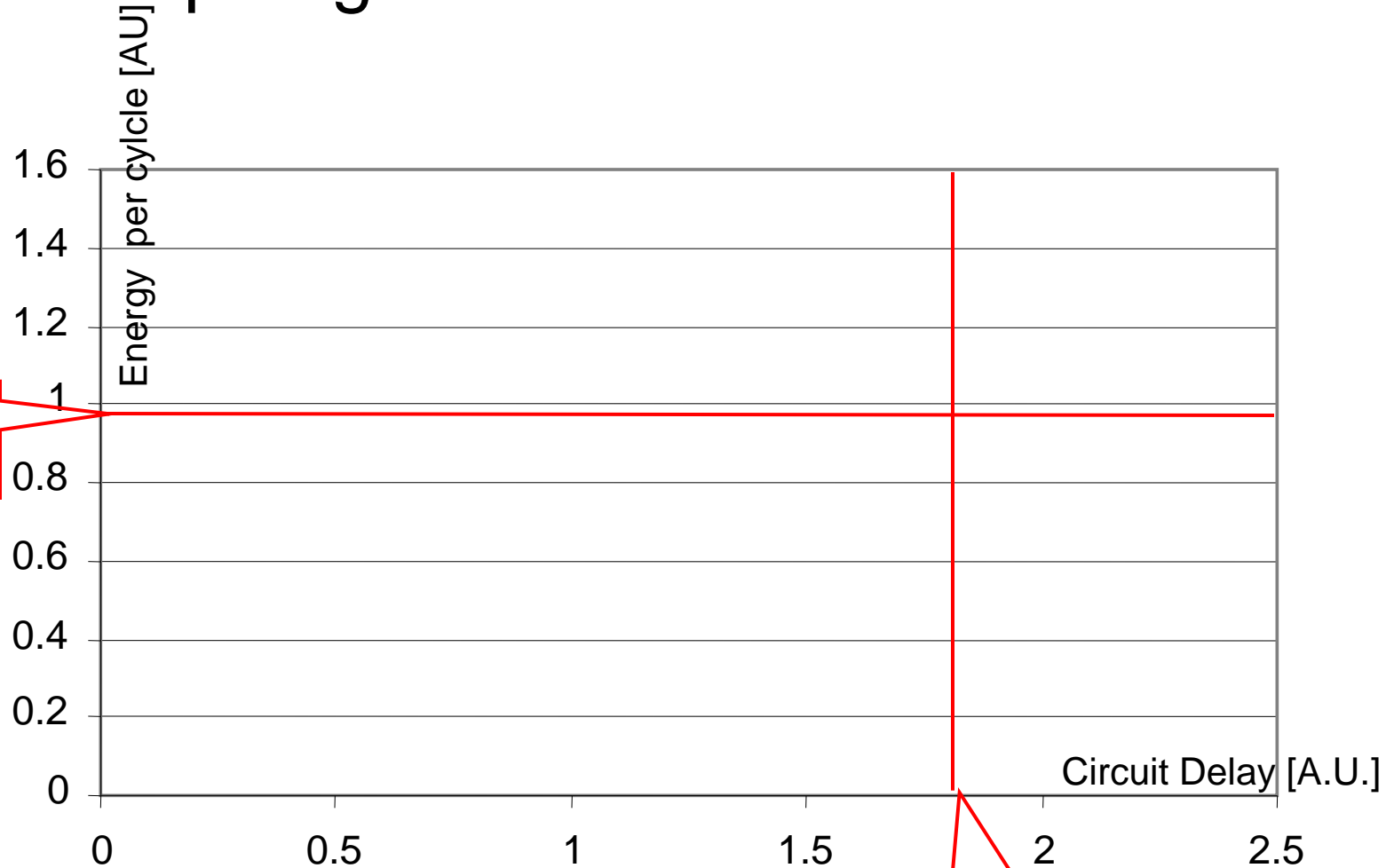
"Liberty" format files (statistical .lib)

Files

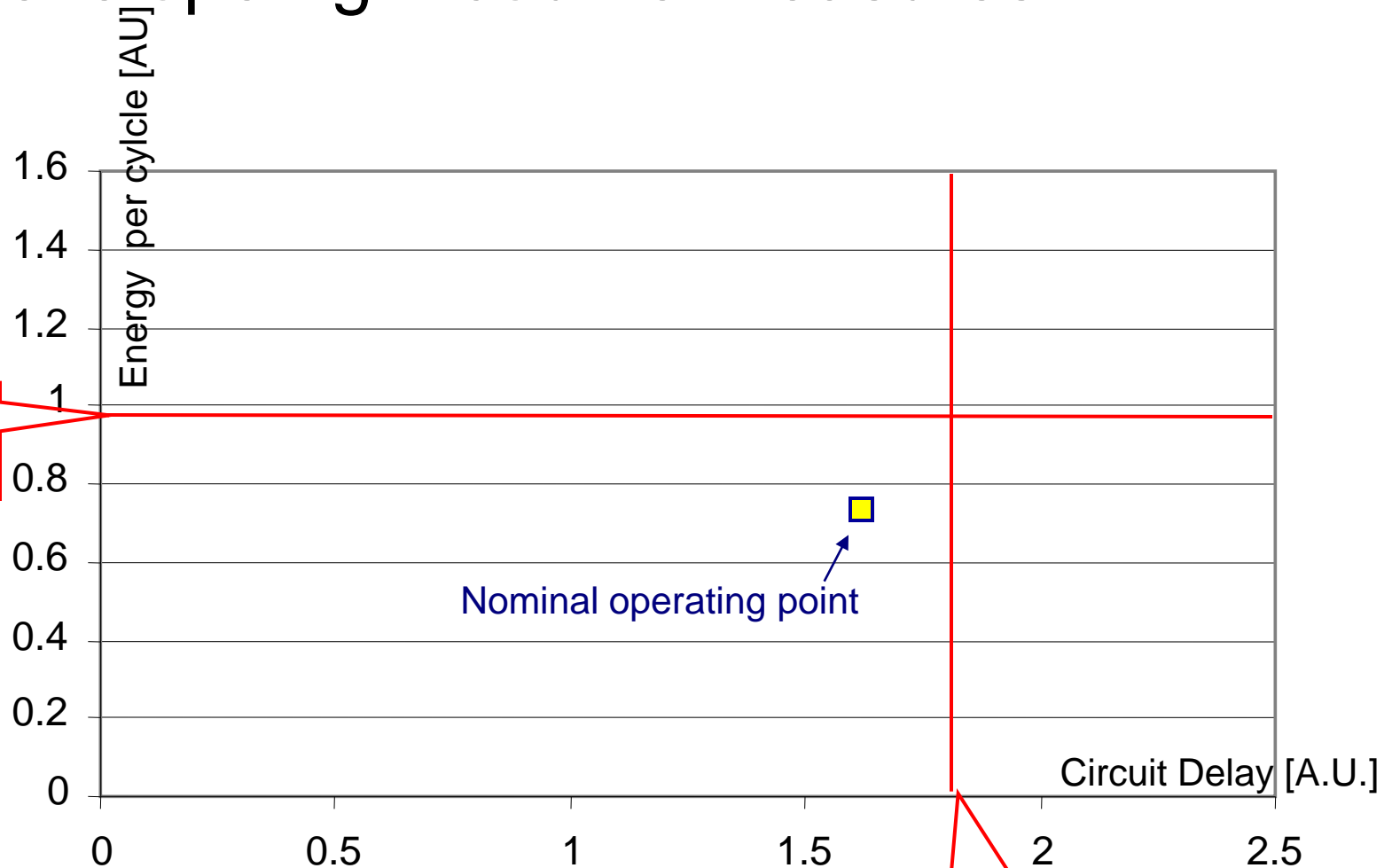
Statistical Device Compact Model

Process bility

...to assess the magnitude of the problem to
2) develop right countermeasures...



...to assess the magnitude of the problem to
2) develop right countermeasures...

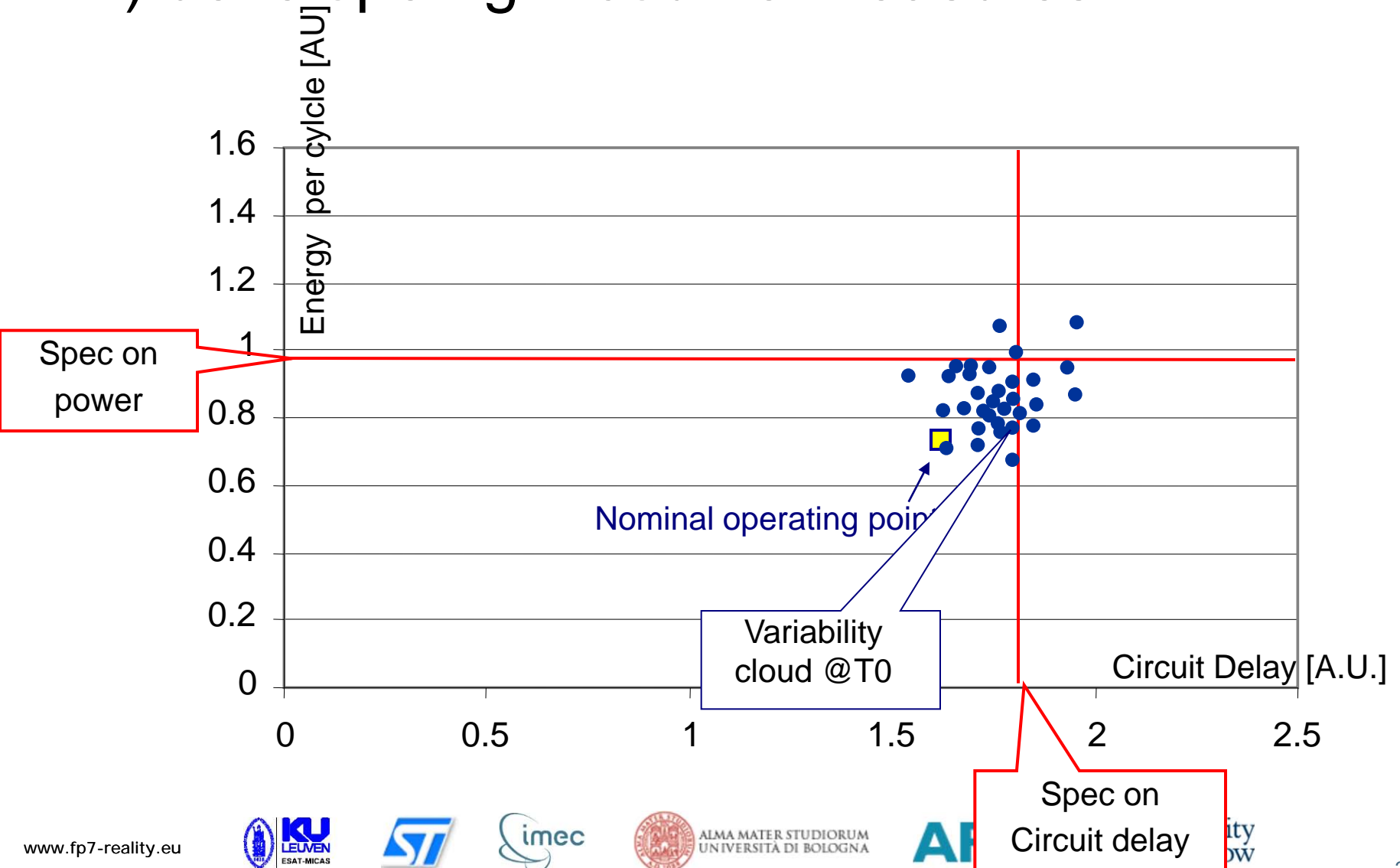


Spec on
power

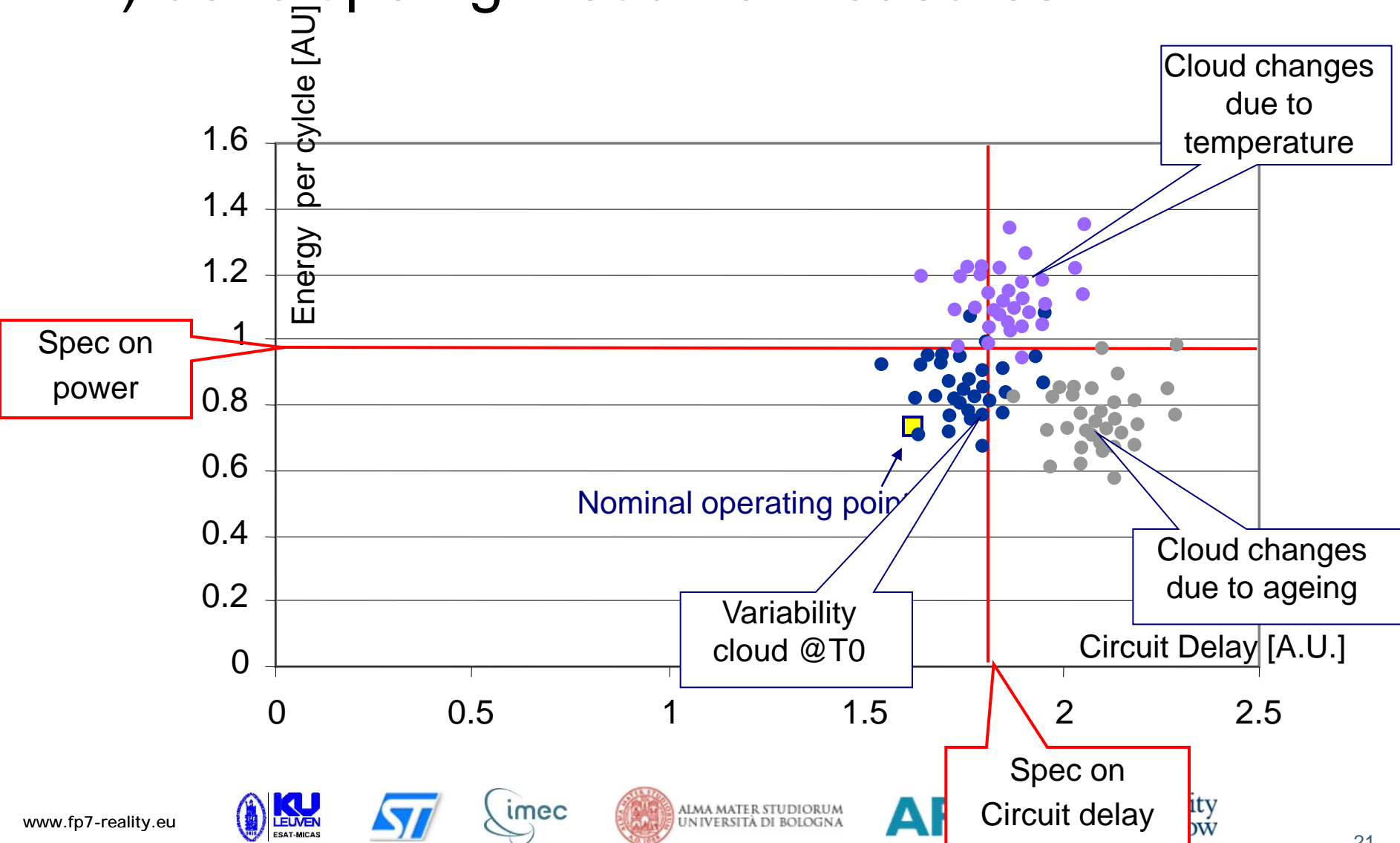
Nominal operating point

Spec on
Circuit delay

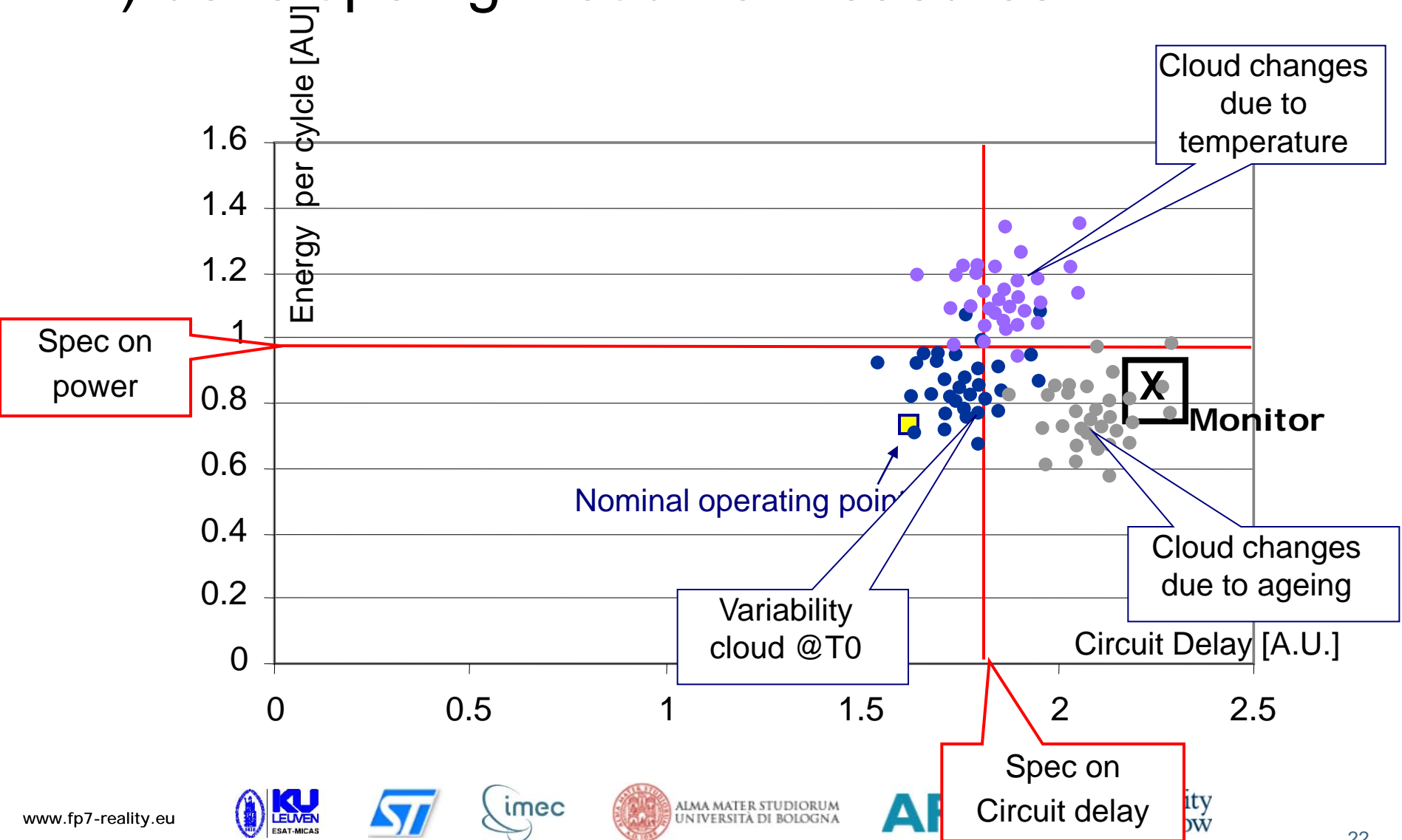
...to assess the magnitude of the problem to
 2) develop right countermeasures...



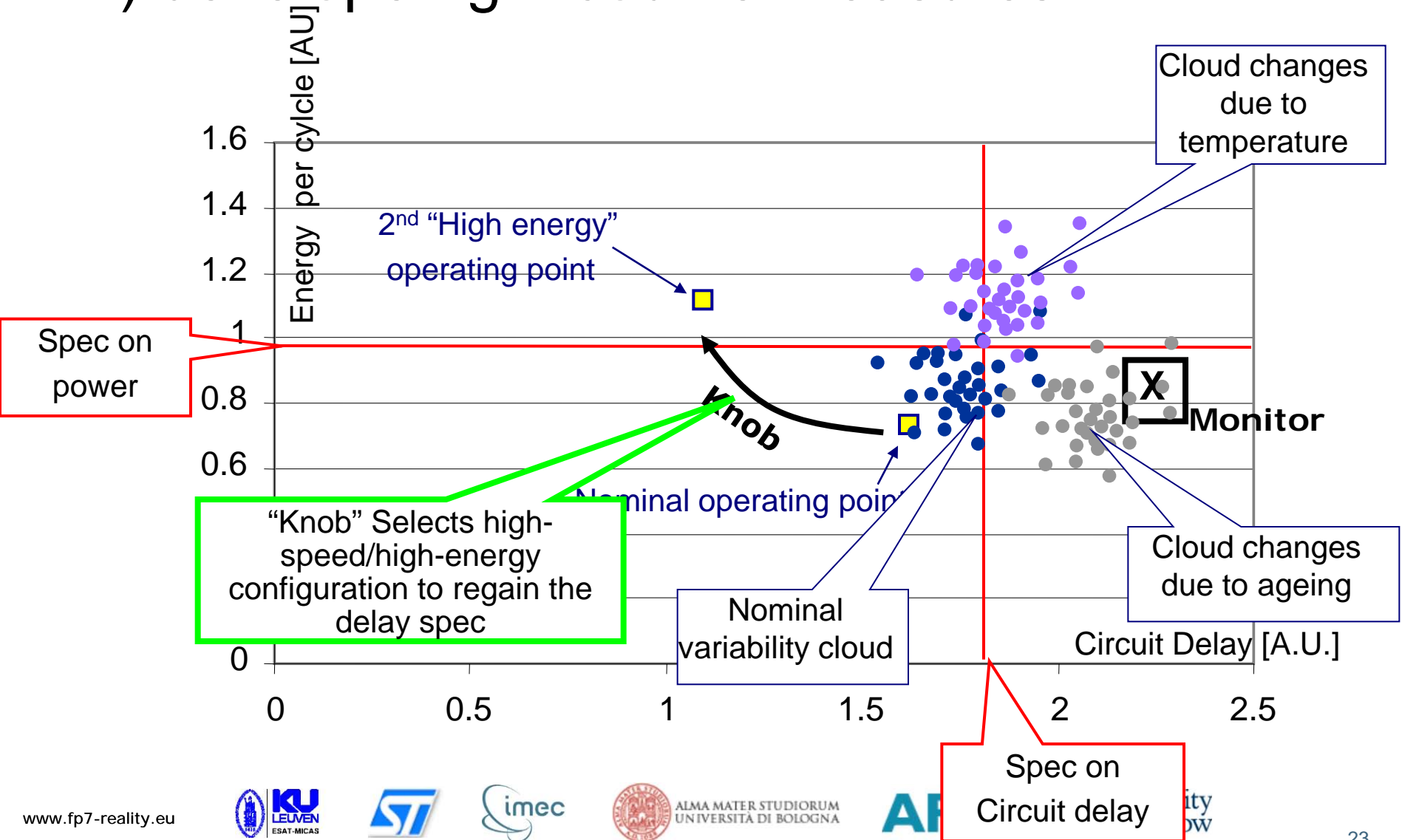
...to assess the magnitude of the problem to
2) develop right countermeasures...



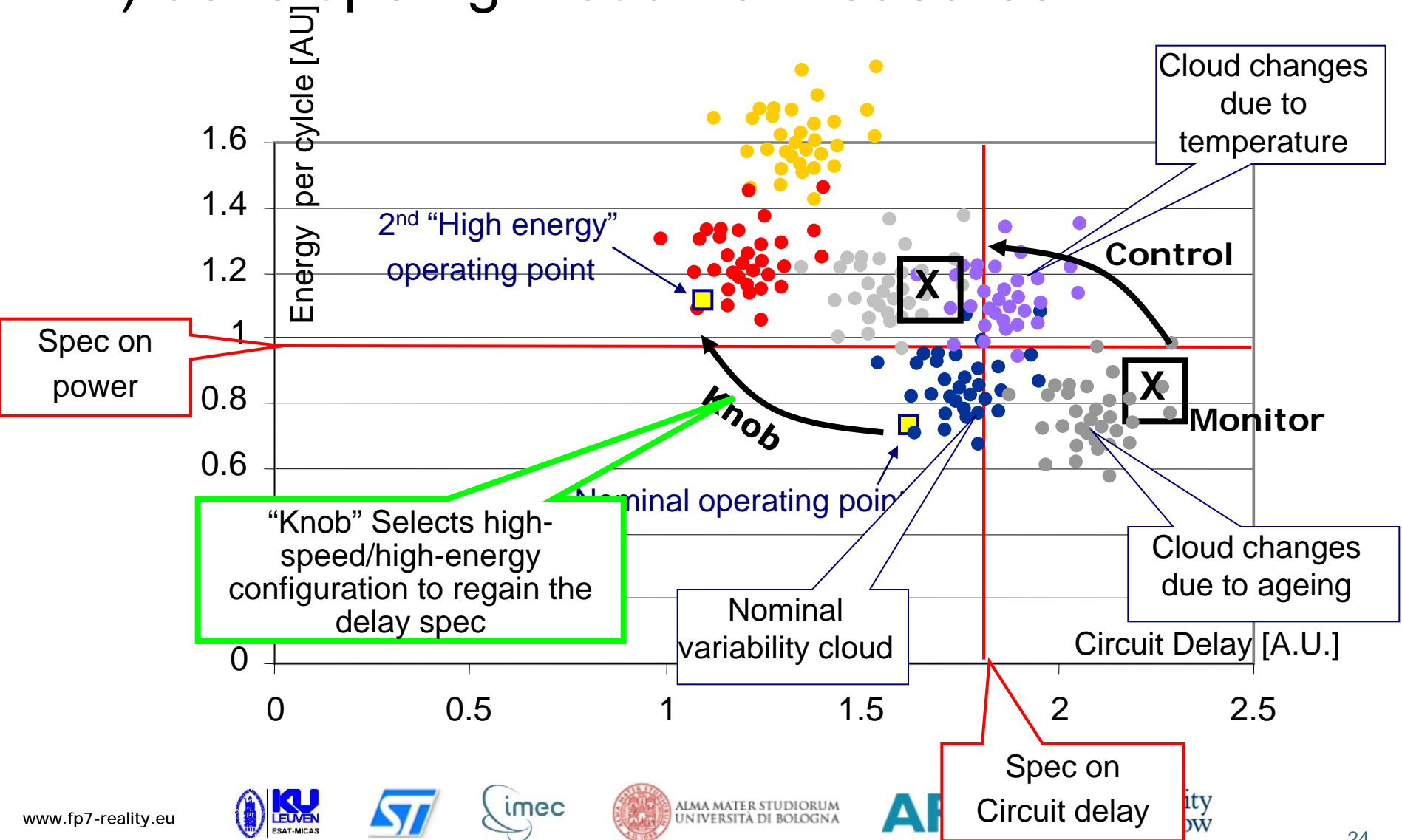
...to assess the magnitude of the problem to
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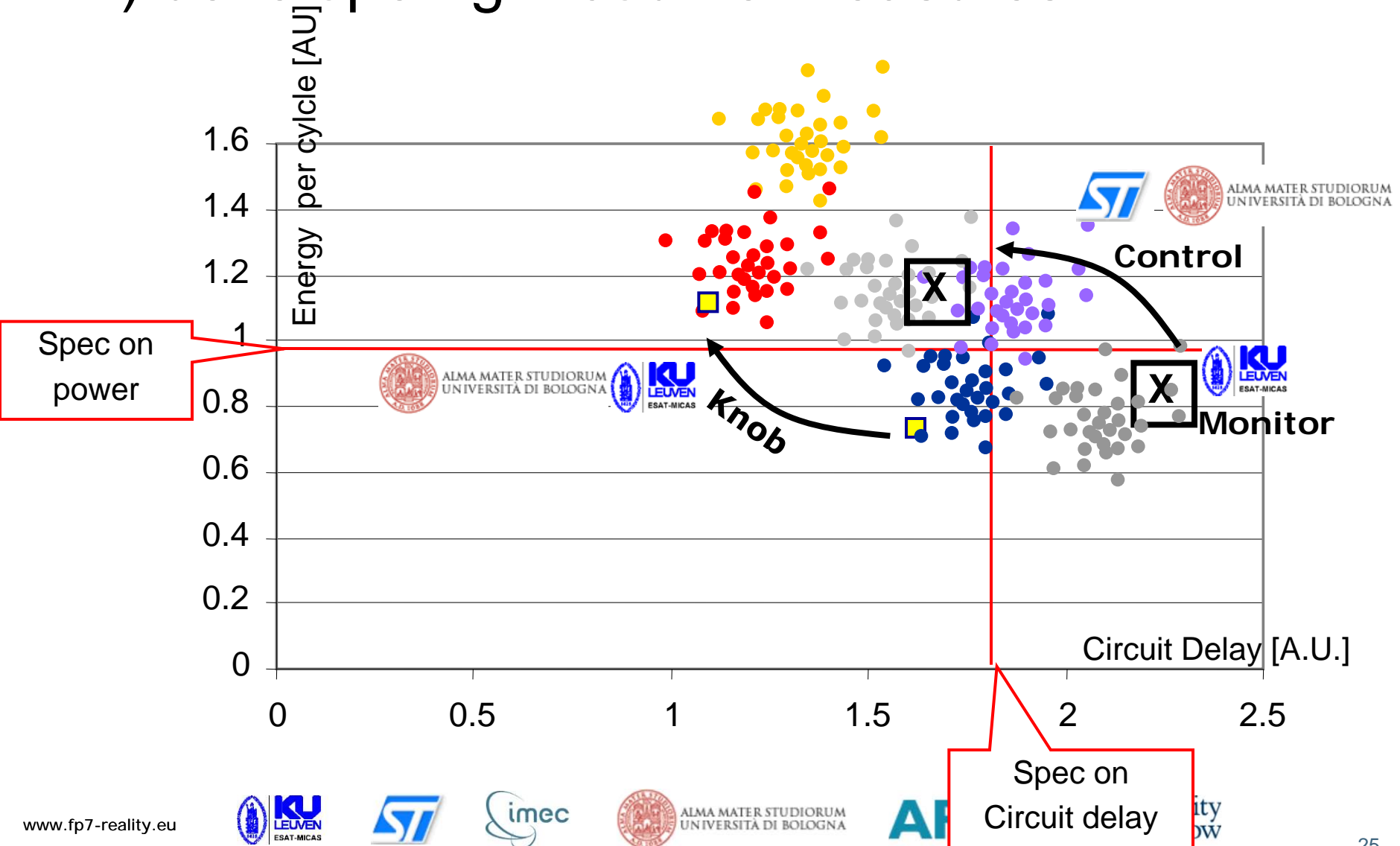
...to assess the magnitude of the problem to
 2) develop right countermeasures...



...to assess the magnitude of the problem to
 2) develop right countermeasures...



...to assess the magnitude of the problem to
 2) develop right countermeasures...



Overall project approach

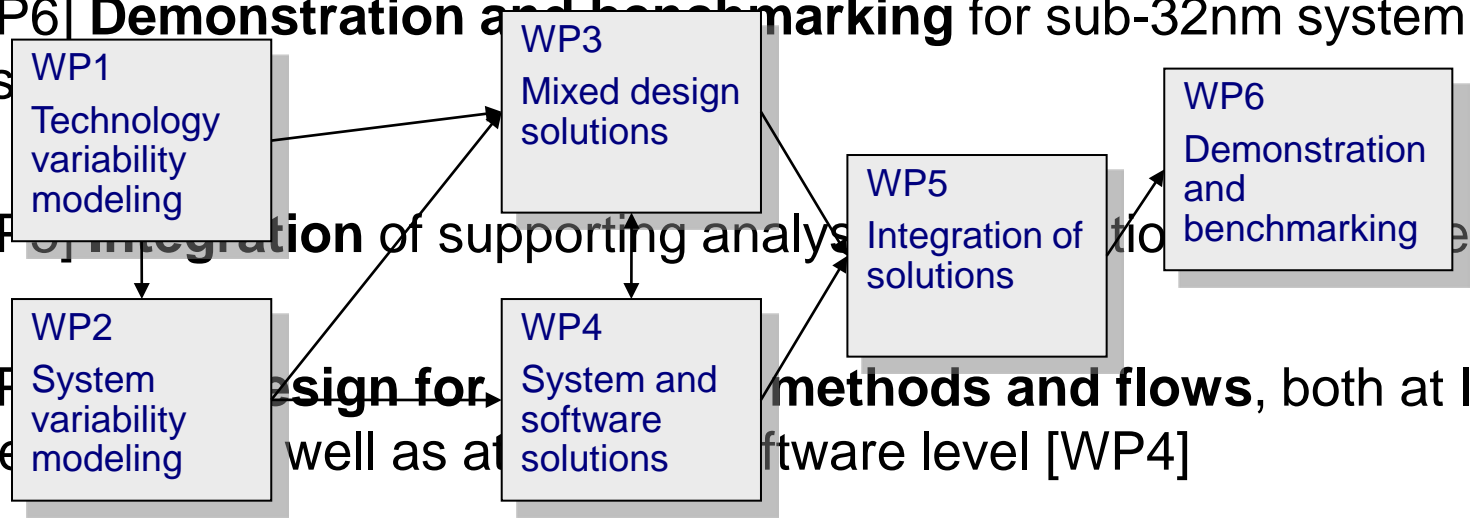
Six technical work packages conceived for a final goal:
“quantify variability to build reliable systems using unreliable technologies”:

- [WP6] **Demonstration and benchmarking** for sub-32nm system design
- [WP5] **Integration** of supporting analysis and solutions techniques.
- [WP3-WP4] **Design for Variability methods and flows**, both at IC level [WP3] as well as at system software level [WP4]
- [WP1-WP2] Vertical path for **Variability Aware Modeling** from technology [WP1] up to SoC level [WP2].

Overall project approach

Six technical work packages conceived for a final goal:
“quantify variability to build reliable systems using unreliable technologies”:

- [WP6] **Demonstration and benchmarking** for sub-32nm system



- [WP5] **Integration of supporting analysis** for design for methods and flows, both at IC level [WP4]

- [WP4] **System and software solutions** for design for methods and flows, both at IC level [WP4]

- [WP1-WP2] Vertical path for **Variability Aware Modeling** from technology [WP1] up to SoC level [WP2].

Overview

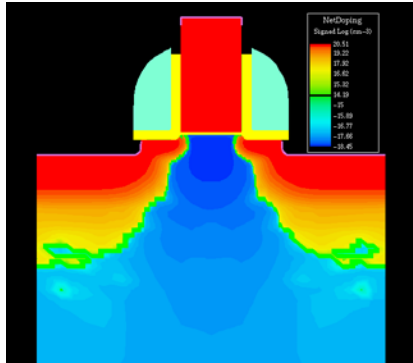
- General project objectives and innovation
- Work plan and status:
 - Technology modeling
 - Circuit to system modeling
 - IC design
 - Processor integration
 - System integration
- Conclusions

Overview

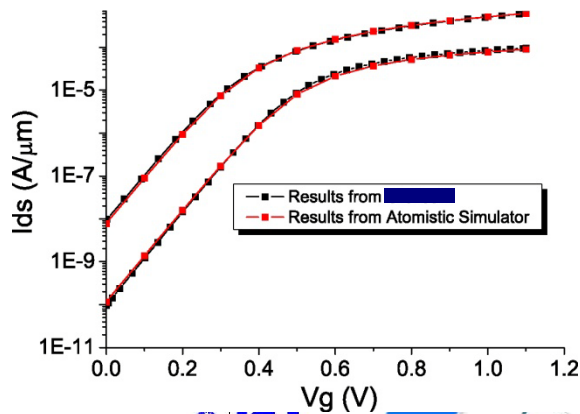
- General project objectives and innovation
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 - Technology modeling
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 - IC design
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- Conclusions

Technology Modeling

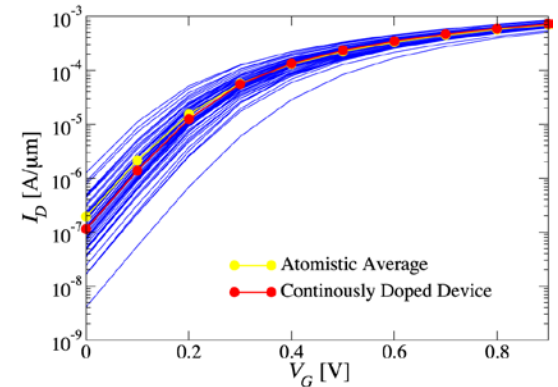
Receive device description



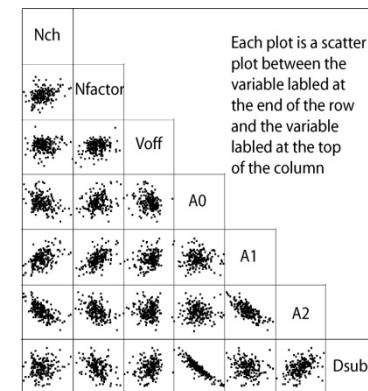
Calibrate our simulator



Introduce IPF sources

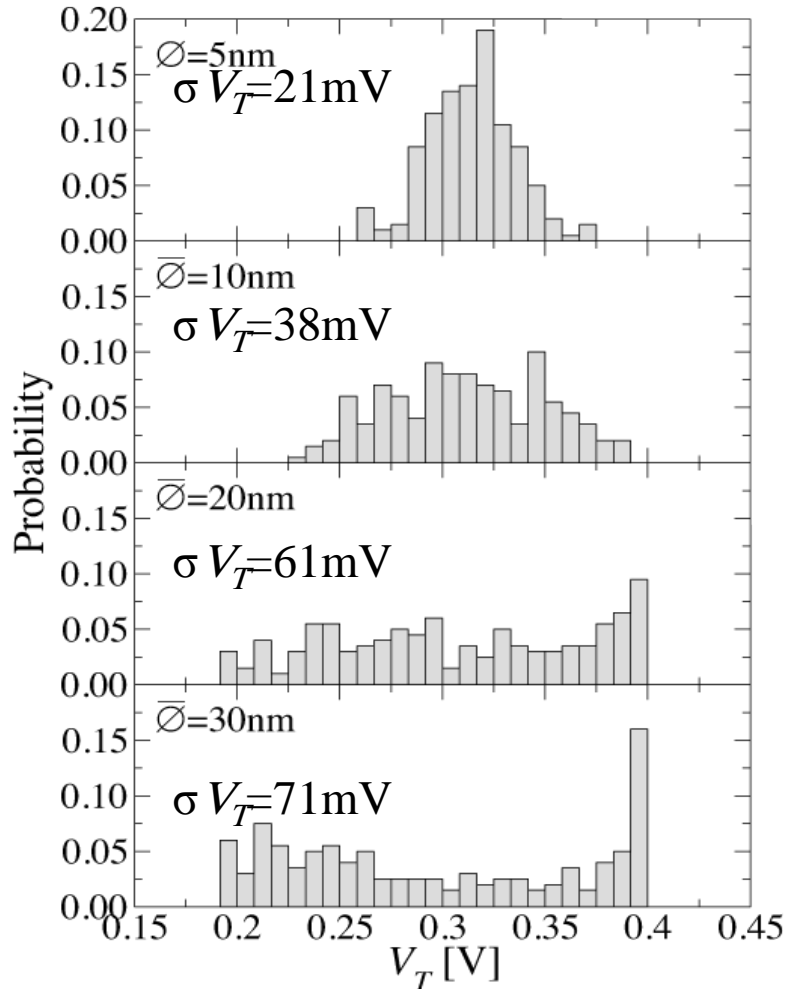


Extract compact model param.

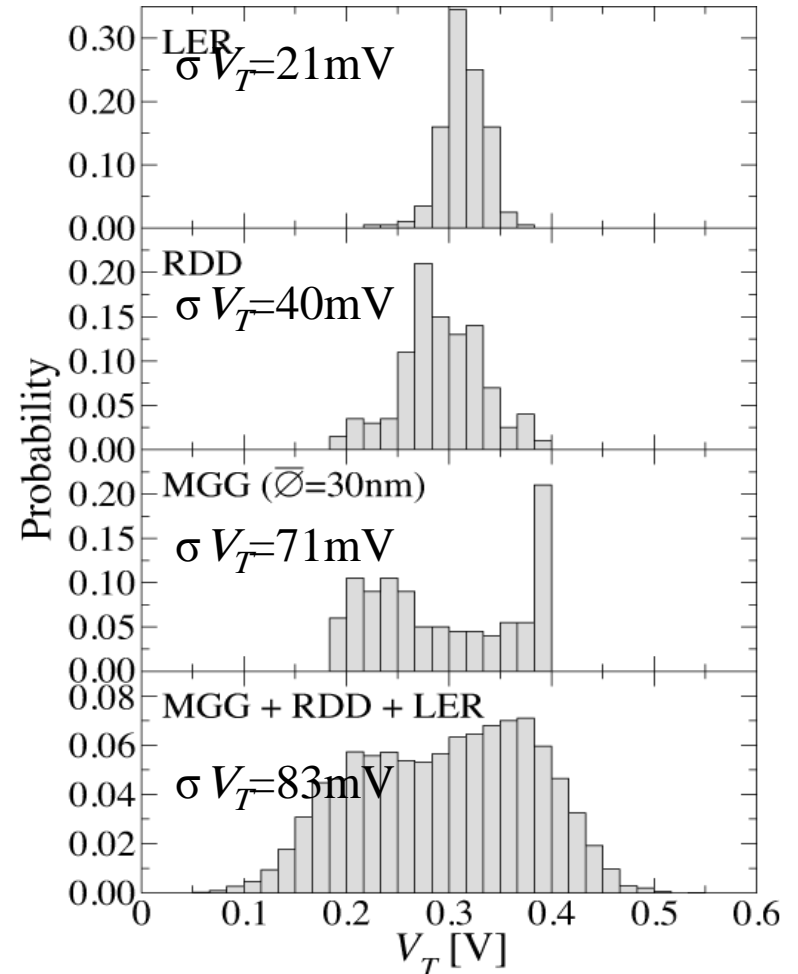


Sensitivity of metal gate grain size to variability

Sensitivity σV_T to metal grain size



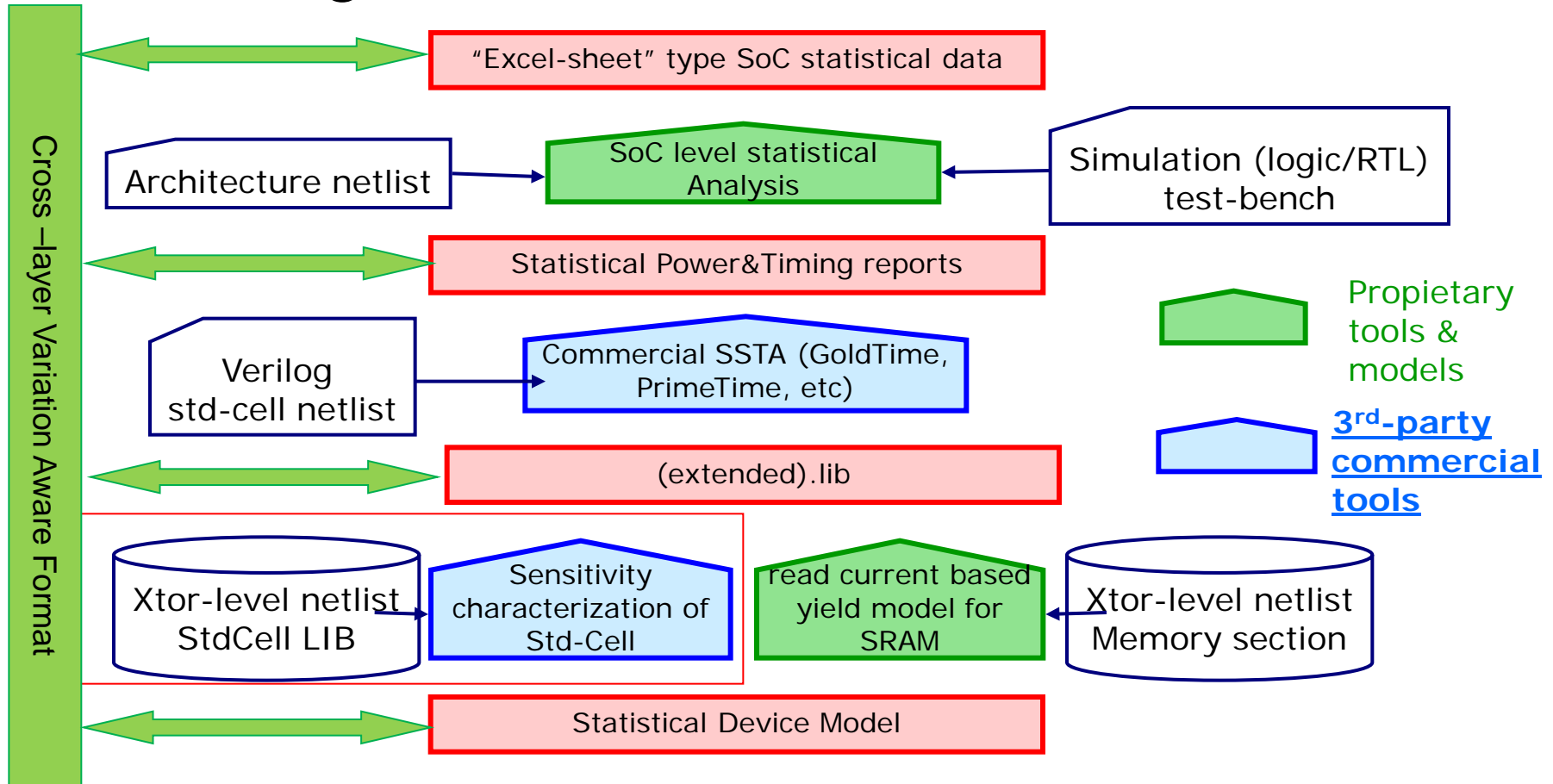
Sensitivity σV_T to variation source



Overview

- General project objectives and innovation
- Work plan and status:
 - Technology modeling
 - Circuit to system modeling
 - IC design
 - Processor integration
 - System integration
- Conclusions

Circuit to SoC variability analysis: holistic modeling flow



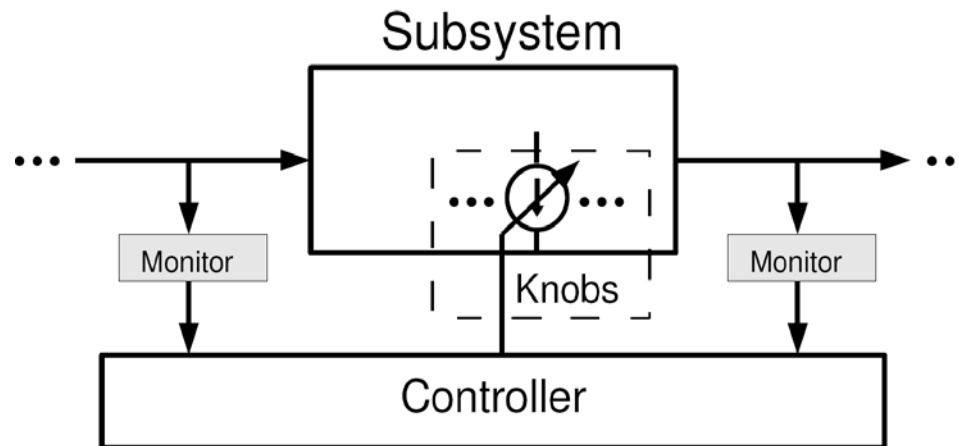
Statistical Analysis Flow from device to SoC level

Overview

- General project objectives and innovation
- Work plan and status:
 - Technology modeling
 - Circuit to system modeling
 - IC design
 - Processor integration
 - System integration
- Conclusions

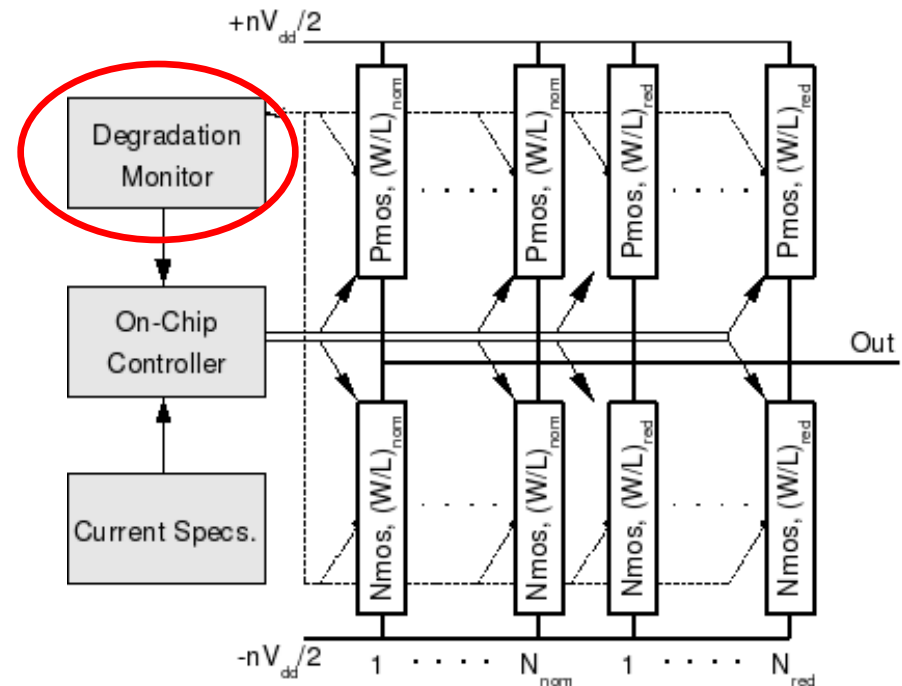
Variability resilient IC design

- Knobs & Monitor principle : adjust system configuration according to:
 - Actual, not worst case performance
 - Degradation as function of workload and service time
 - => Performance guaranteed at all time



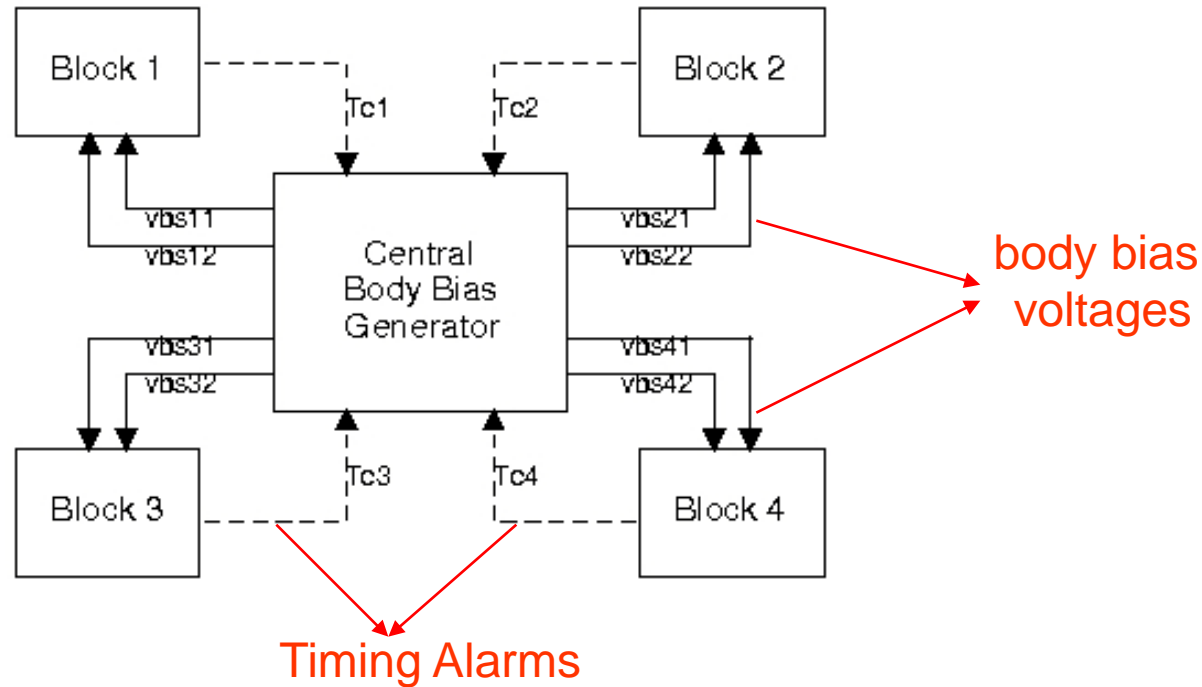
Mixed signal design

- Example circuit: high-voltage output driver
 - Low R_{on} needed to preserve power efficiency
 - Additional stages are activated depending on the output current measured



Digital design

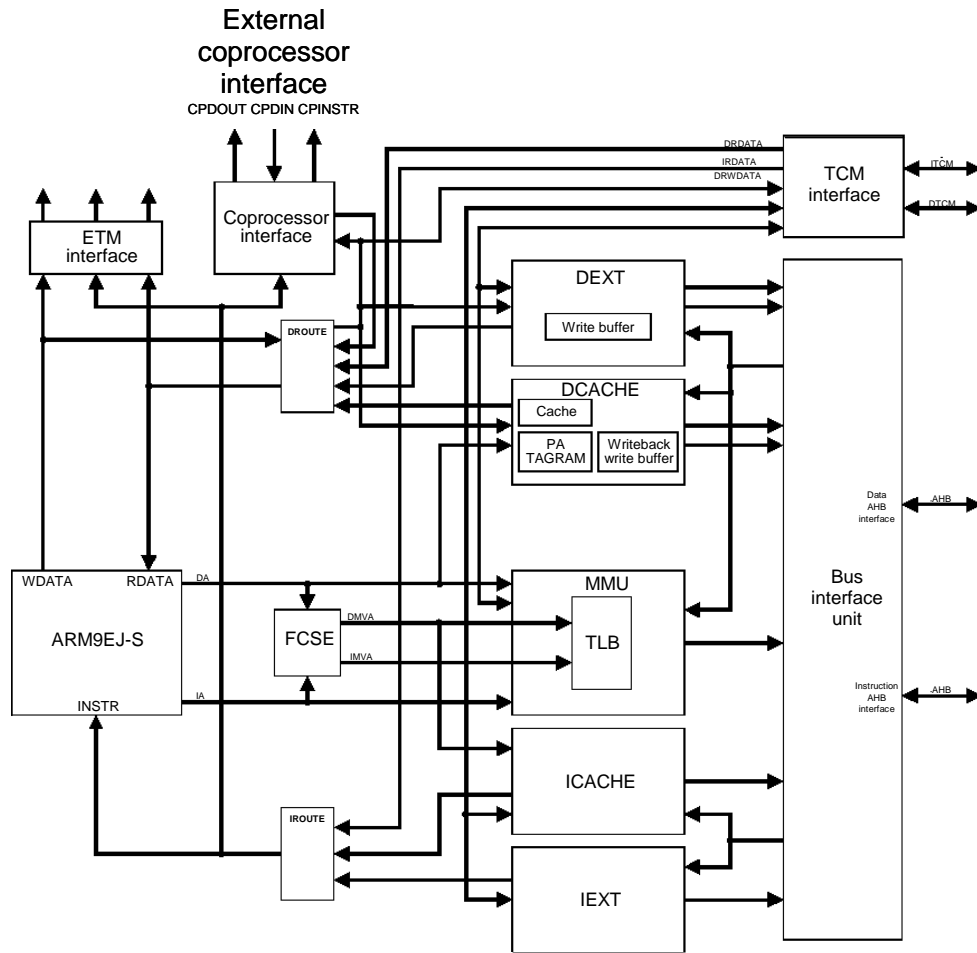
- Selective Forward Body Biasing to correct for timing violations



Overview

- General project objectives and innovation
- Work plan and status:
 - Technology modeling
 - Circuit to system modeling
 - IC design
 - Processor integration
 - System integration
- Conclusions

Processor level integration of the building blocks into an evaluation system.



ARM926:

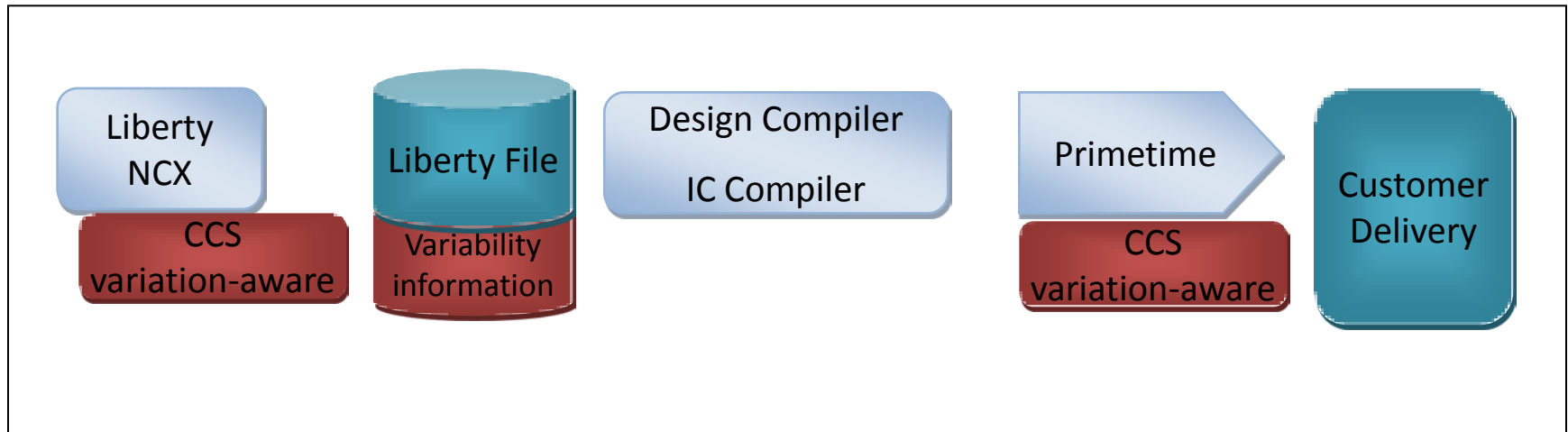
- Reference flow for Variability Aware Modelling
- Quantify variability at processor level
- Vehicle for evaluation of adaptive techniques (ABB)

Development of a validation flow for commercially available solutions

■ Reference flow:

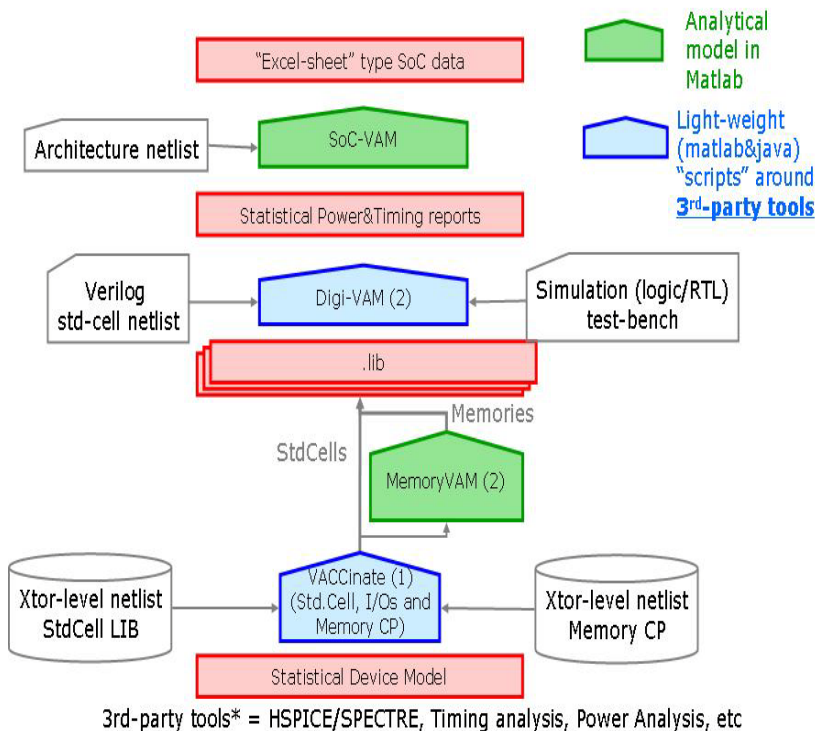
- To evaluate options commercially available
- Models Adaptation issues

■ Need for accuracy analysis



Integration and deployment of an alternative state-of-the-art flow

Variability Aware Modeling (VAM) from technology to SoC



The VAM flow follows the classic levels of design abstraction

- device compact models
- standard cells and memories
- digital IP blocks
- SoC integration level (developed within REALITY-WP2).
- Vertically integrated database to exchange variability info across levels (developed within REALITY-WP2)

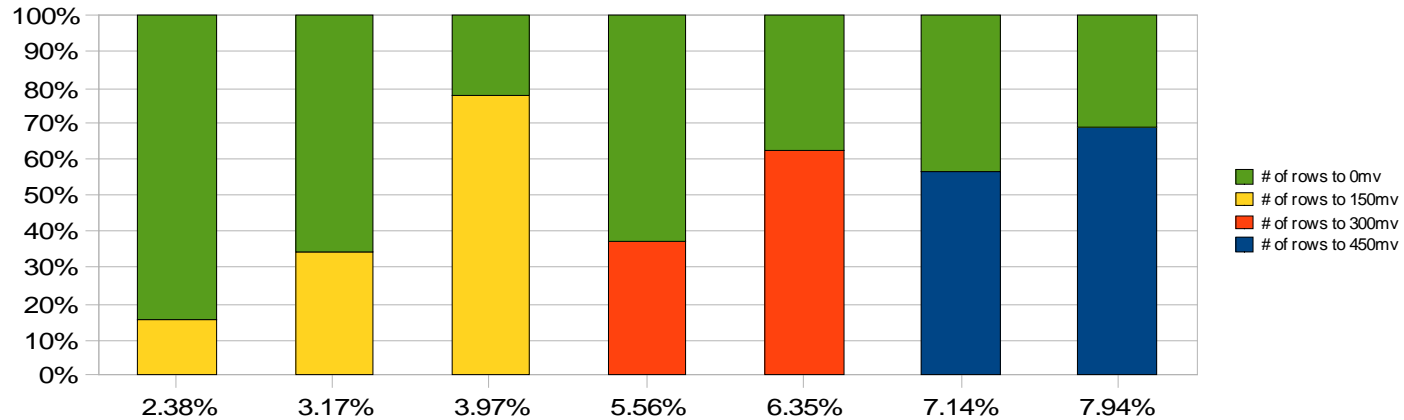
From device variations to processor variations (IBM/ST 32nm ARM926)

	Local Variability(*)		Global Variability(**)		Total		Corner	Units
	-3 σ	+3 σ	-3 σ	+3 σ	-3 σ	+3 σ	TT	
Vth	120	480	255	345	119	481	300	mV
	Local Variability		Global Variability		Total		Corner	Units
	-3 σ	+3 σ	-3 σ	+3 σ	-3 σ	+3 σ	TT	
Critical Path	1435	1593	1395	1698	1524	1759	1506	psec
Leak Power	7420	7583	5456	8552	6144	9228	6824	uW
Energy/cycle	301.6	305	295	308	295.6	310	300.8	pJ

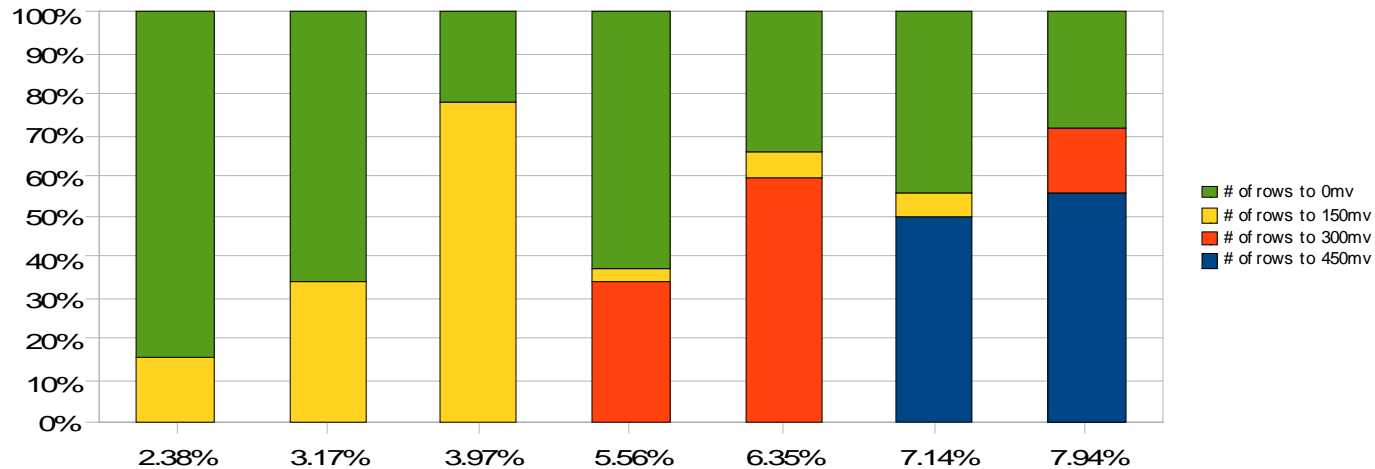
(*) minimum transistor sizes

(**) transistor size independent

Number of Rows (%) for each ABB island for ARM9 ALU



Speedup with 2 clusters

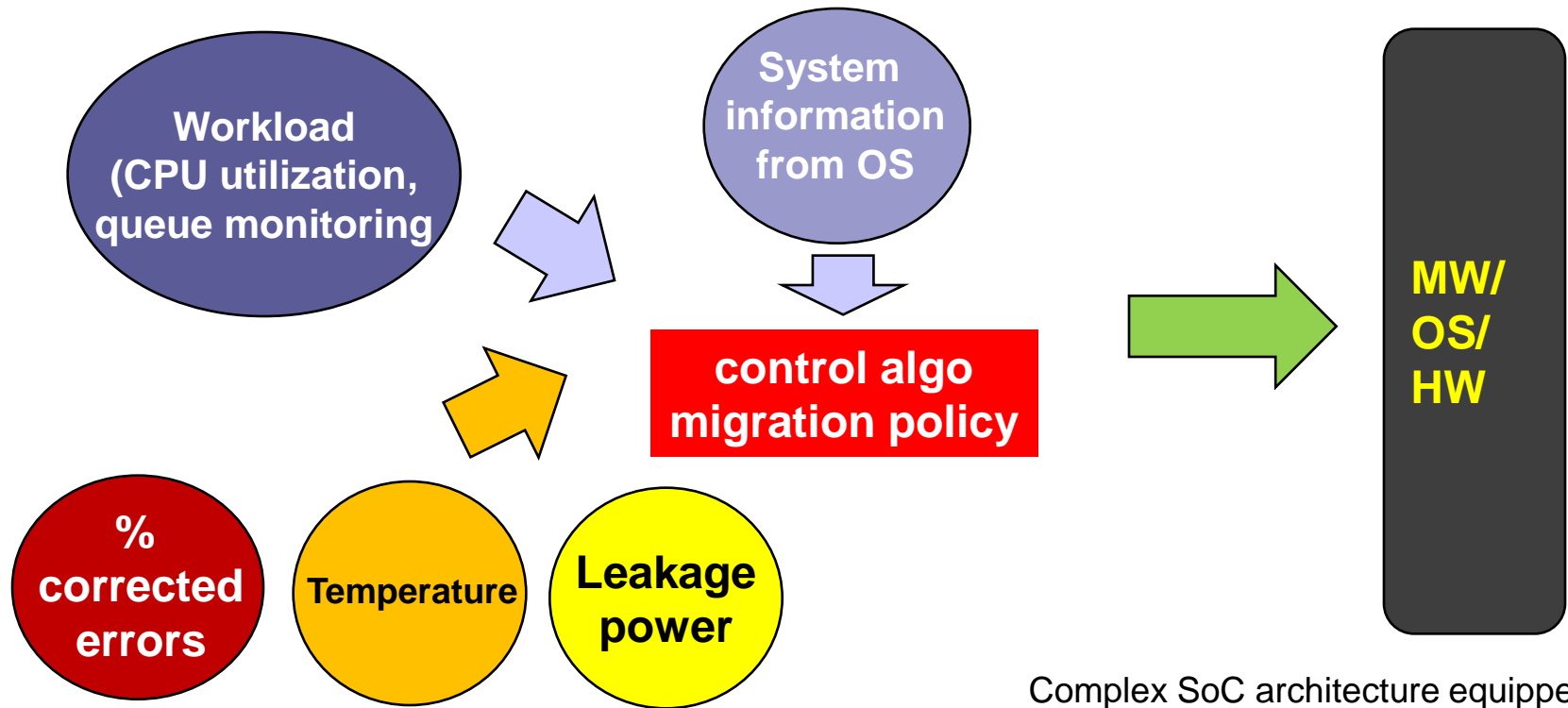


Speedup with 3 clusters

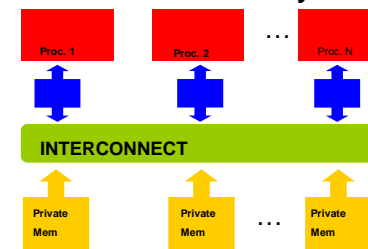
Overview

- General project objectives and innovation
- Work plan and status:
 - Technology modeling
 - Circuit to system modeling
 - IC design
 - Processor integration
 - System integration
- Conclusions

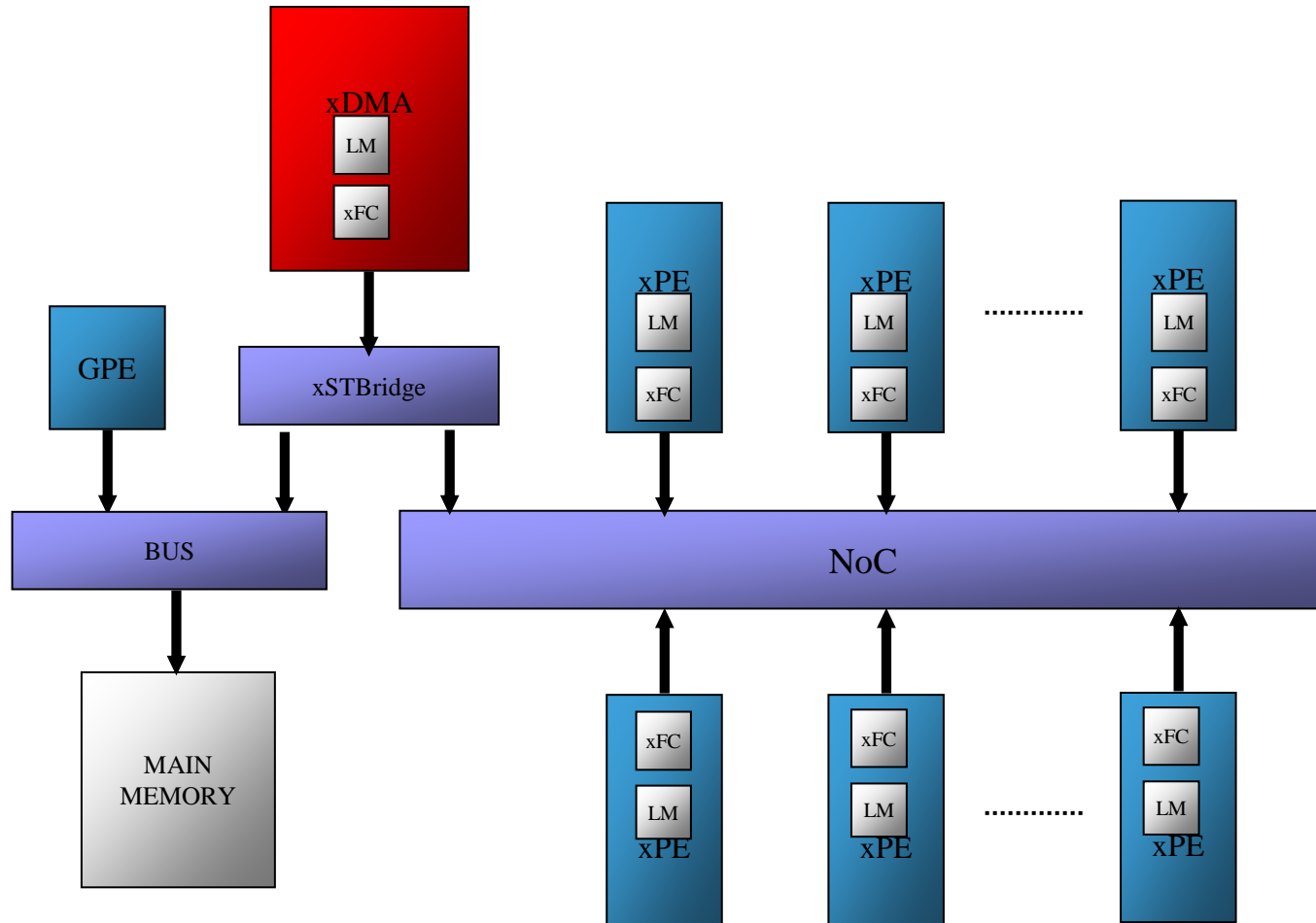
Variability and reliability resilient system design



Complex SoC architecture equipped with on-board variability monitors

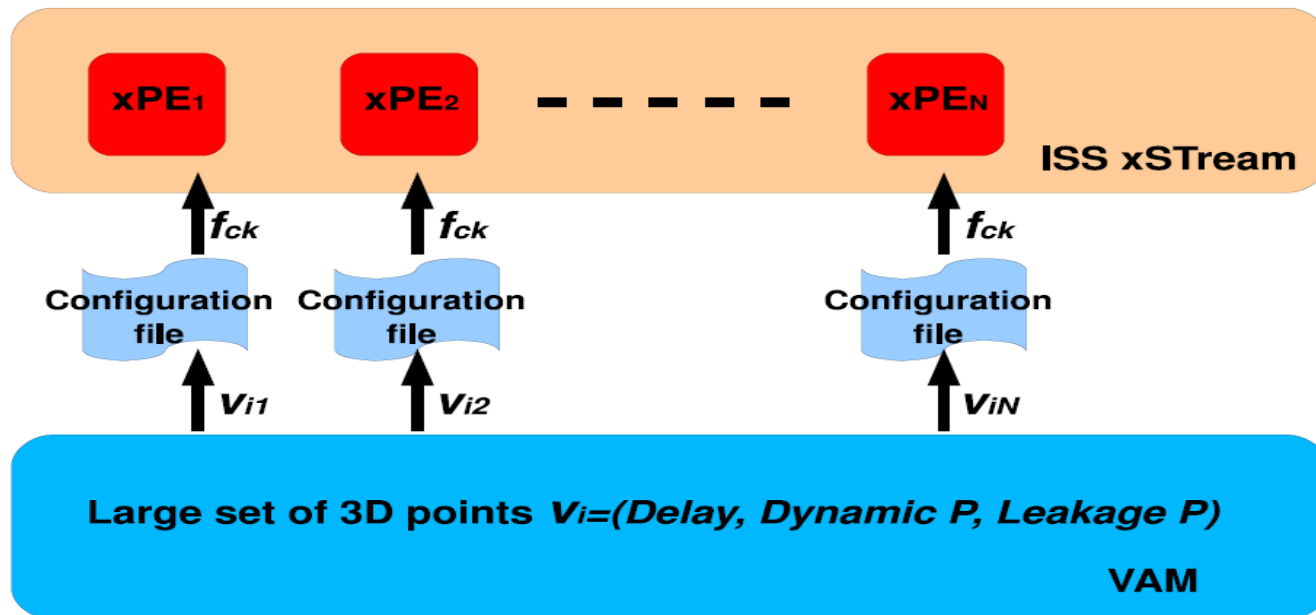


Multimedia Multicore platform



Processor to System integration

- Statistical longest path delay, dynamic energy, and leakage power per core from variability aware modeling flow
- ISS plug-in set clock frequency according to longest path delay, and stores power values for evaluation of the energy consumed during a run.



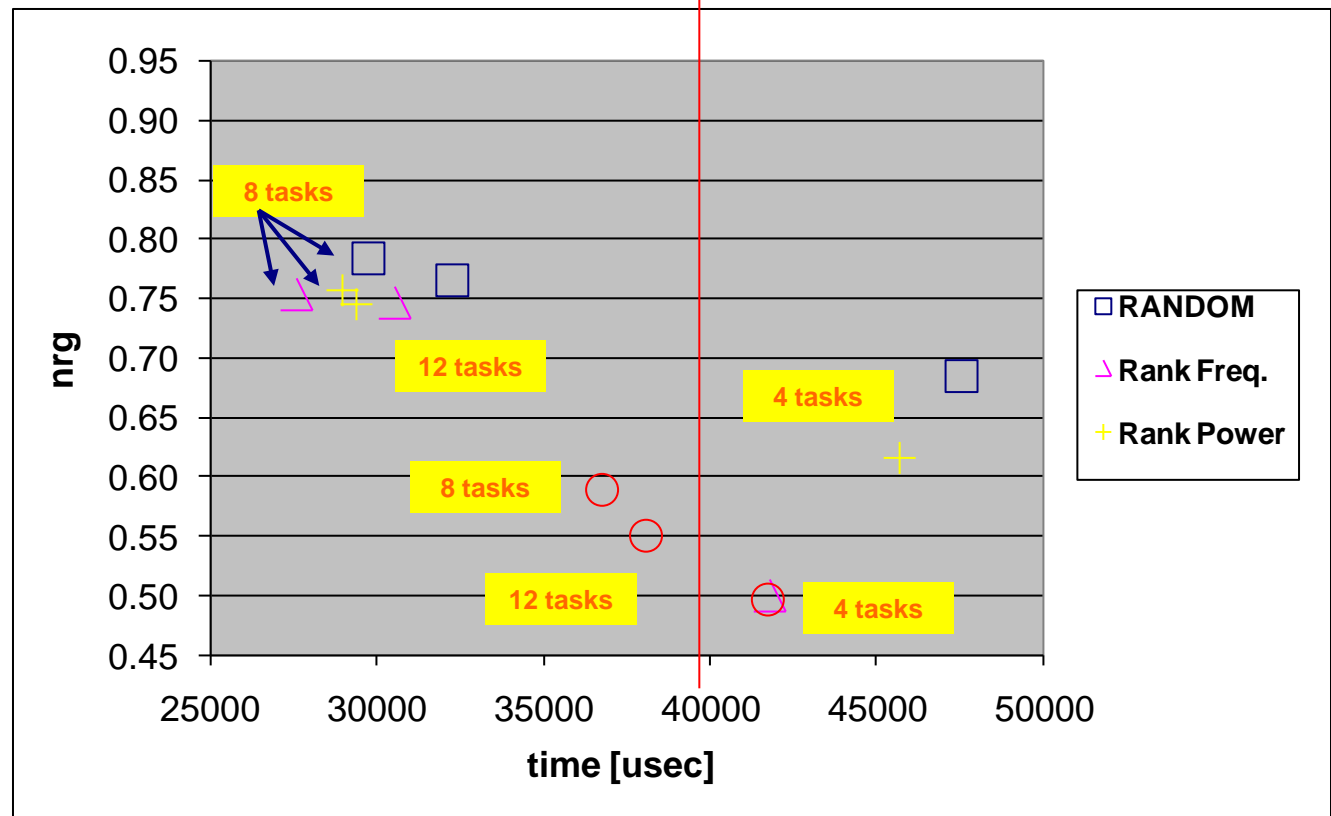
System benchmarking

- Modified MPEG2 decoder:
 - 1 control thread (CPU) + N decode threads (hardware threads of xPEs)
 - Each decoding thread decodes an N-th of the frame slices and one vertical portion of the frame image



System Platform Results

- 4 tasks do not expose enough granularity to meet application deadline for all frames, Online-policy and Rank Frequency shows more resilience.
- *Online-policy consumes less energy in all cases*



Overview

- General project objectives and innovation
- Work plan and status
- Conclusions

Conclusions

- Under technology challenges:
 - Increased variability at smaller feature sizes
 - New materials and devices requires understanding of design margins

- To address new design challenges:
 - How to build reliable systems out of unreliable technology
 - Allowing technology scalable, energy efficient SoC systems

- Project effort along two main axes:
 - Analysis.
 - Solutions for avoidance and adaptability

- Demonstrators
 - Technology to Processor: ARM926
 - Processor to System application: ST-xStream

REALITY

Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Thank you!