

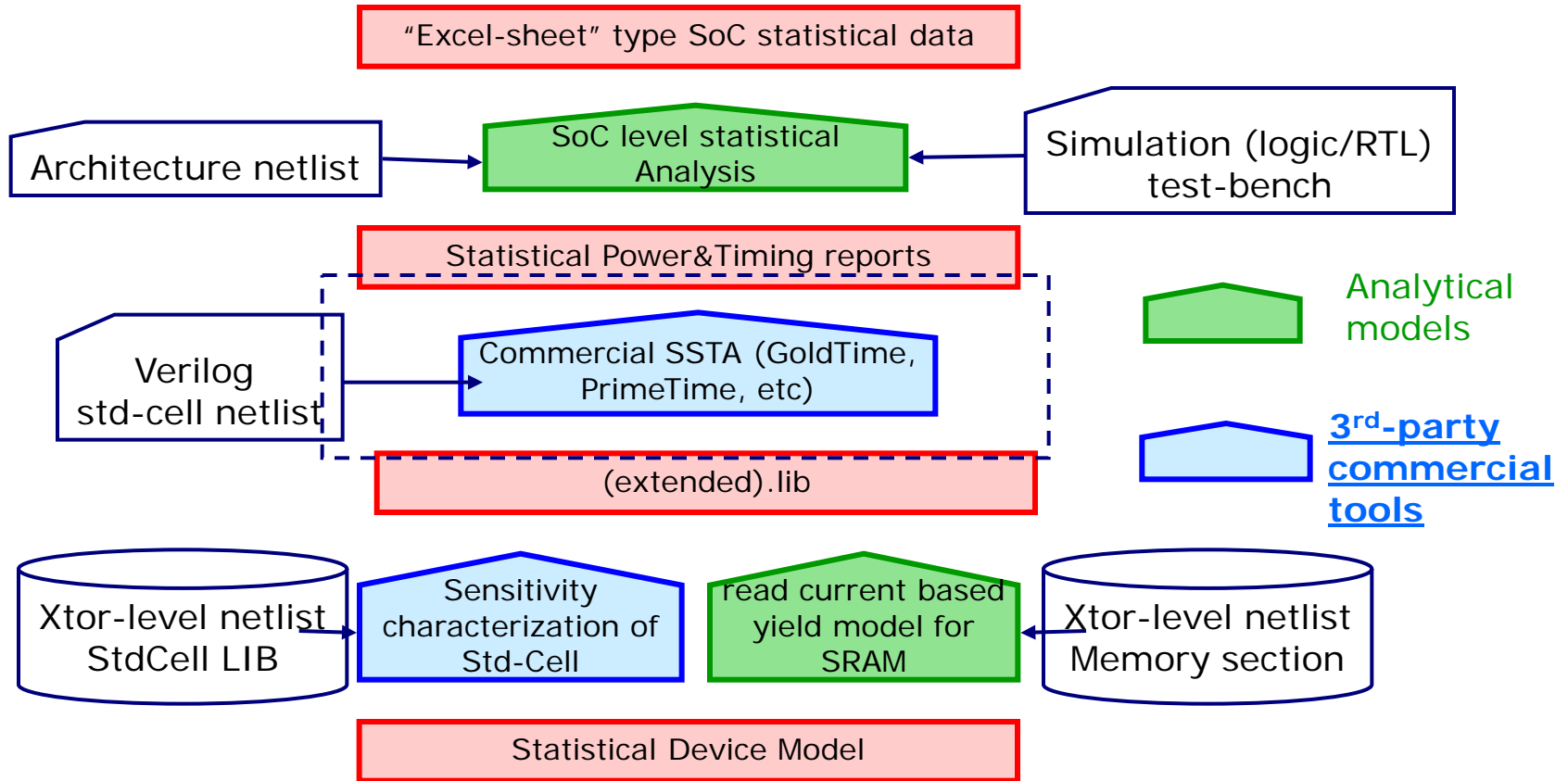
REALITY

REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Project Workshop - Work Package 6 VAM Demo and Benchmarking results



Demo



Statistical Analysis Flow from device to SoC level

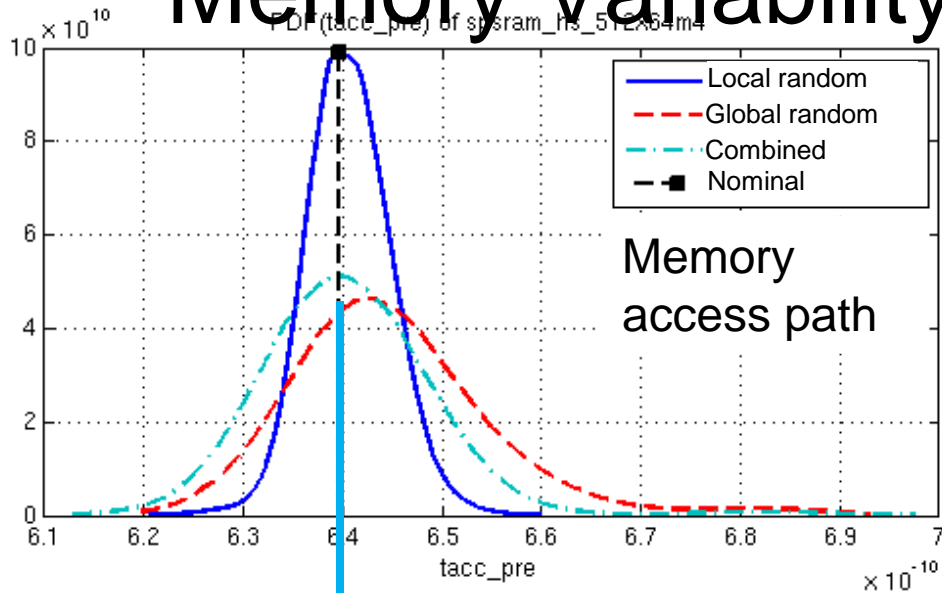
Test Vehicle: ARM926 Core

- St-32nm technology, ARM production
- 500MHz
- 27 memory modules, ARM prelim netlists
- Dhrystone power testbench
- Pre-layout
- Zero-delay clock tree

Analysis

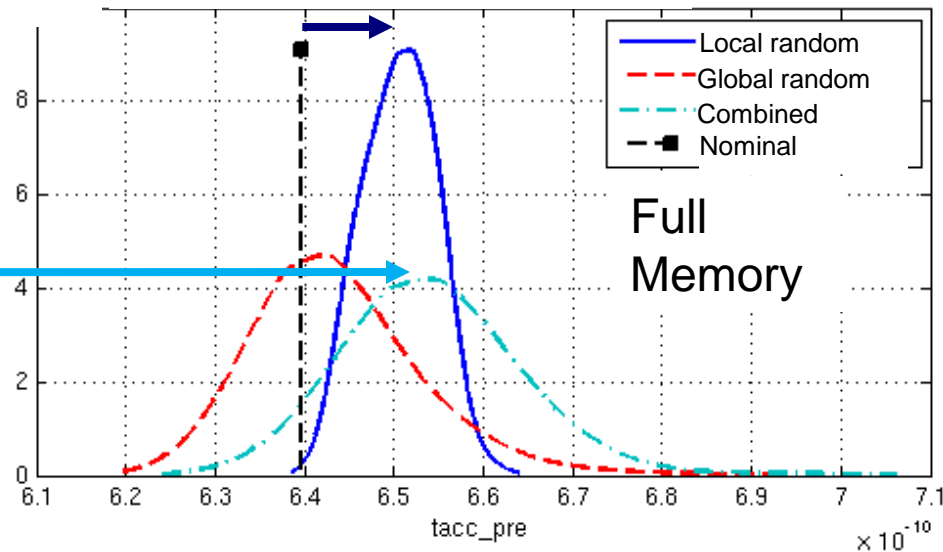
- Different corners
- 50 local, 50 global Enhanced MonteCarlo variants each corner
- Statistical cells AND memories

Memory Variability



(2) Combined variability shifts too

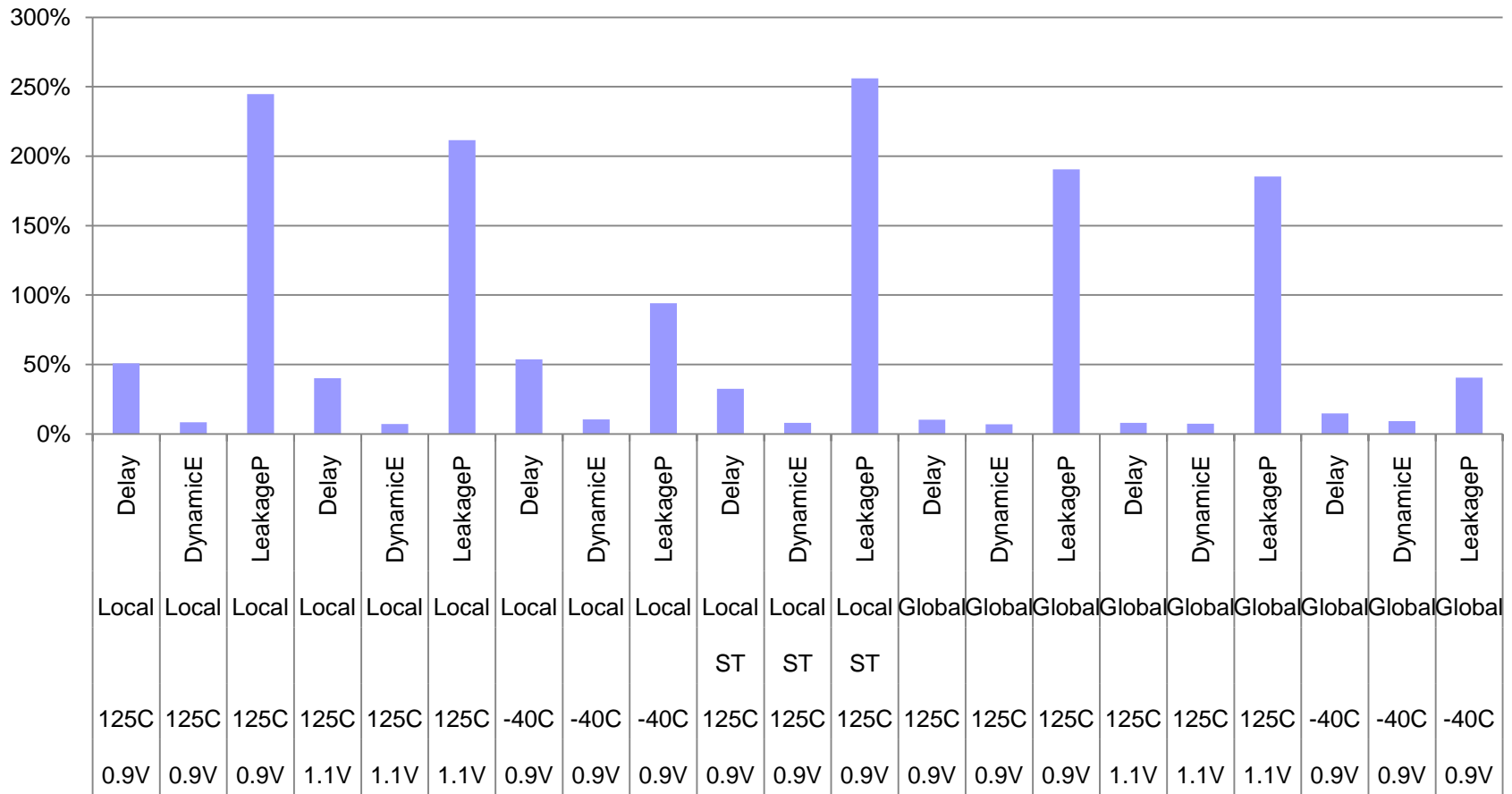
(1) Local variability shifts



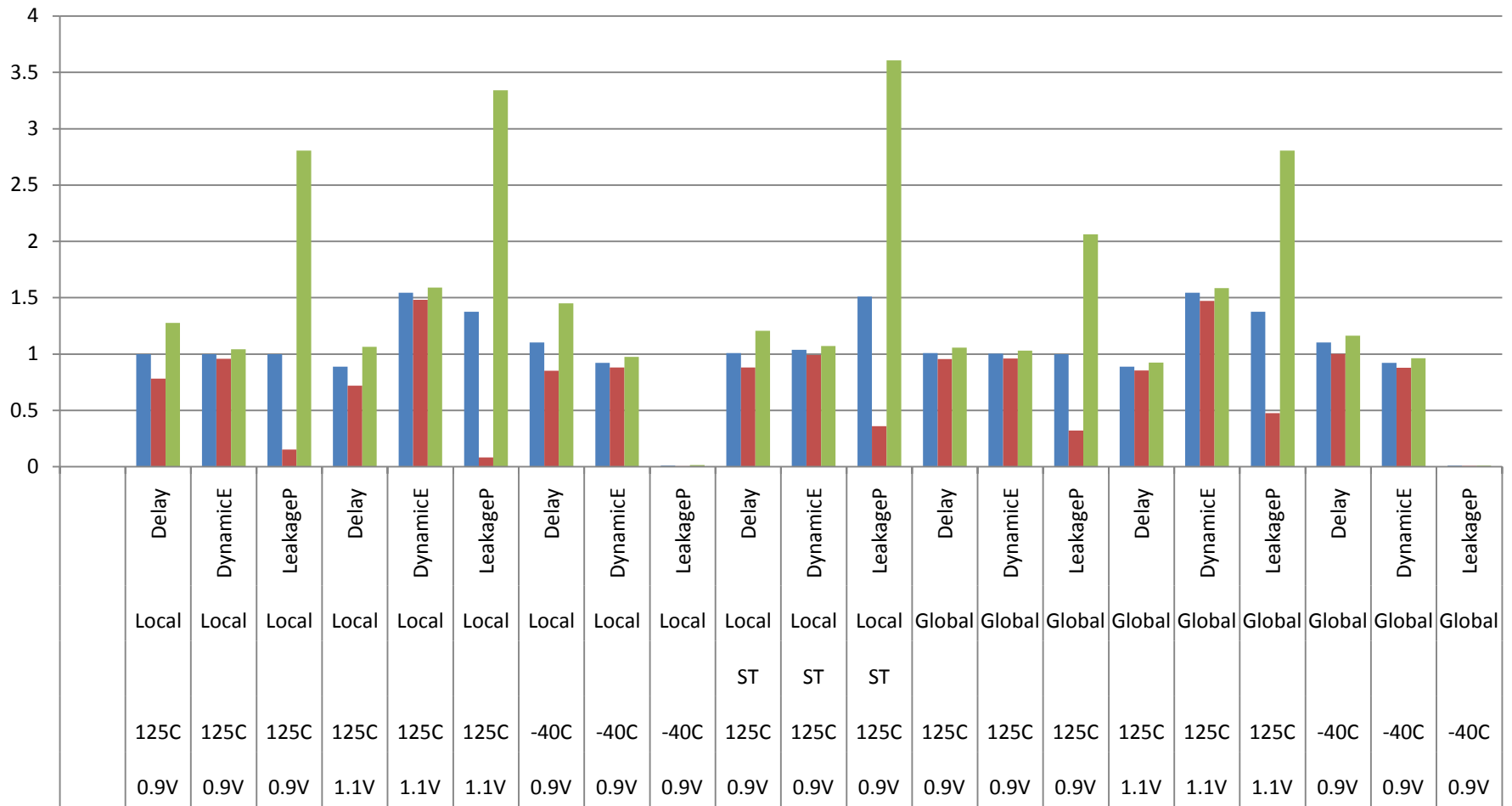
Demo Plan

- We expect to see:
 - Input netlist
 - Original timing report
 - 2x .lib variants (for memories)
 - Browsing cells, memories
 - Sample run of DigiVAM, 2 variants
 - Browsing core
 - Timing reports, power reports

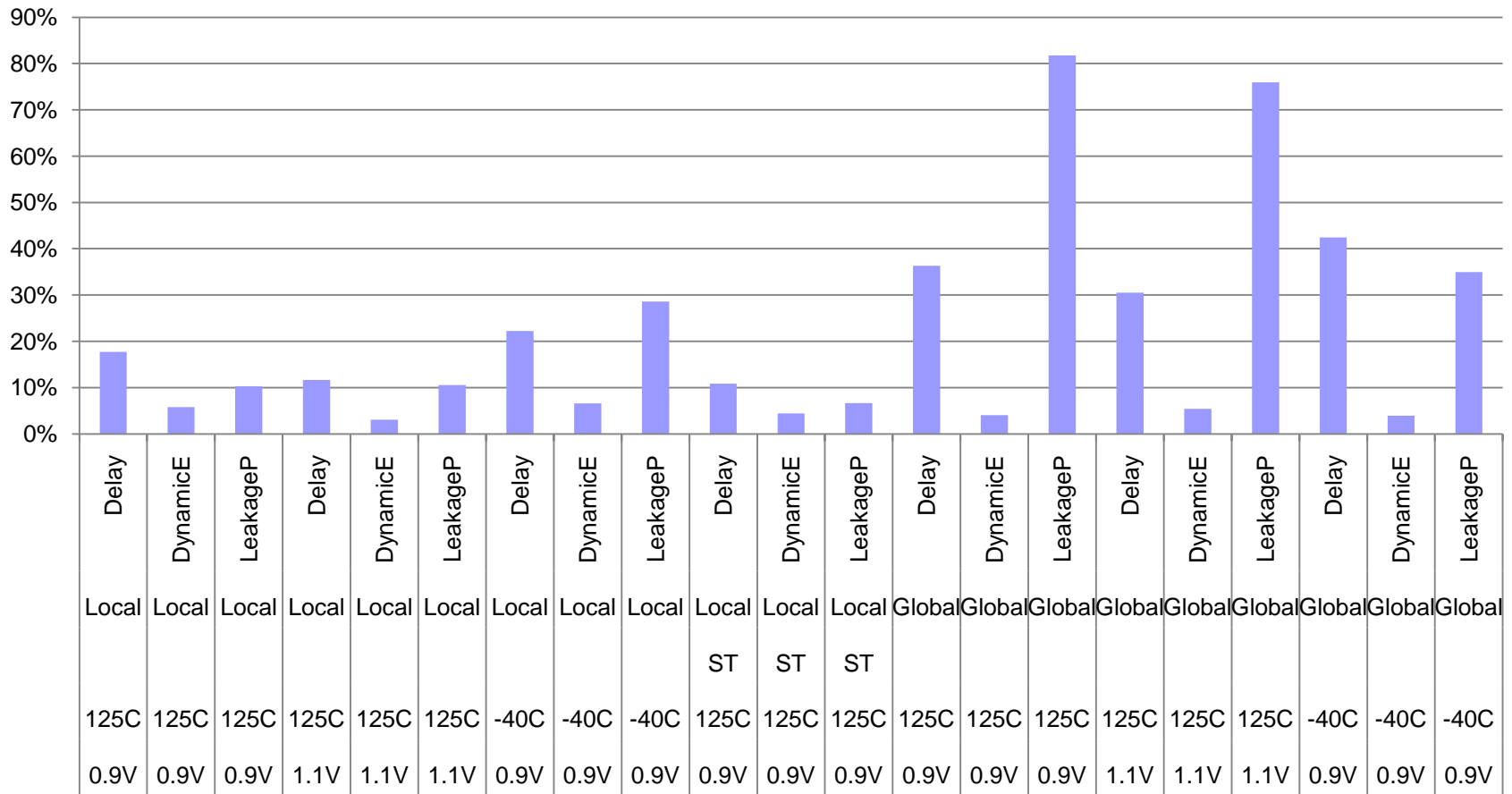
NAND2 variability



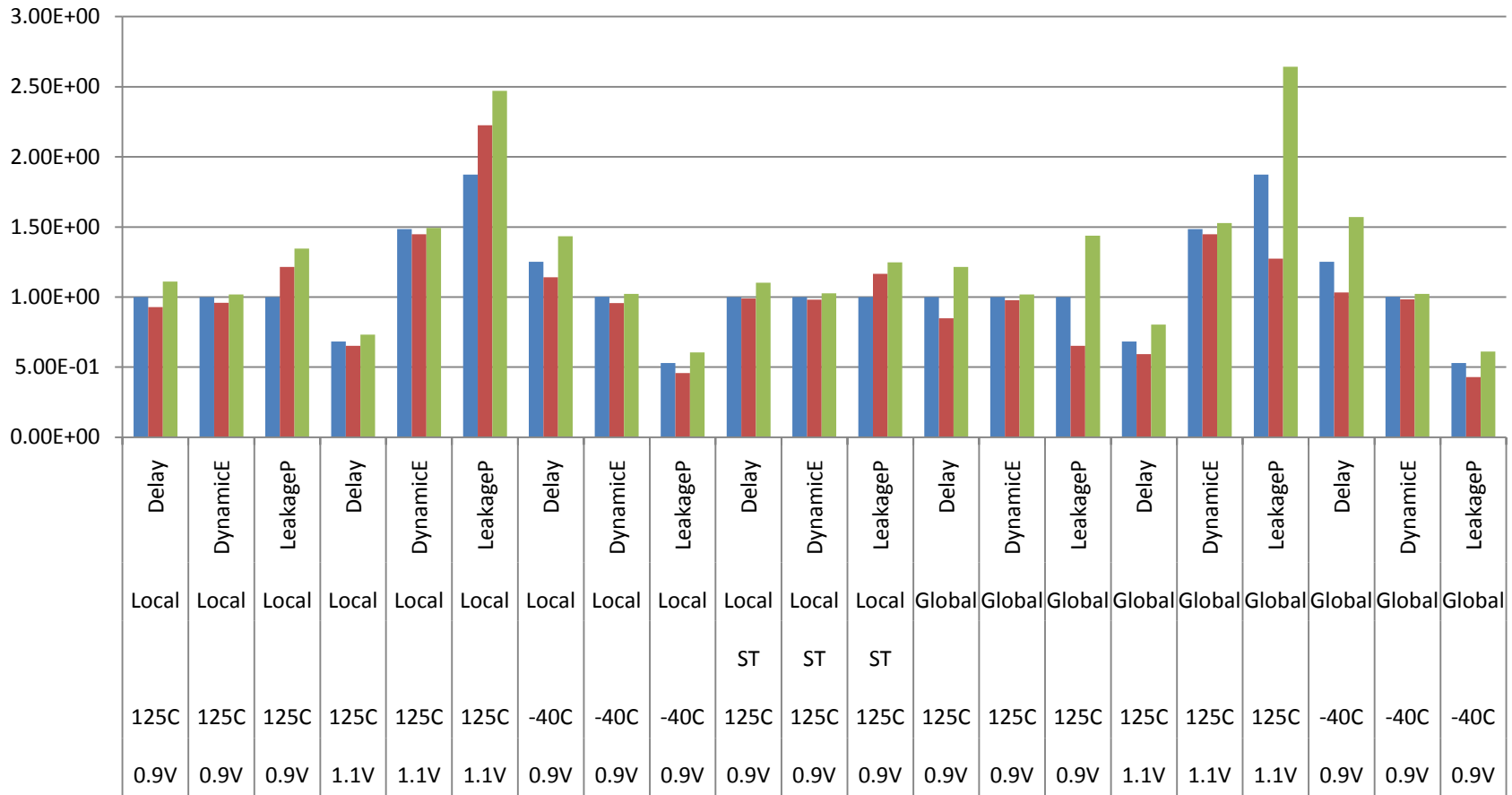
NAND2 TT, -3 σ , +3 σ



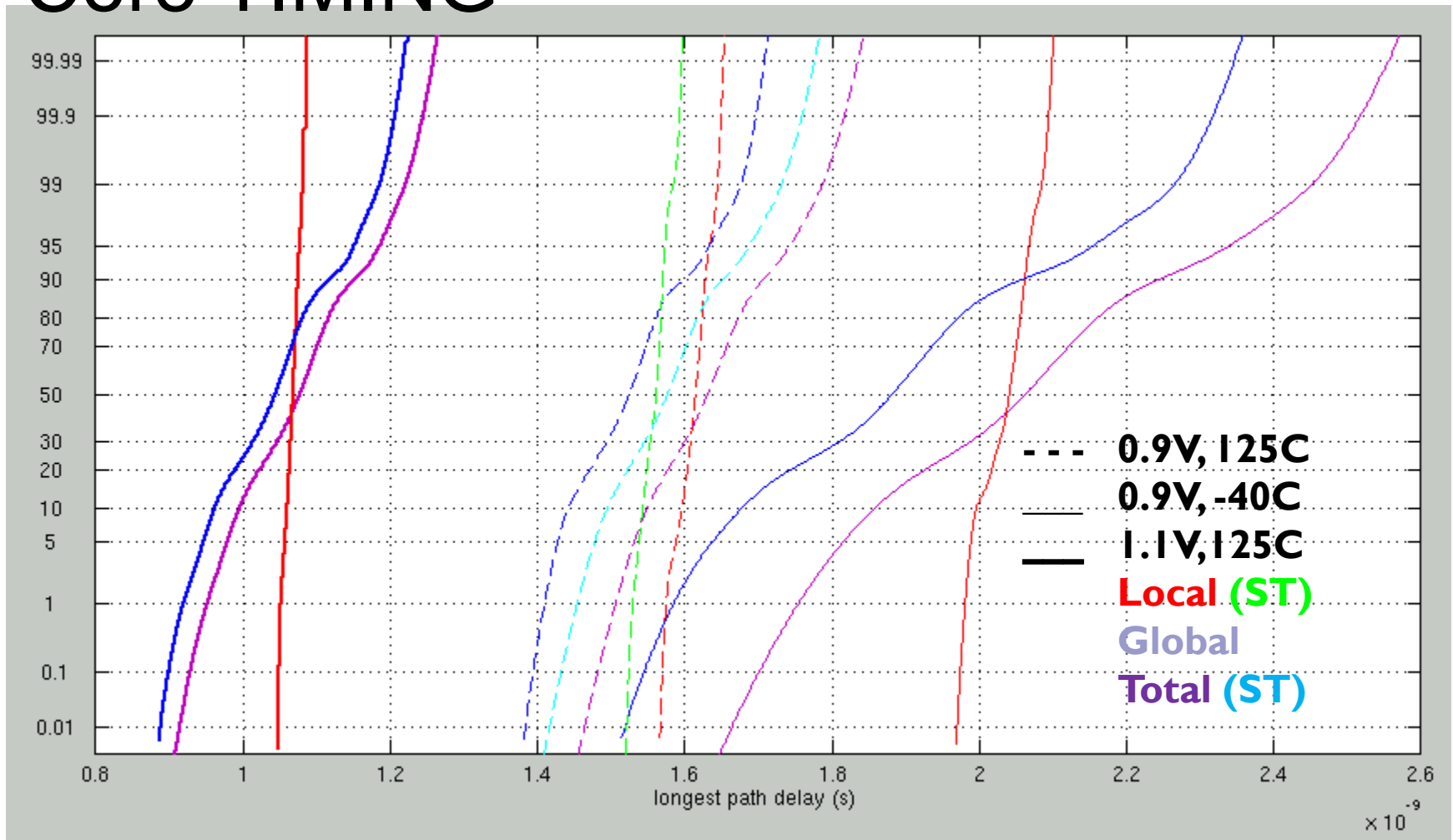
Ram1024x32 variability



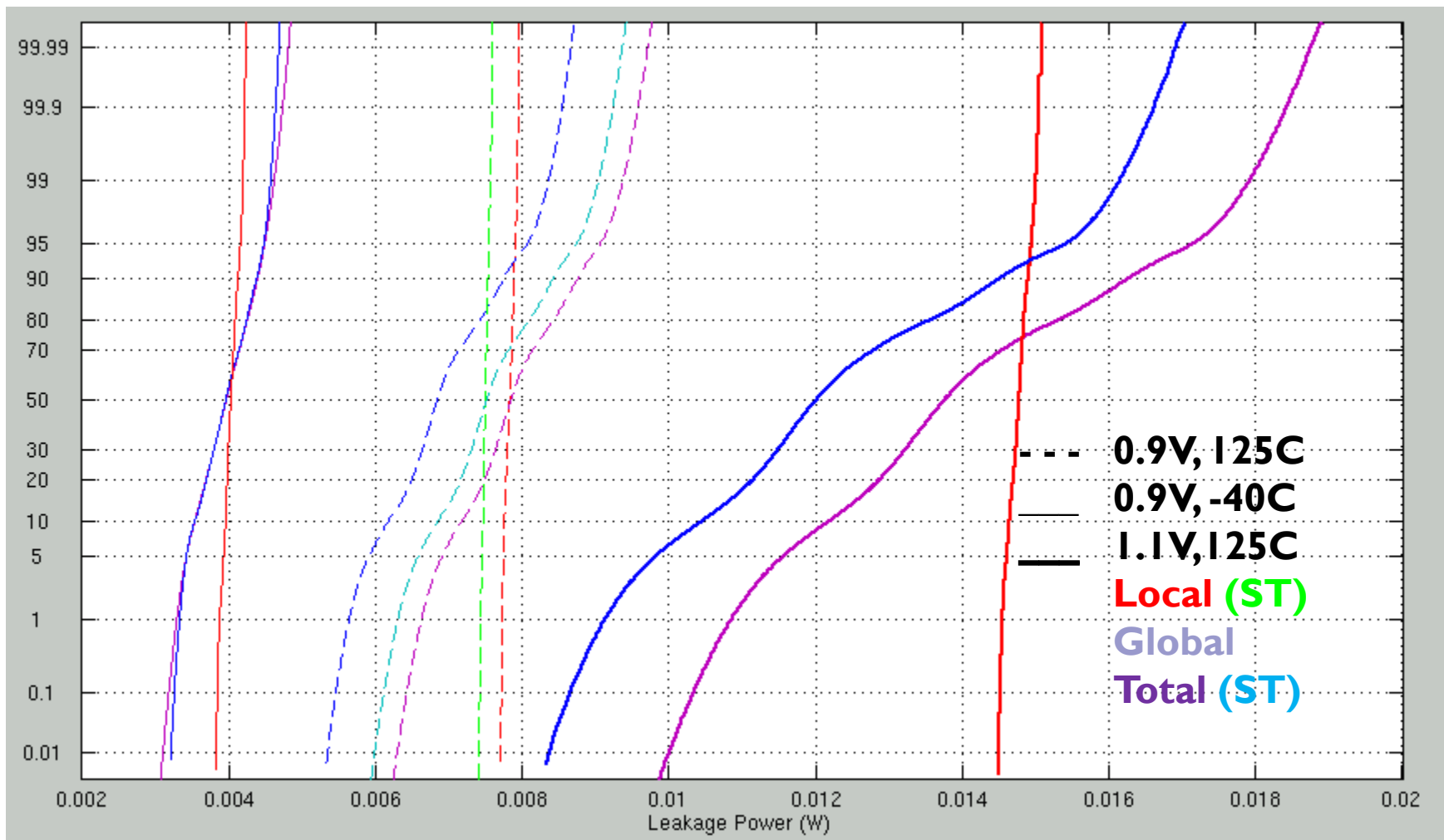
Ram1024x32 TT, -30,+30



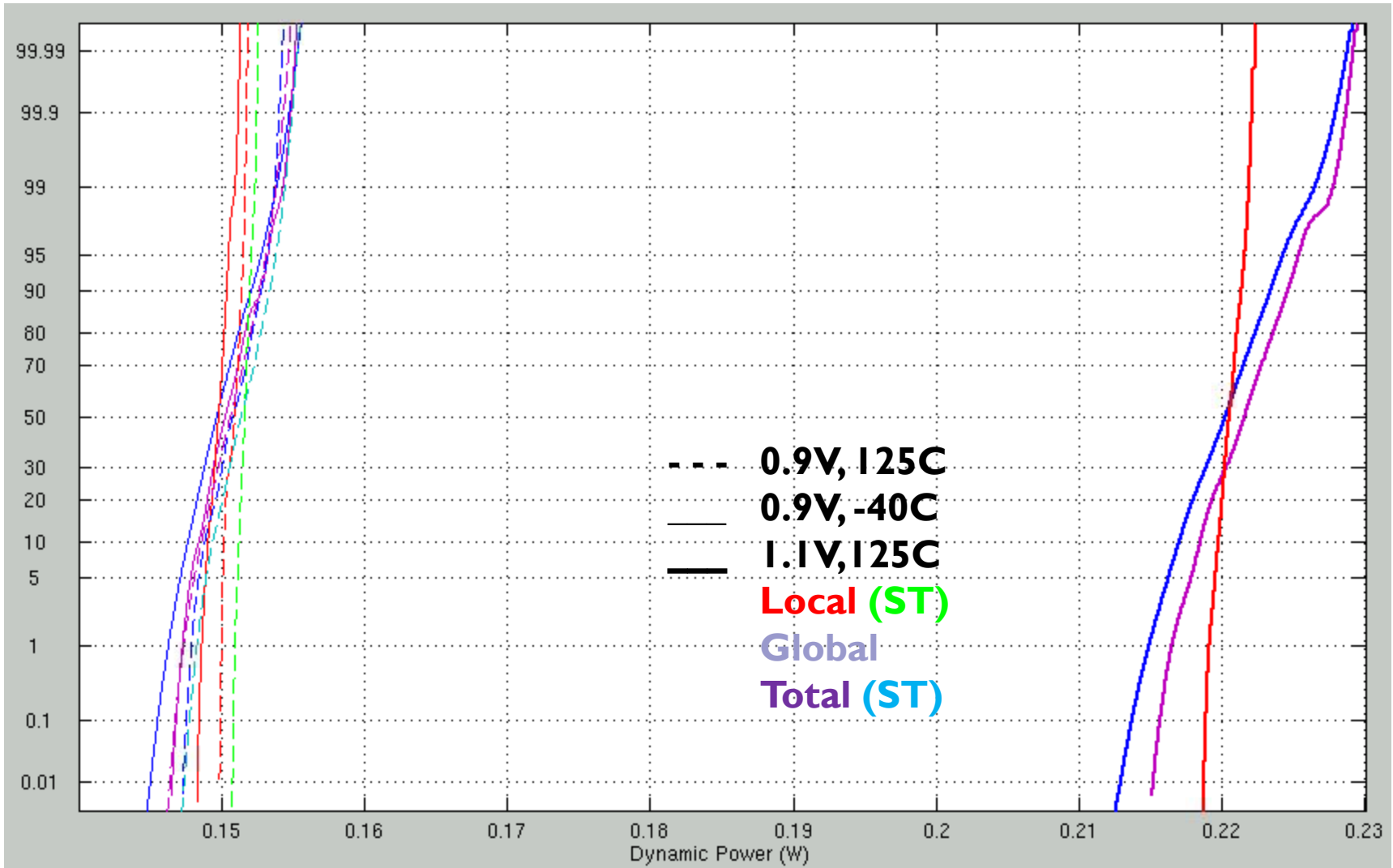
Core TIMING



CORE LEAKAGE

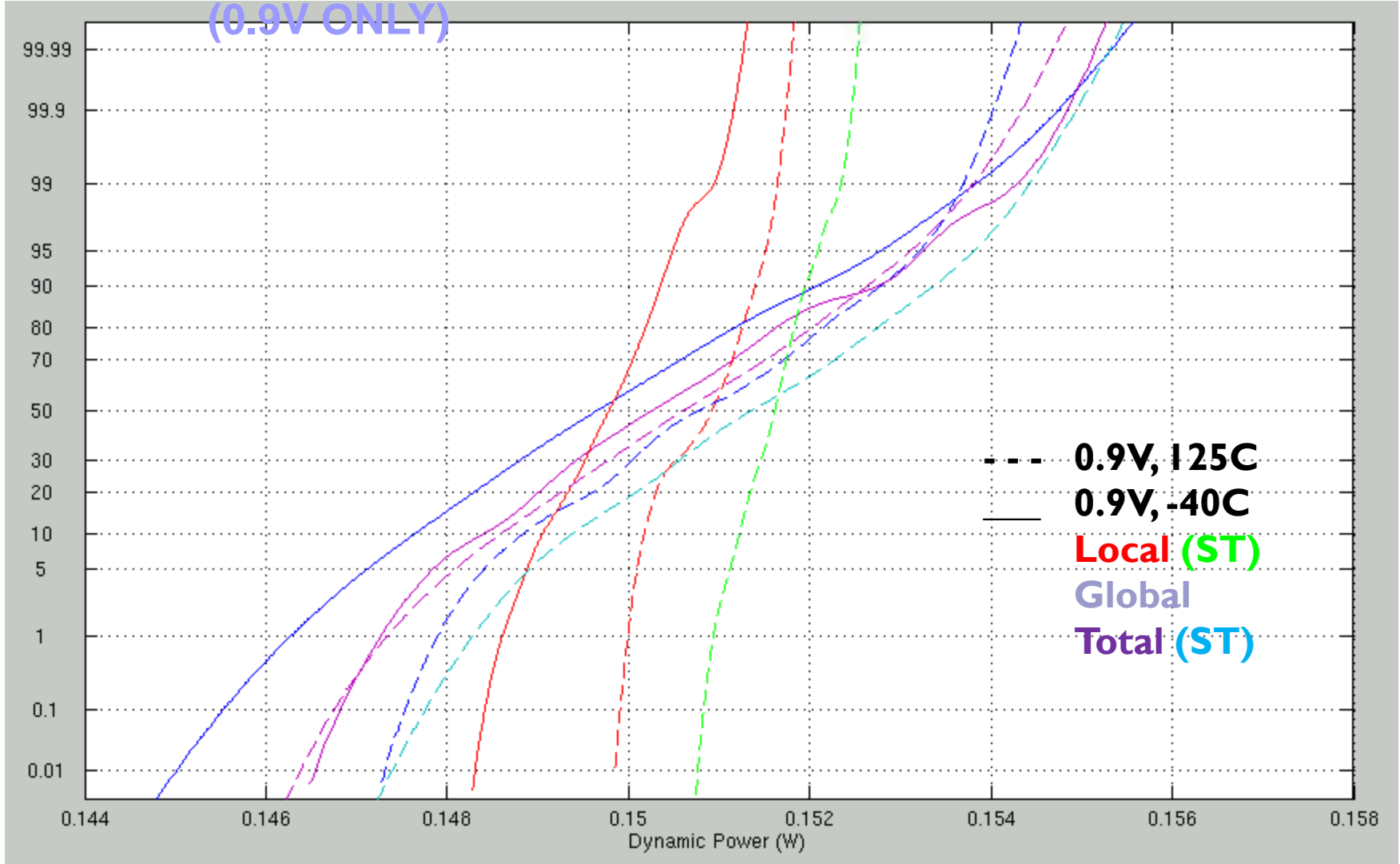


CORE DYNAMIC POWER @500MHZ

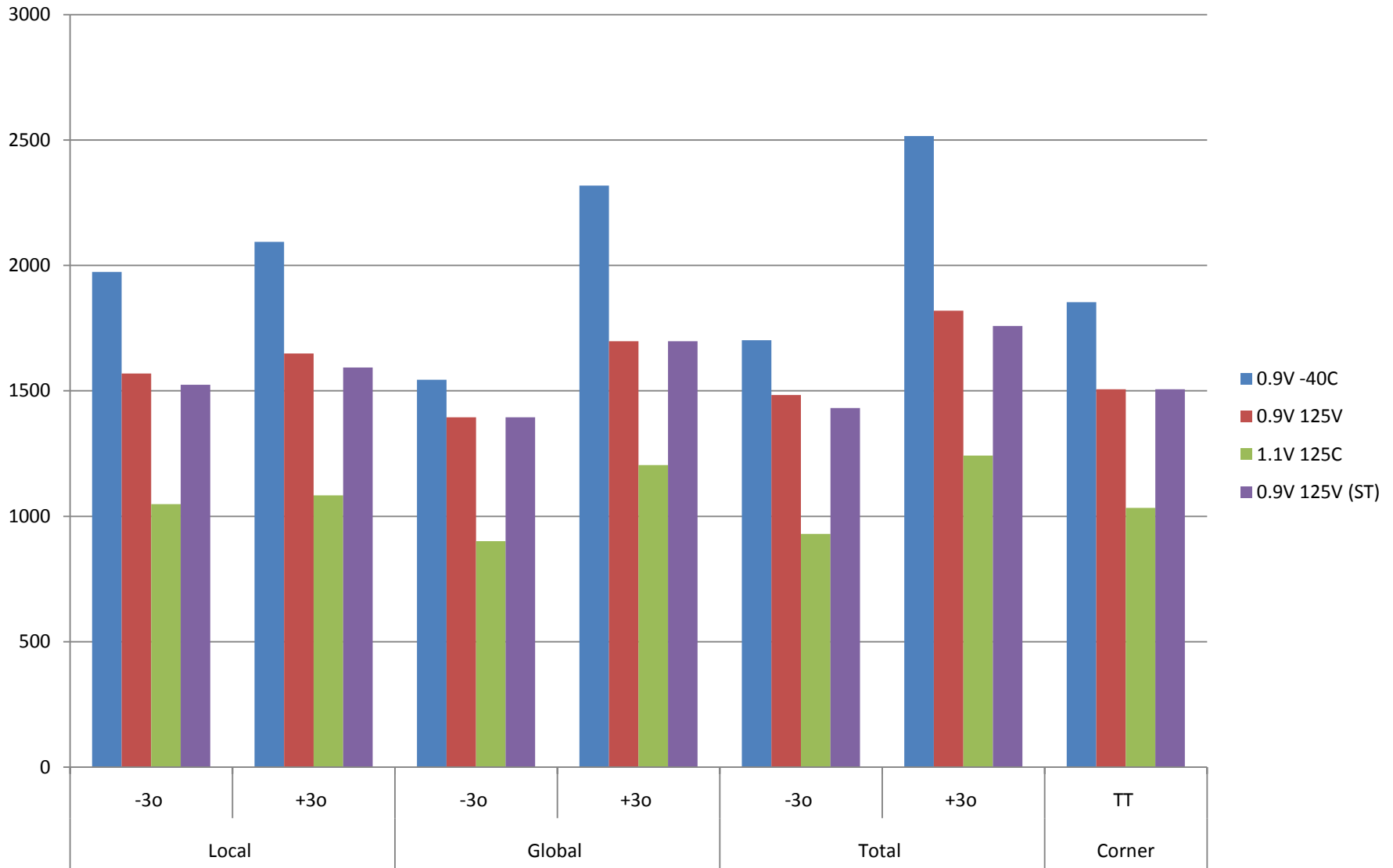


CORE DYNAMIC POWER @500MHZ

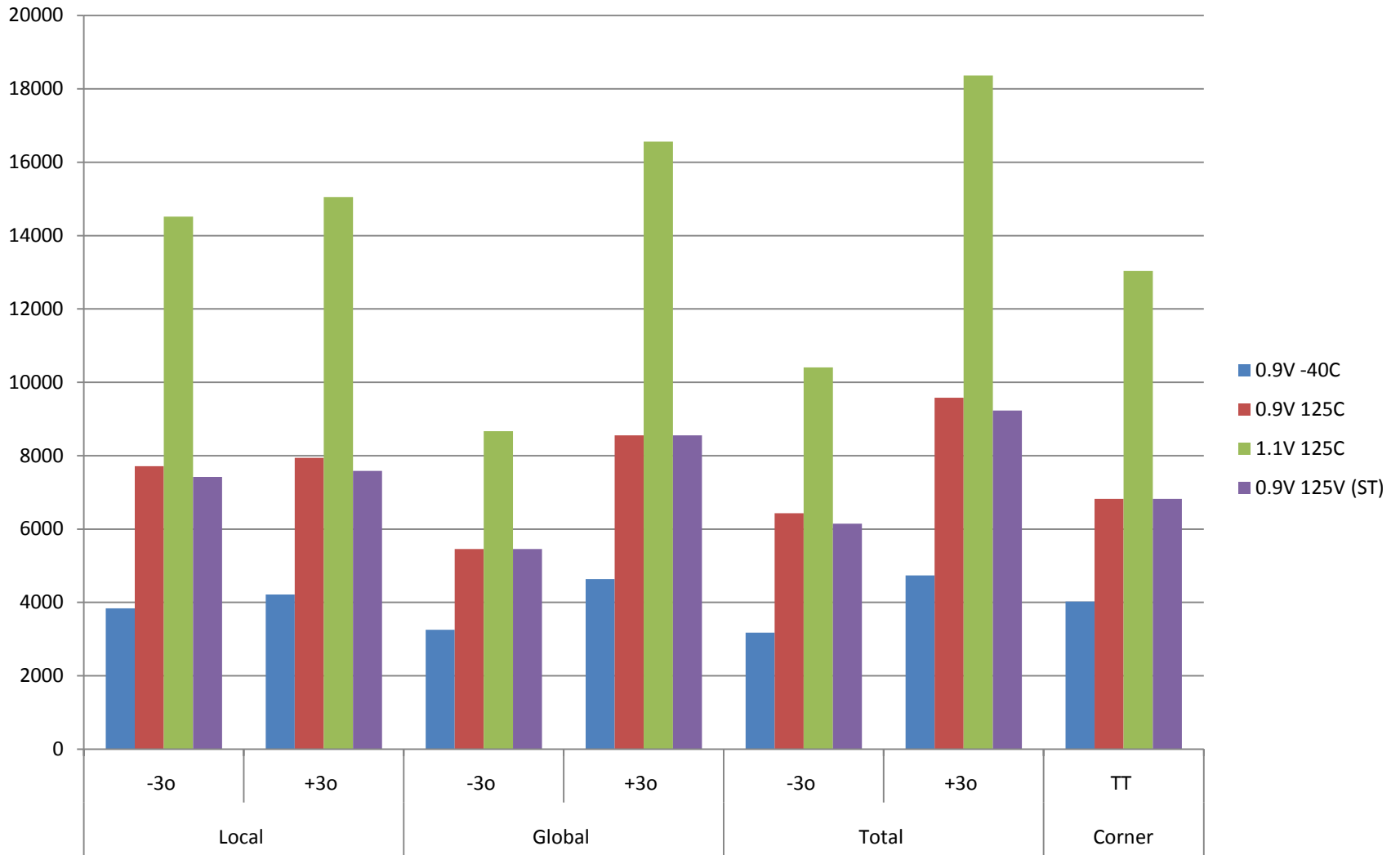
(0.9V ONLY)



TIMING RANGES



LEAKAGE RANGES



ENERGY/CYCLE RANGES

