IC Design for Reliability in nm CMOS

REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

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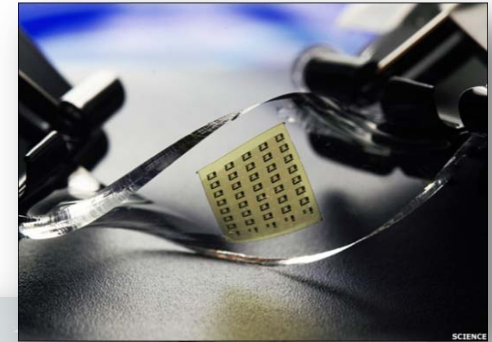
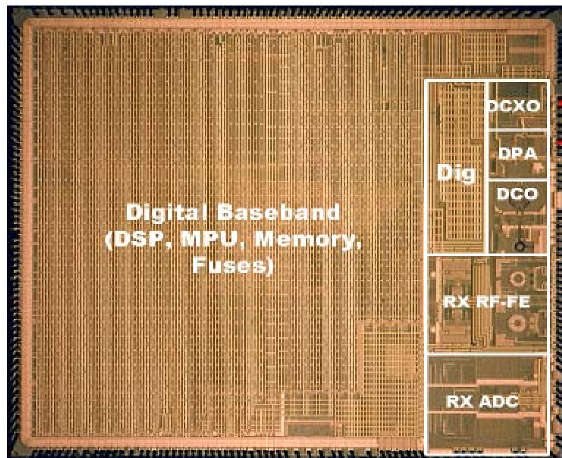
Overview

- **IC Reliability: why is this suddenly an issue?**
- Capturing the physics
- Analyzing a circuit
- Case study: SRAM design
- Conclusions

Towards Systems-on-Chip (SoC)

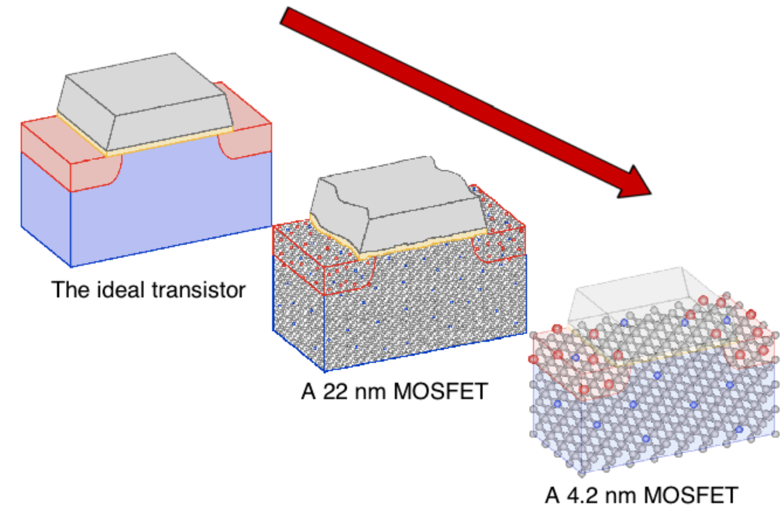
- Move to increased levels of integration
  - reduced cost, size/volume, power
  - improved performance
- Increasing chip complexity
  - integrated *heterogeneous* systems
    - mixed hardware/software
    - mixed RF/analog/digital

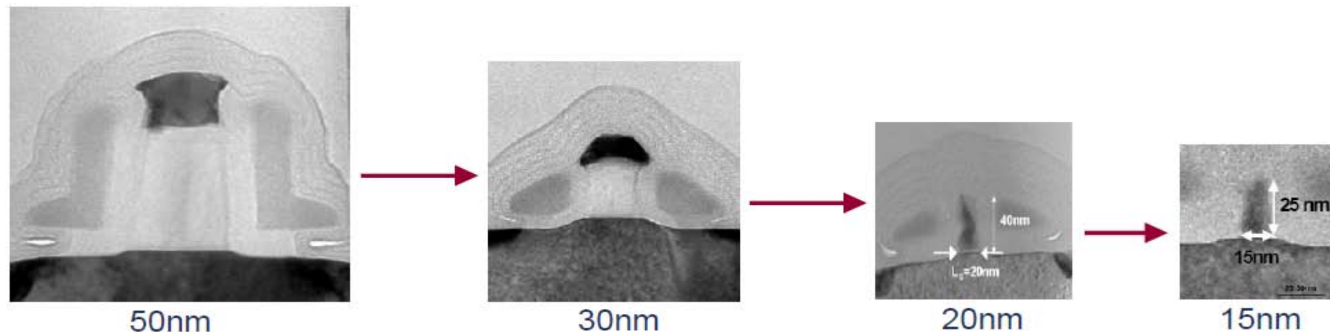




Scaling to atomistic scale devices…

- Nanometer CMOS scaling problems:
  - Noise problems (signal integrity)
  - Leakage (digital)
  - Channel length modulation
  - Velocity saturation
  - Mobility degradation
  - Drain induced barrier lowering (DIBL)
  - Parasitic effects
  - **IC reliability**
  - …





Source: M. Bohr, Intel, IRPS 2003

ITRS Roadmap 2009

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Table PIDS6 Reliability Difficult Challenges

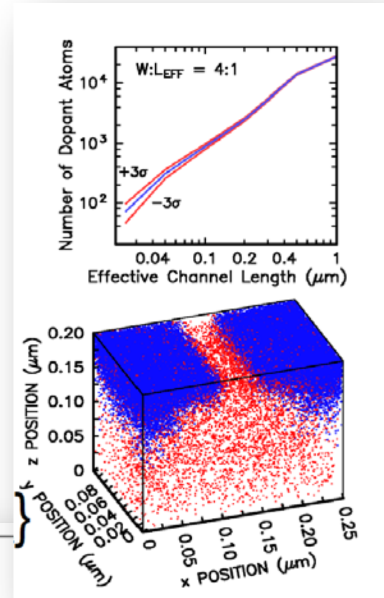
Difficult Challenges ≥ 22 nm	*Summary of Issues*
Transistor Reliability	Time dependent dielectric breakdown Negative bias temperature instability Threshold voltage shifts due to traps, carrier injection, program or erase Mobility degradation due to mechanical stress relaxation or interface state density change New or changed failure mechanisms (TDDB, PBTI, NBTI< moisture absorption, etc.) resulting from high κ/metal gate

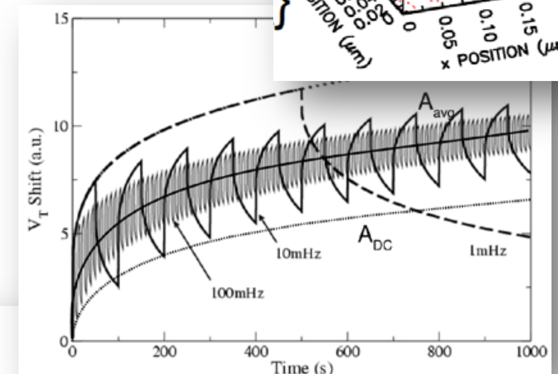
- IC Unreliability
  - Random manufacturing defects
  - Increasing electric field
  - Voltage and temperature variations
  - Signal integrity issues
  - …

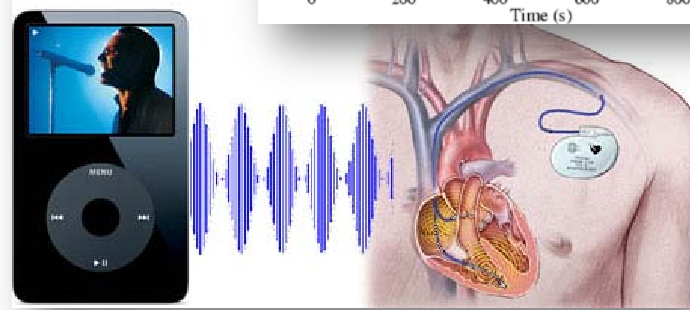
[www.itrs.net]

IC Reliability …

- Spatial Unreliability
  - manufacturing process variations
  - random defects
- Temporal Unreliability
  - ageing effects
- Dynamic Unreliability
  - workload dependent
  - temperature variations
  - EMC

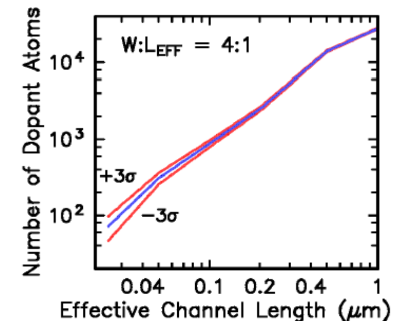


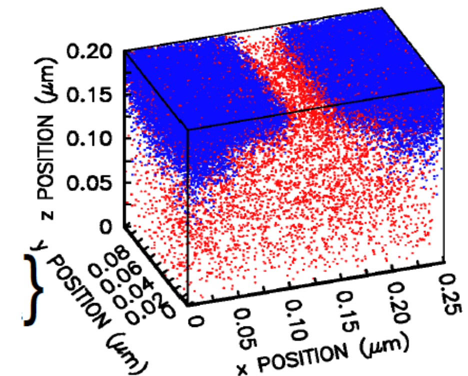


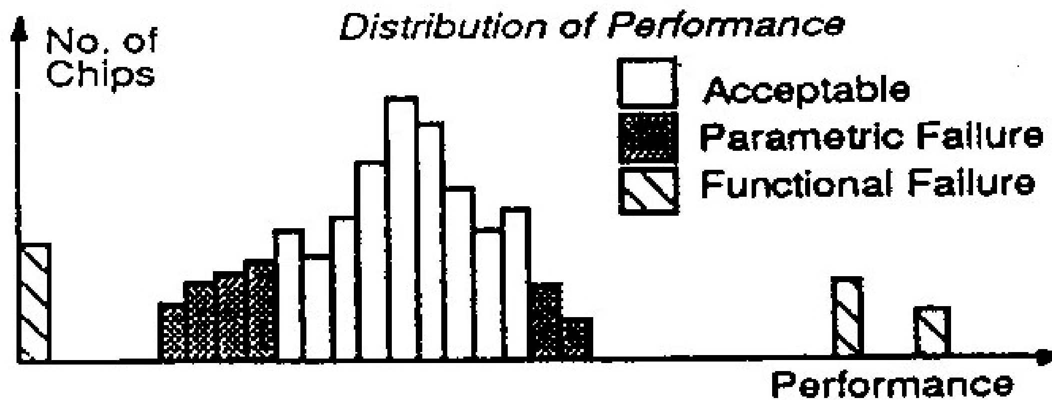


Spatial Unreliability

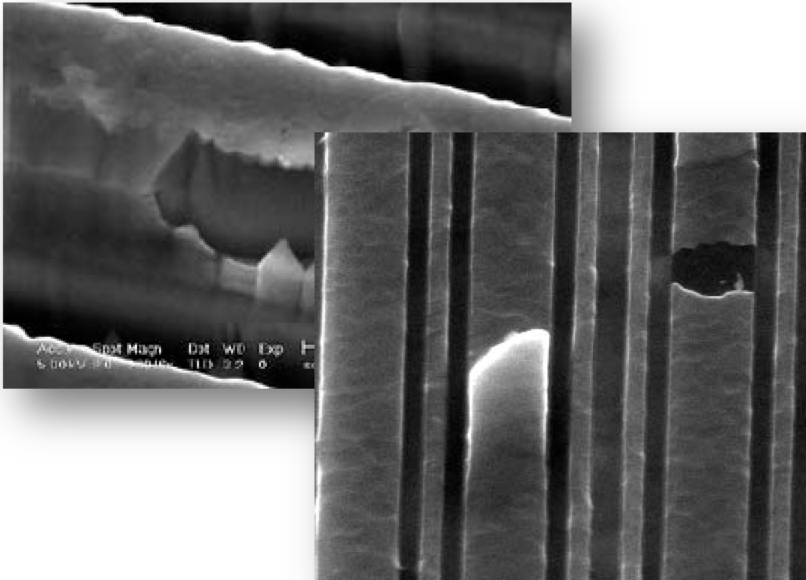
- the IC manufacturing suffers from defects and from inherent fluctuations
  - results in faulty chips and in fluctuations in circuit performances
  - yield smaller than 100% affects profitability of IC manufacturing process

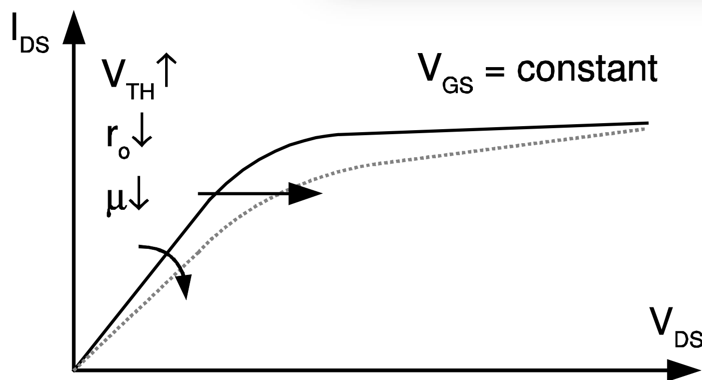






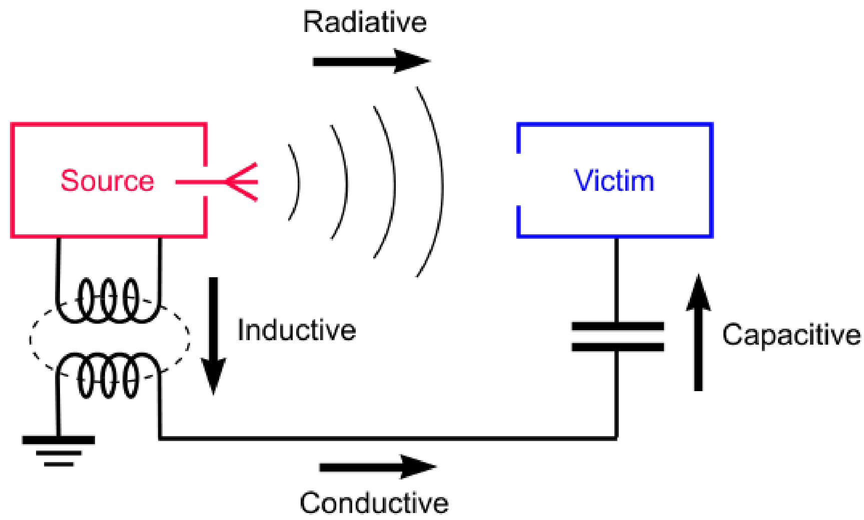
Temporal Unreliability

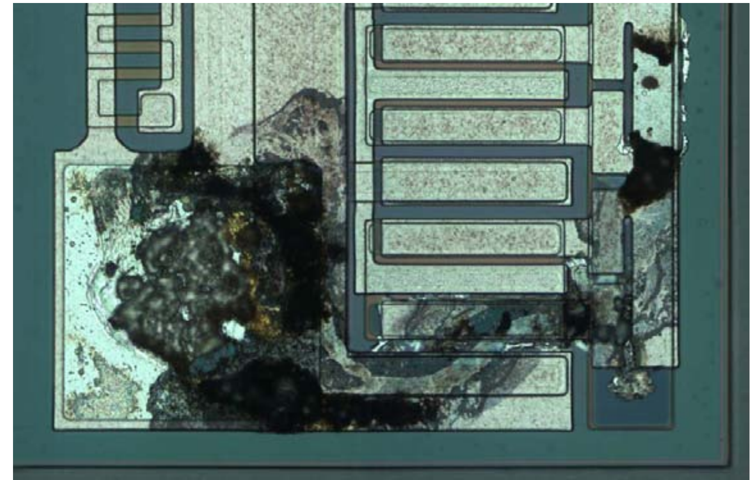


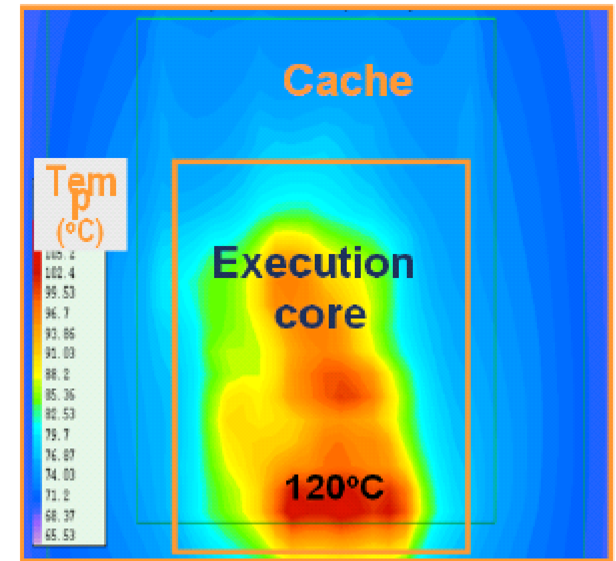


- IC level
  - Electro migration
  - Stress voiding
  - Bias Temperature Instability (BTI)
  - Hot Carrier Injection (HCI)
  - Time Dependent Dielectric Breakdown (TDDB)
  - ...
- PCB
  - Corrosion
  - Solder cracking
  - ...
- Packaging
  - Bond wire sheering
  - ...

Dynamic Unreliability







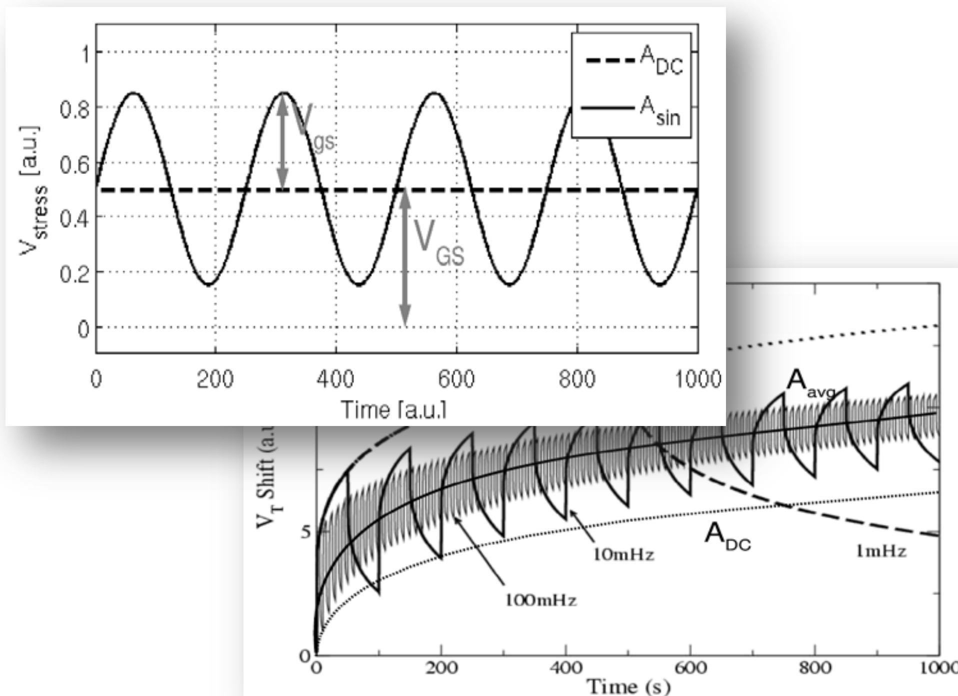
- Power, Voltage, Temperature variations
  - EMC
  - EOS
  - ESD
  - …

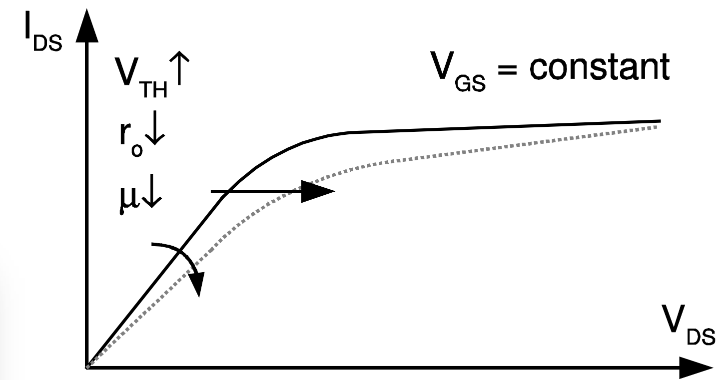
Overview

- IC Reliability: why is this an issue?
- **Capturing the physics**
- Analyzing a circuit
- Case study: SRAM design
- Conclusions

Capturing the physics: deterministic effects

$$D = D_0 + A_x T_{str}^{\eta_x}$$
$$A_x = f(V_{DS}, V_{GS}, V_{TH0}, T, W, L, \ldots)$$





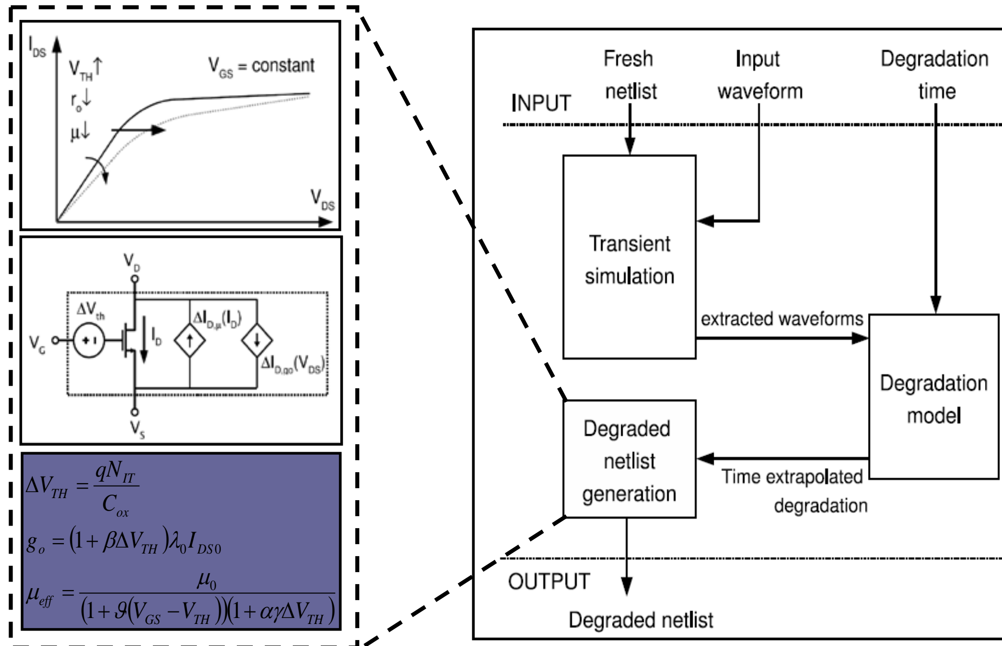
$$D(t) = \left[\int_0^t (A_x(t))^{1/n_x} dt\right]^{n_x}$$

[Maricau ESREF08, IOLTS 09]

Overview

- IC Reliability: why is this an issue?
- Capturing the physics
- **Circuit reliability analysis**
- Case study: SRAM design
- Conclusions

Nominal Reliability Simulation



- IC Analysis: Performance(t)?
- Time-varying stress (Analog!)
- Gradual OP shift

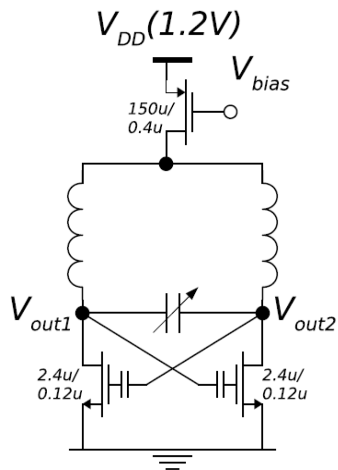
[Maricau DRV 08]

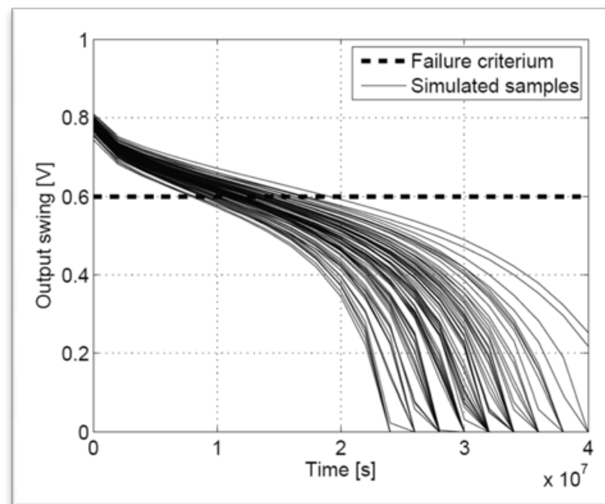
Variability-awareness?

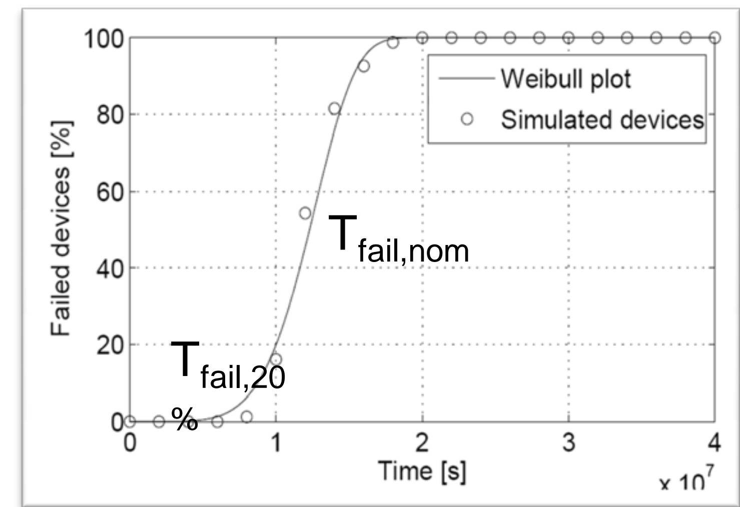
- Process variability introduces stress variability
- Transistor aging + process variability = yield(t)

$$\sigma(V_{TH}) = (1 - \alpha\Delta V_{TH})\sigma(V_{TH0})$$

$$\sigma(\mu) = \frac{\sigma(\Delta V_{TH})\beta\mu 0}{(1 + \beta\Delta V_{TH})^2}$$

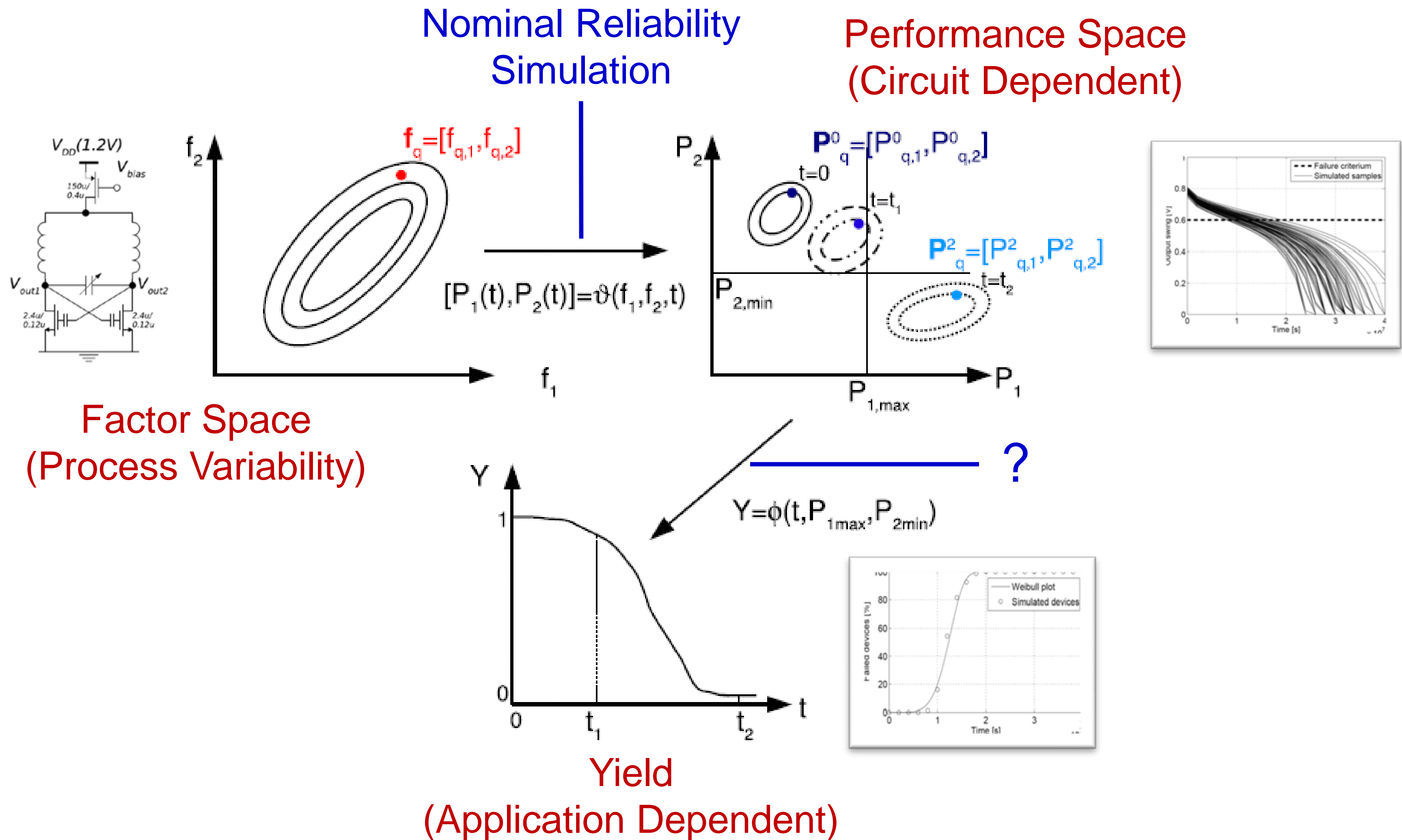






[Maricau DATE 09]

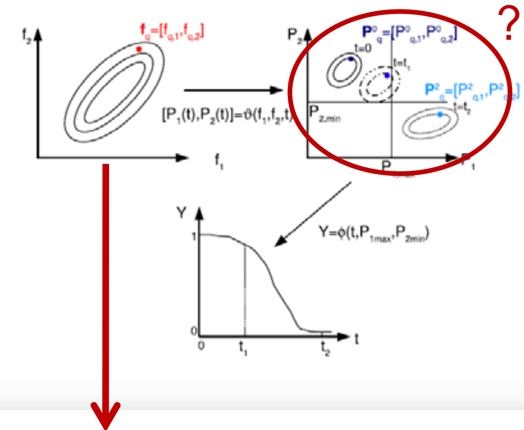
Variability-aware Reliability Simulation

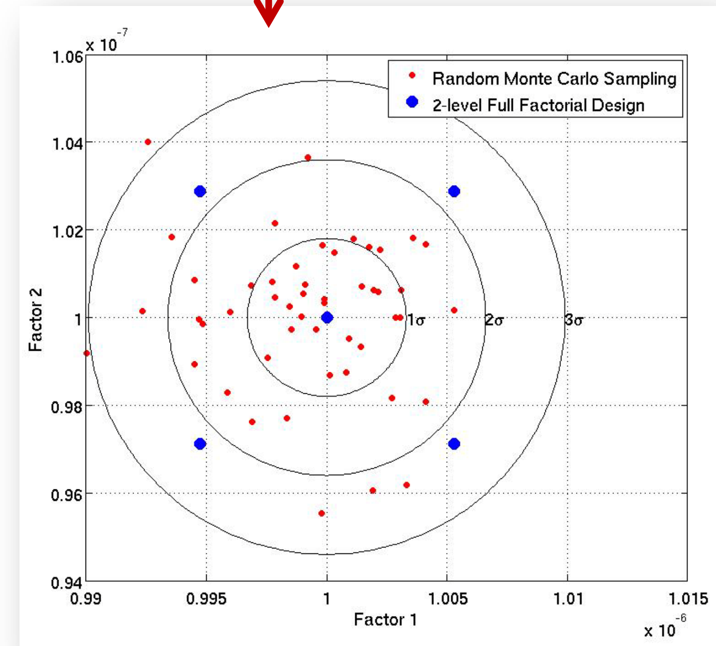


Performance Space Exploration

- Option 1: Monte-Carlo
  - Monte-Carlo loop around nominal reliability simulation
  - Chi-square goodness-of-fit to find a good PDF at every time-point
  - Accurate but very slow

- Option 2: Design of experiments + RSM
  - Goal: faster while maintaining accuracy
  - Means
    - Make every sample count!
    - Monte-Carlo on RSM





Variability-aware Reliability Simulation

- Factor Space Exploration
  - Screening
    - Linear model
    - Detect interactions
  - Regression
    - Interactions
    - Weak non-linear effects

- Polynomial RSM

$$\hat{\vartheta}'^{i}_{j} = a_0 + \sum_{k=1}^{n} a_k f'_k + \sum_{k=1}^{l-1} \sum_{l=2}^{n} a_{kl} f'_k f'_l + \sum_{k=1}^{n} a_{k,2} {f'_k}^2$$

- Residual analysis
  - Error estimation

[Maricau DATE 10]

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- IC Reliability: why is this an issue?
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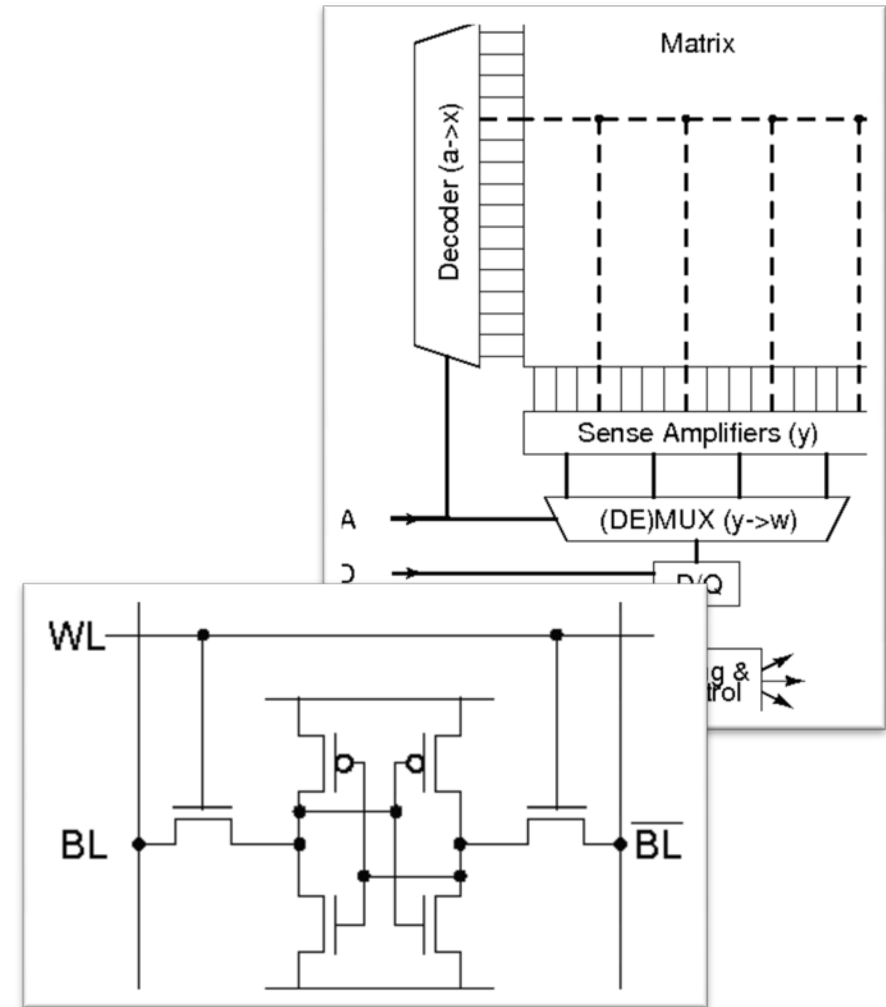
- Conclusions

Spatial reliability hazards in a 6T SRAM cell

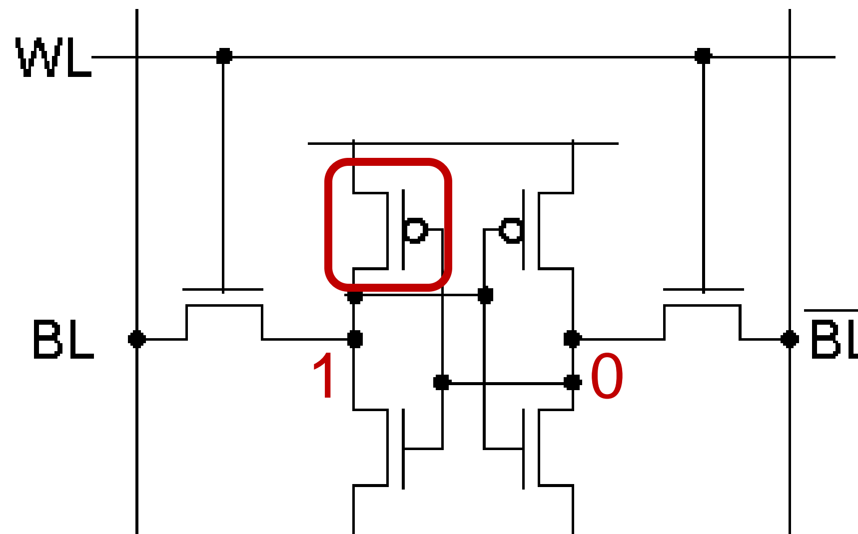
- It is (was?) all about area, but…
  - Minimal transistors
    - Lots of variation
  - Large cell matrices
    - Big bit line load
  - Lots of cells
    - Distribution tail cells are used

- Process variability is the most important design issue for memory cells



Temporal reliability hazards in a 6T SRAM cell [I]

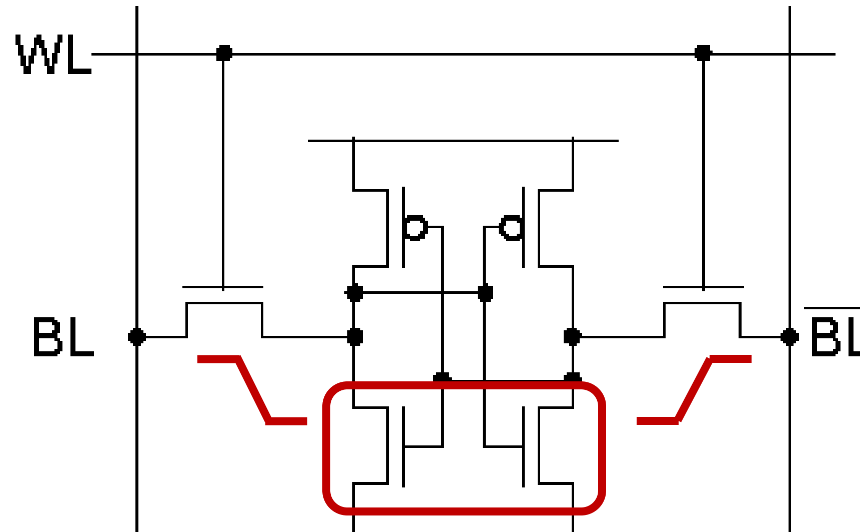
- Negative Bias Temperature Instability



  - V_{TH} shift
  - PMOS becomes slower
  - Increasing asymmetry under asymmetric stress
  - Partial recovery under time-varying stress

Temporal reliability hazards in a 6T SRAM cell [II]

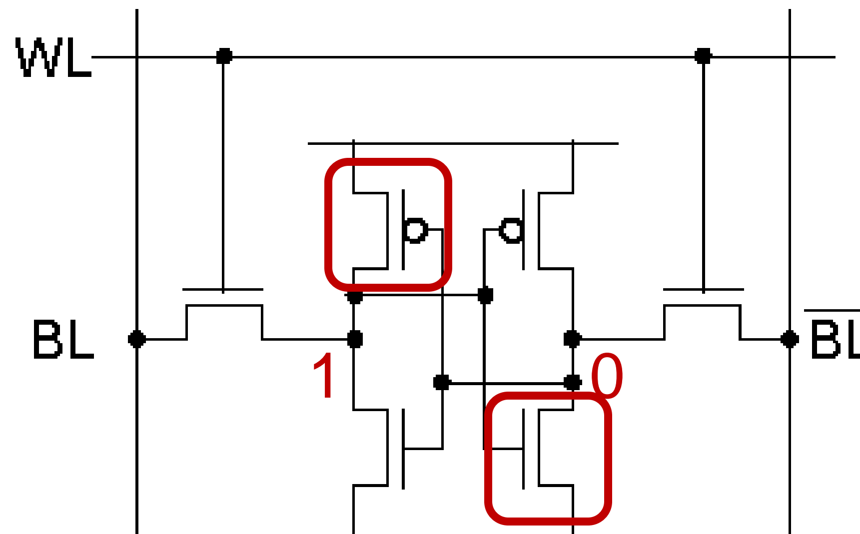
- Hot Carrier Injection



  - V_{TH} shift
  - NMOS becomes slower

Temporal reliability hazards in a 6T SRAM cell [III]

- Soft Breakdown

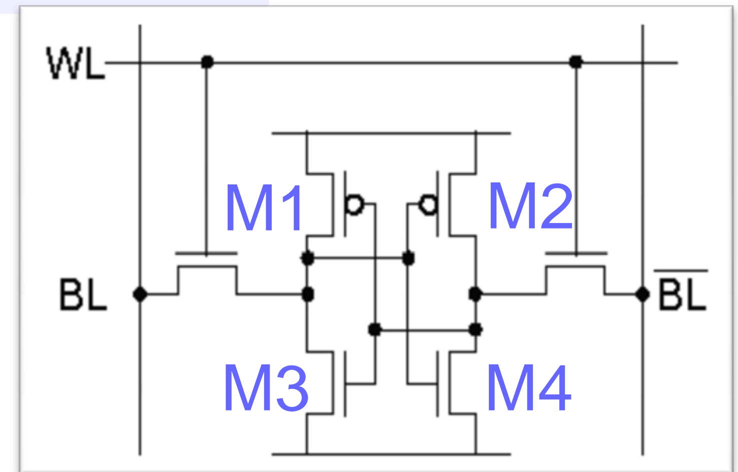


  - Decreasing gate resistance (to drain and source)
  - Increasing asymmetry under asymmetric stress

Temporal reliability hazards in a 6T SRAM cell [IV]

VDD	M1	M2	M3	M4
1.0V	$\lvert\Delta V_{TH}\rvert$=70mV			
1.1V	$\lvert\Delta V_{TH}\rvert$=88mV #SBD=4			#SBD=4
1.3V	$\lvert\Delta V_{TH}\rvert$=120mV #SBD=40		$\lvert\Delta V_{TH}\rvert$=5mV	#SBD=40
1.5V	$\lvert\Delta V_{TH}\rvert$=180mV #SBD=50+		$\lvert\Delta V_{TH}\rvert$=20mV	#SBD=50+

- 3 year constant voltage stress
- predictive 32nm CMOS



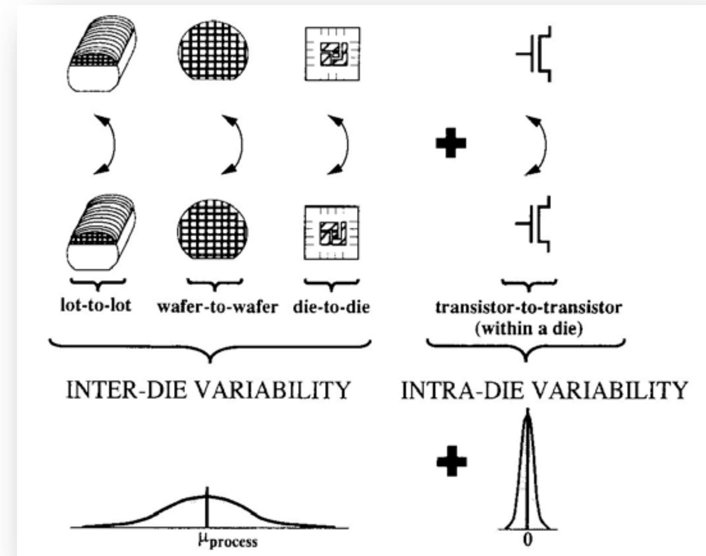
Temporal reliability hazards in a 6T SRAM cell [V]

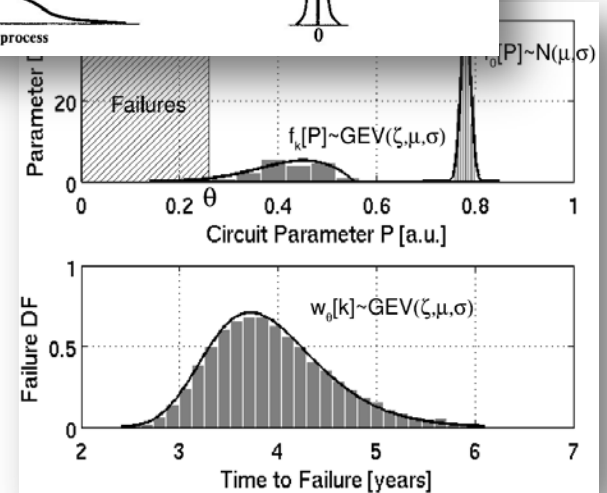
- Negative Bias Temperature Instability
  - SNM ↓
- Hot Carrier Injection
  - SNM ↓
  - Read speed ↓
- Soft Breakdown
  - Cell leakage ↑

WL
BL
$\overline{BL}$

Solutions

- Inter die variability
  - Tuning, margins
  - Performance differences between dies
- Intra die variability
  - Circuit techniques
- Time dependent degradation
  - Knobs and monitors (self-healing)
  - Robust design

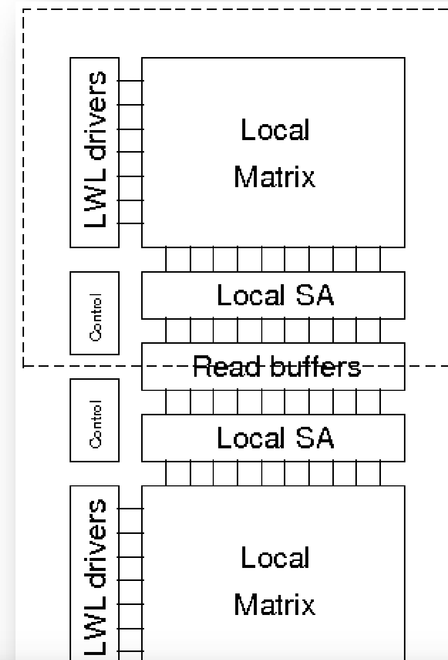


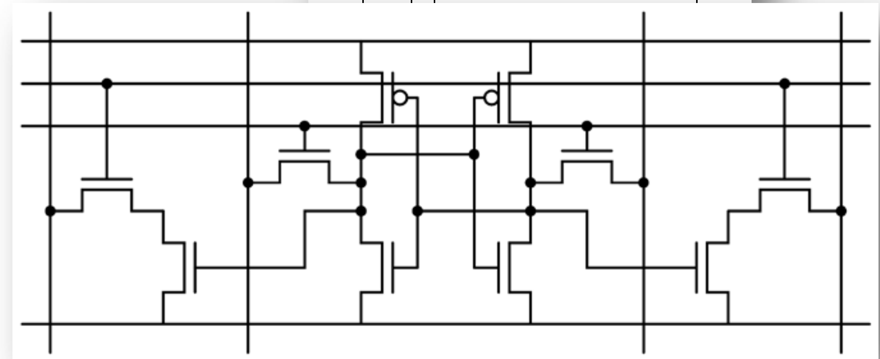


➡ This is not for free!

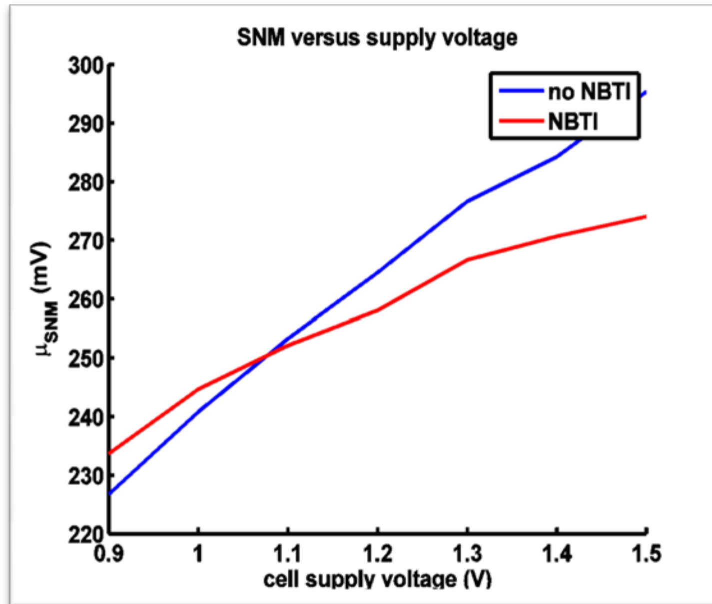
Some circuit techniques…

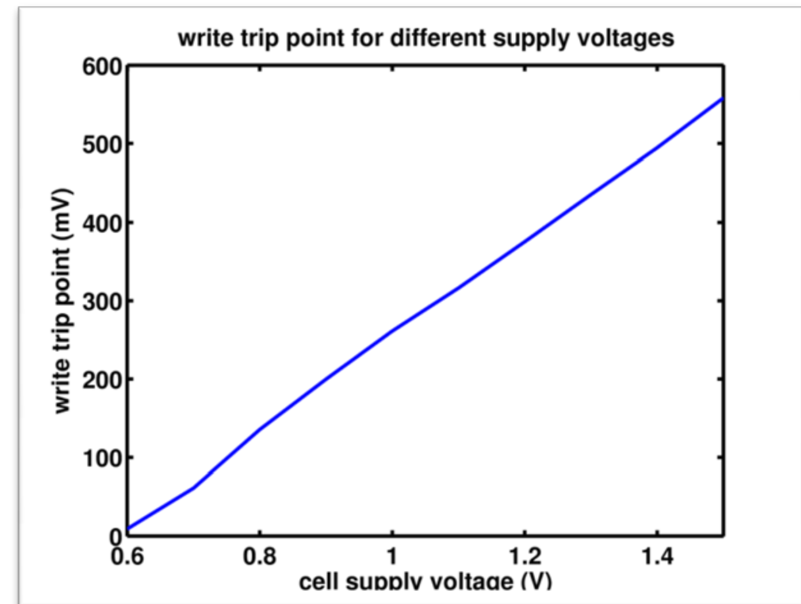
- Size up transistors
  - Limited result
  - Power, area
- VDD↑
  - Leakage, extra supply
  - Reliability issues
- HVT cells
  - Read speed
  - Writeability
- Alternative cell designs
  - (much) more area
- Local periphery
  - Area
  - Design complexity





Increase supply voltage

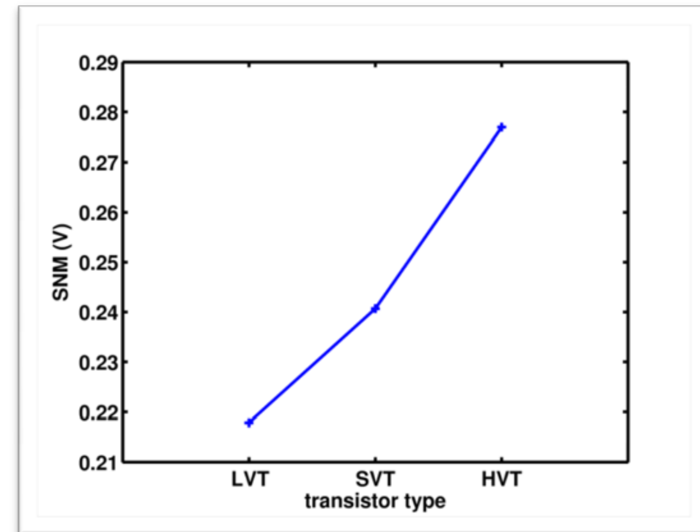


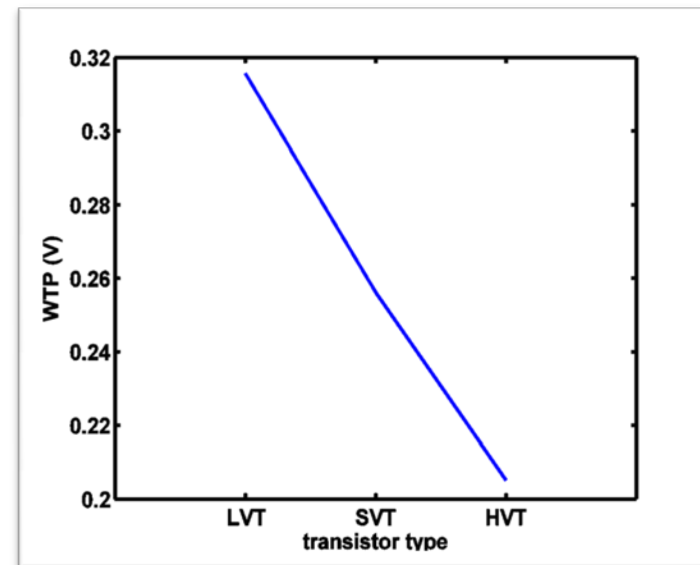


- Write ability improves
- Leakage ↑
- NBTI effect ↑

High VT cells

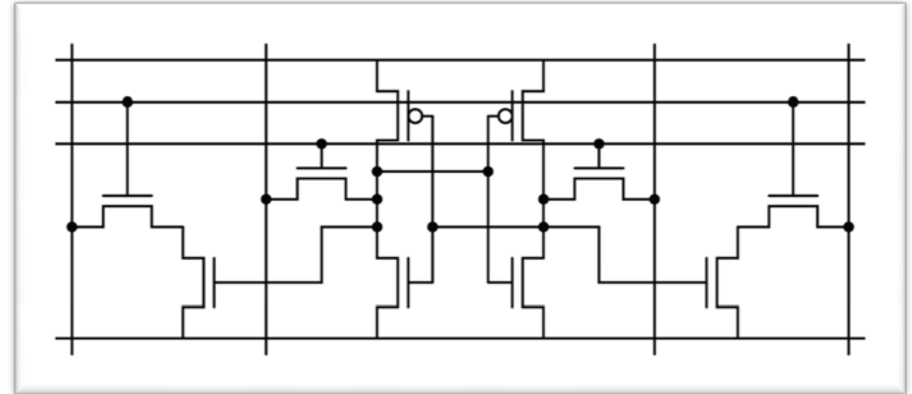
- Higher SNM
- Writeability is an issue
- Read speed
- Often there is a conflict between stability and writeability

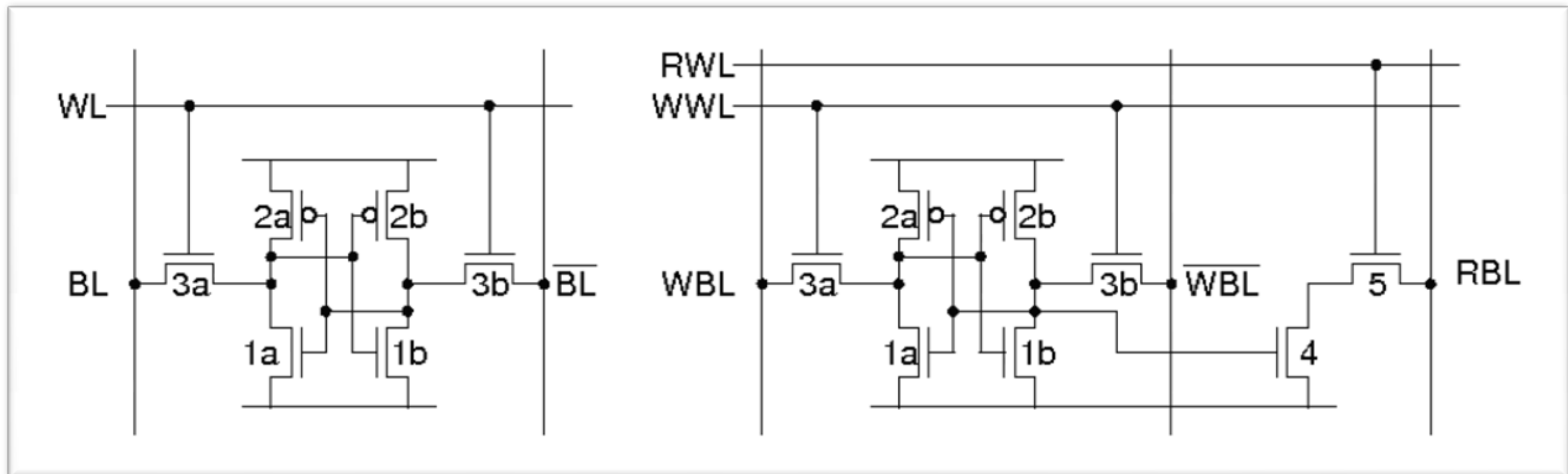




Alternative cell designs

- < 6T cell
  - Worse
- 6T cell
  - As long as possible
- > 6T cell
  - Area ↑



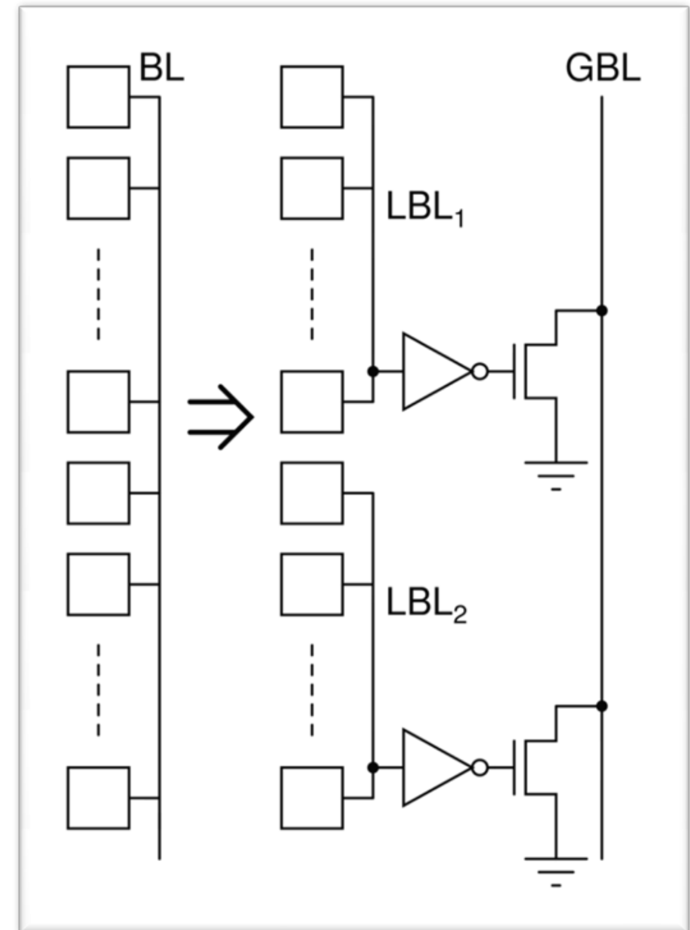


Local periphery

- Local bit lines
  - # cells/bit line = 16, 32, 64, …
  - Impact of cell ↓
  - Variability
    - Read speed

$$\tau_{6\sigma} = \frac{C_{BL}}{I_{cell,6\sigma}}$$

    - Dynamic stability
  - Power ↓
  - SA less critical
  - Merges with other low power tricks
  - More area



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Conclusions

- Spatial and temporal reliability are an issue in nanometer CMOS IC designs
- Accurate modeling and efficient CAD tools are needed to assist the designer
  - Design for reliability
  - Increase design margins
- Solutions are needed at different levels of integration
  - Device level (e.g. LDD to reduce HC effects)
  - Circuit level (e.g. HVT, Local bitlines, 10T cells, …)
  - System level