

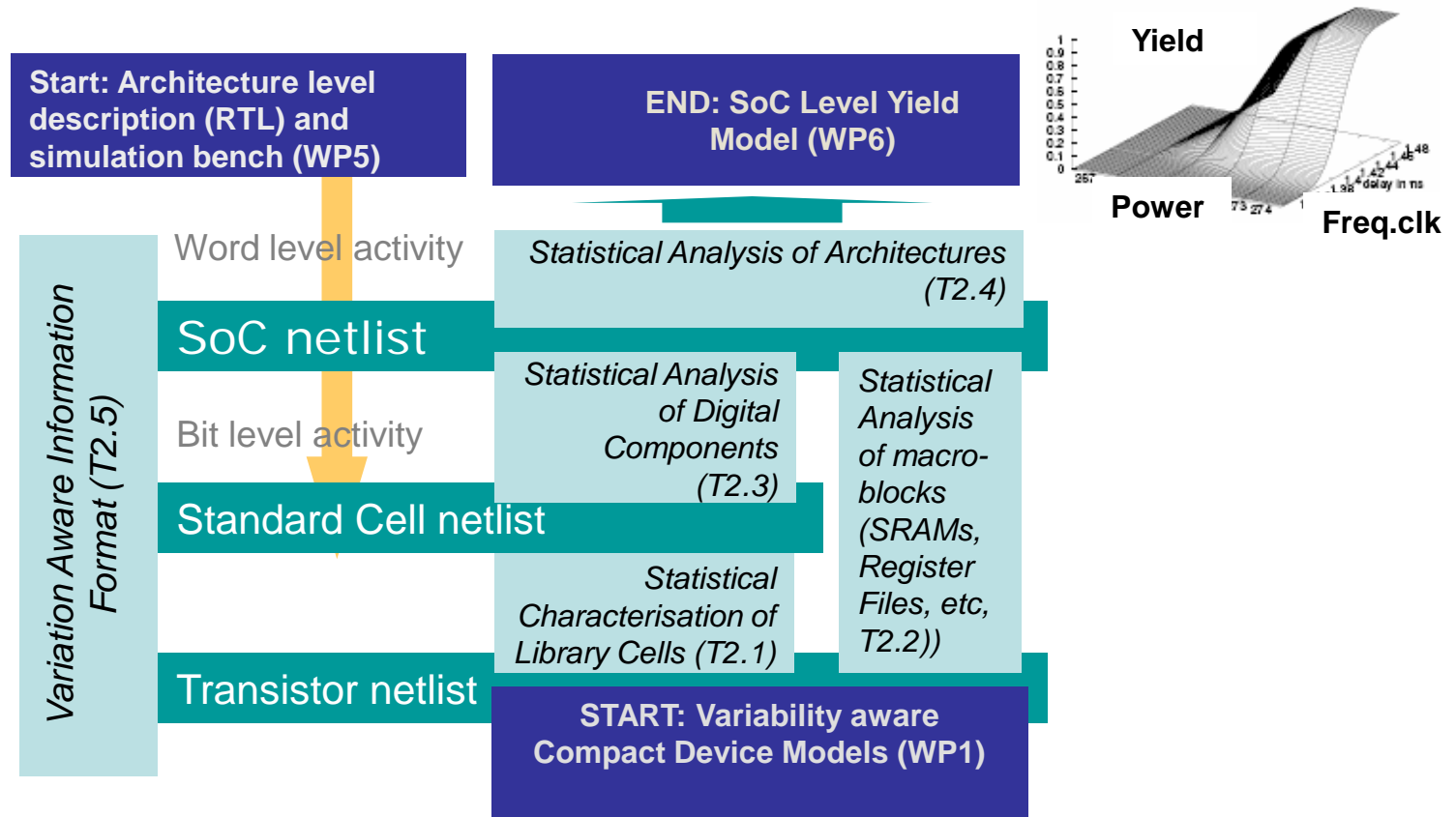
REALITY

REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Project Workshop - Work Package 2 System and circuit characterisation and sensitivity analysis



WP2 Goal - Holistic Variability Aware SoC Modeling



Effort done, planned, remaining

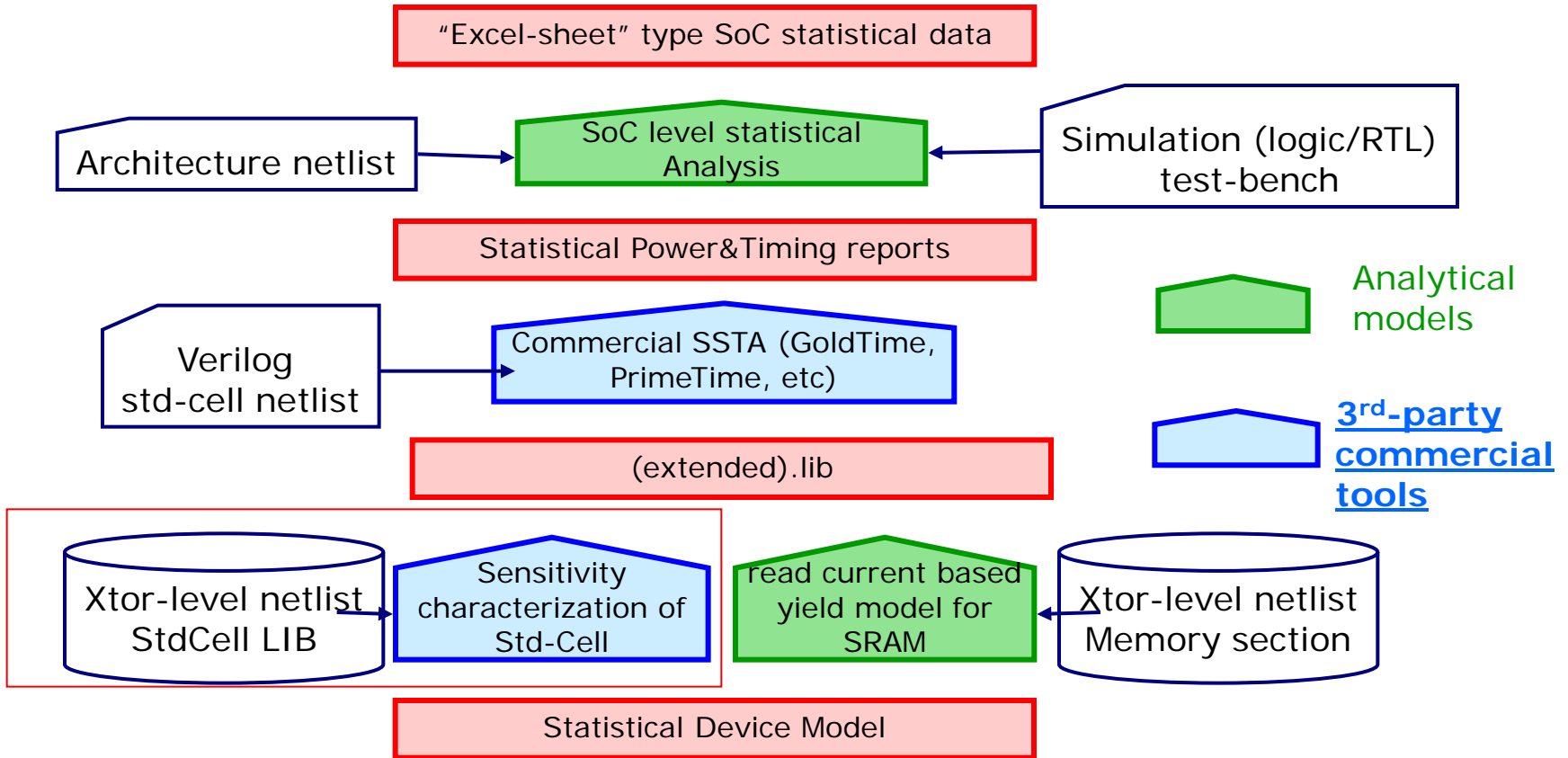
Partner	Total Effort (MM)	Y1 Effort (MM)	Planned Y2 Effort (MM)	Actual Y2 Effort (MM)	Remaining Effort till T0+27M (MM)
UoG	3	1.5	1.5	1.5	0
IMEC	24	10.8	10.8	10.8	2.4
UNIBO	0	0	0	0	0
ST	30	15	15	15	5
KUL	3	0	3	1	2
ARM	18	8	10	10	0
Total	78	30.3	40.3	38.3	9.4

Workpackage Closed

Tasks

- **Task 2.1: Development and characterization of a standard cell library under variability impact**
 - T2.1.1: Design of a limited standard cell library in 32 nm
 - T2.1.2: Statistical Characterization of Standard Cell Libraries
- Task 2.2: Statistical Characterization of Macro-Blocks
- Task 2.3: Statistical Analysis of Digital Blocks
- Task 2.4: Statistical Analysis of SoC Architectures
- Task 2.5: Variation Aware Information Format

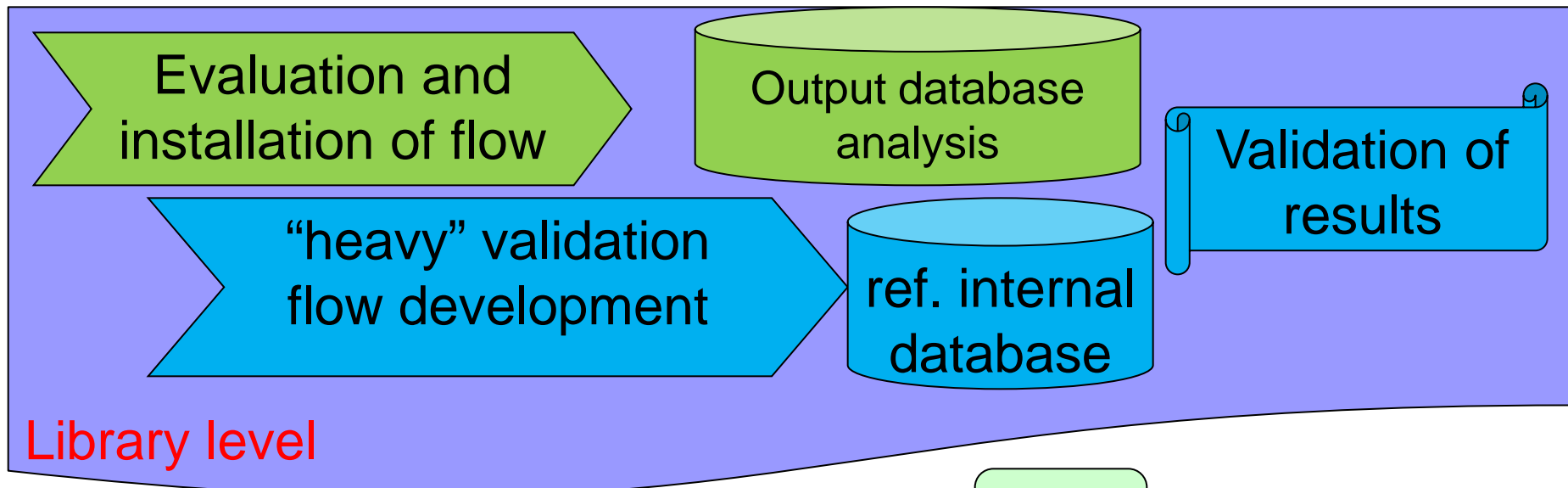
Task 2.1 Context



Statistical Analysis Flow from device to SoC level

Task 2.1.2 Statistical Characterization of Standard Cell Library

- Statistical library characterization using VAM and Magma SiliconSmart SSTA
- Validation with “Heavy” validation flow
- Debug of Magma tools to show good dispersion information

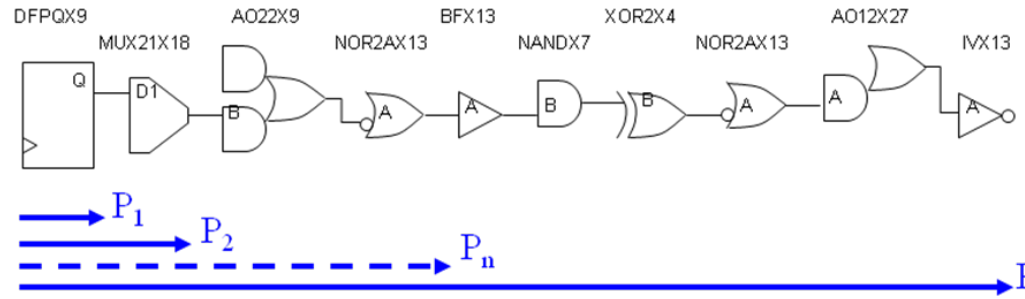


Task 2.1.2 Statistical Characterization of Standard Cell Library

Based on:

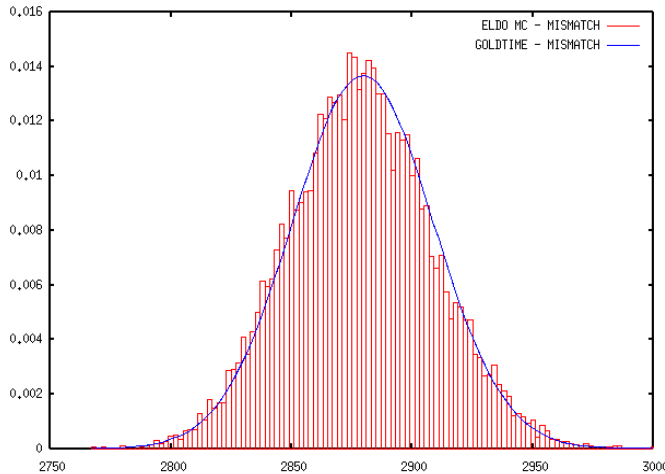
- 1) identification of transistors impacting the cell performances
- 2) reduction of the characterization grid size
- 3) identification of a restricted set of transistor parameters that mostly impact on the device performances

Timing path in CMOS065LP technology



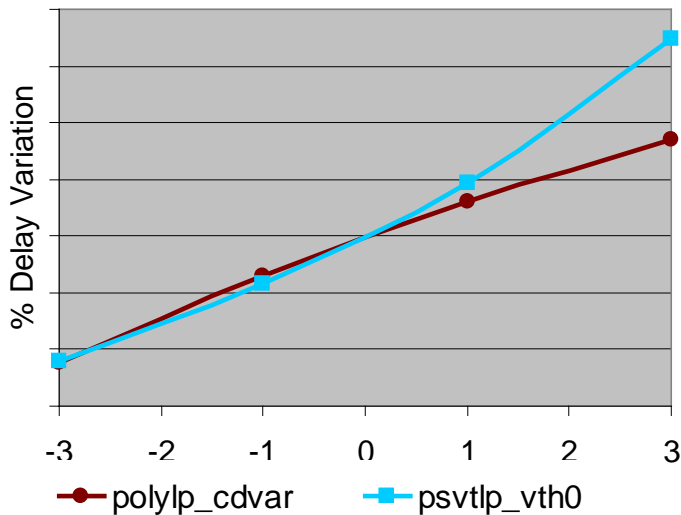
Device mismatch impact on path delay

SSTA vs. Monte Carlo



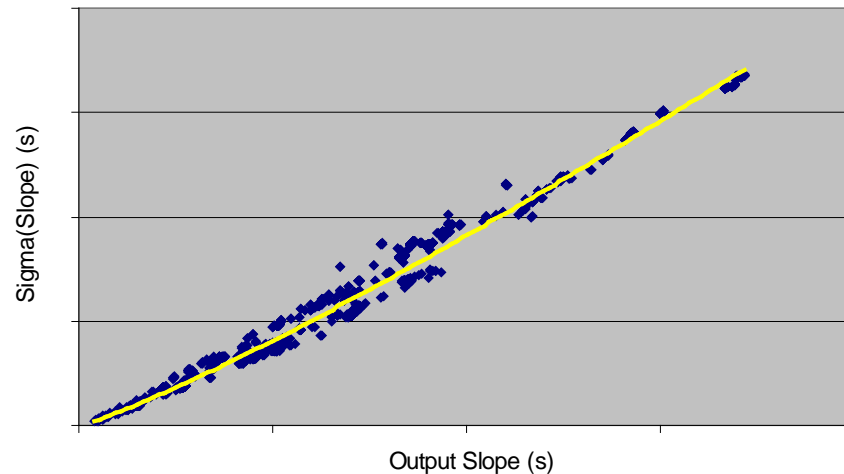
Excellent correlation

Task 2.1.2 Statistical Characterization of Standard Cell Library

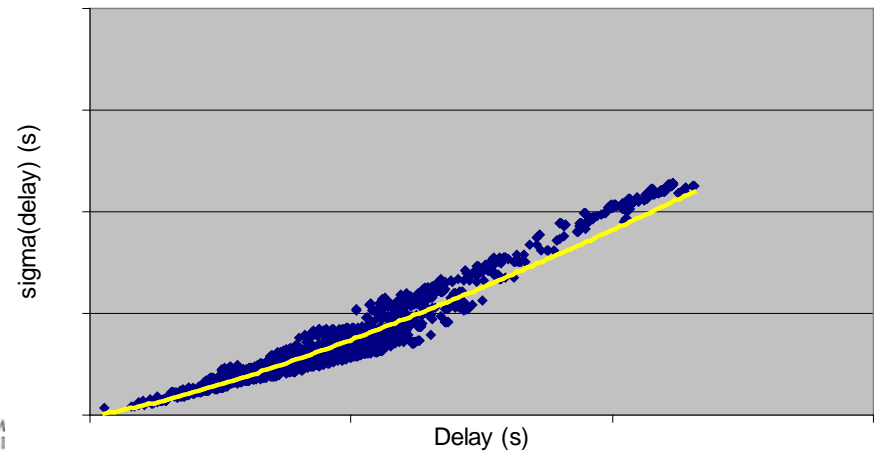


- Non-linear dependence of cell delay on process variations
- Poly CD and threshold voltage: more significant in PMOS devices
- Poly CD non-linearity was known in CMOS065LP but threshold voltage was observed in CMOS045LP
 - likely due to large deviations coupled with low voltage and temperature

Sigma vs Output Slope



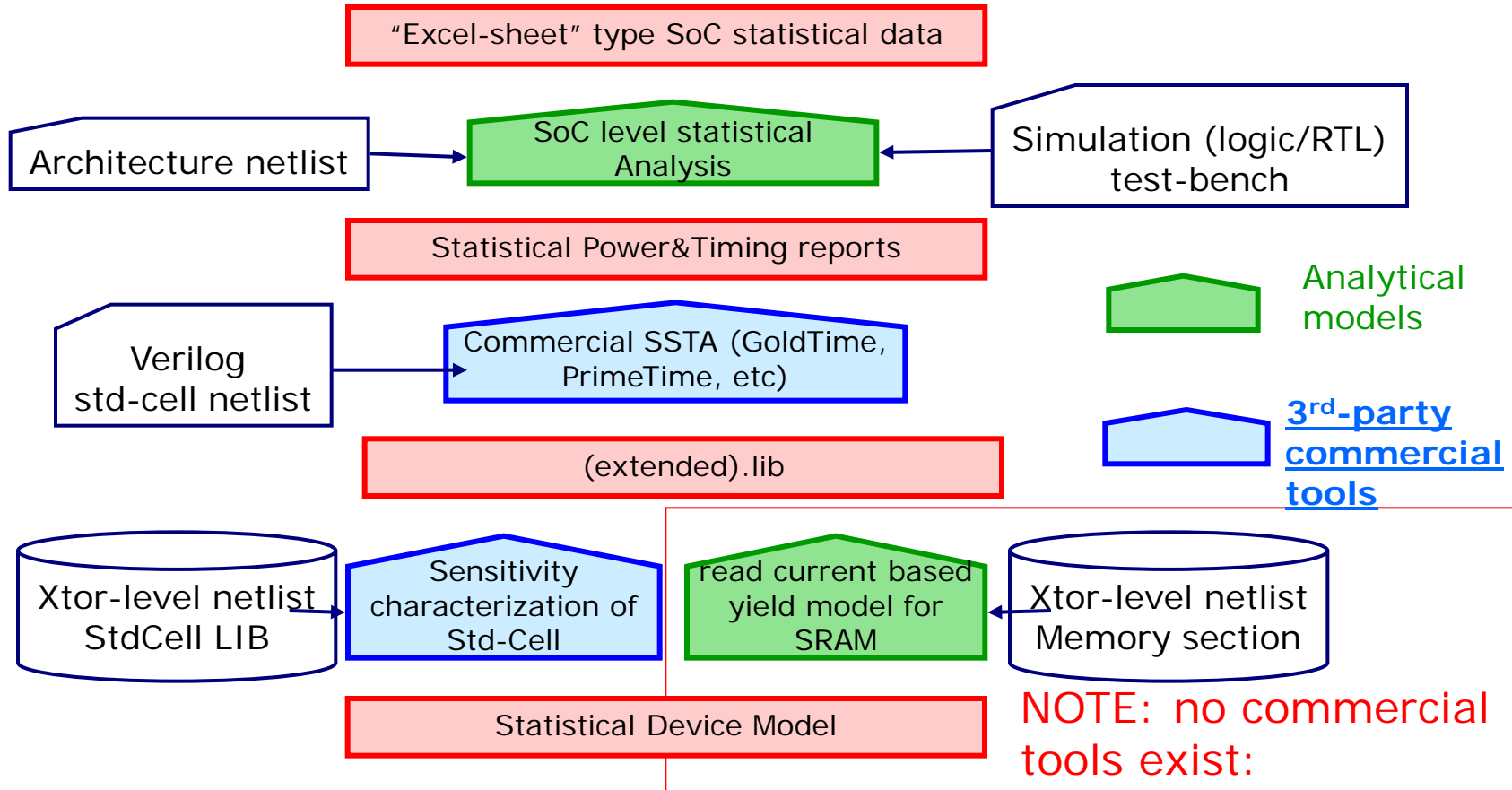
Sigma vs Delay



Tasks

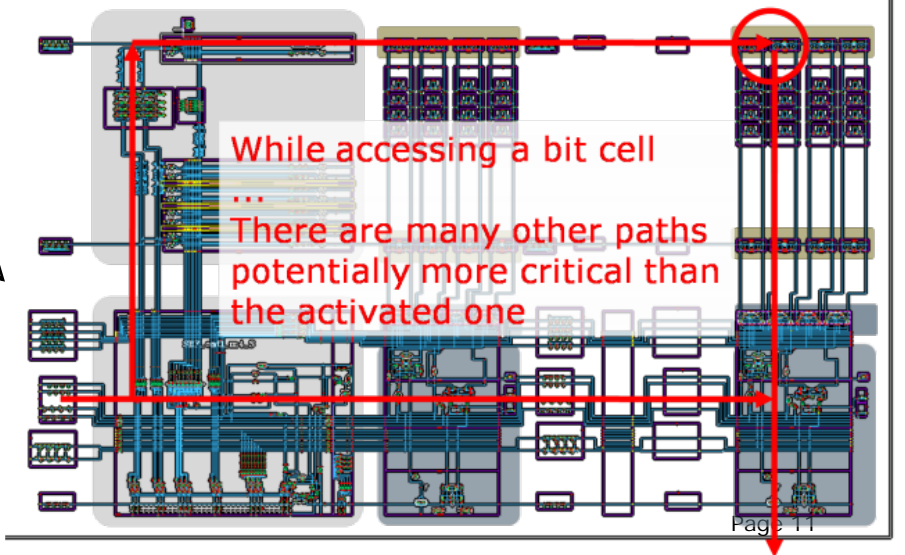
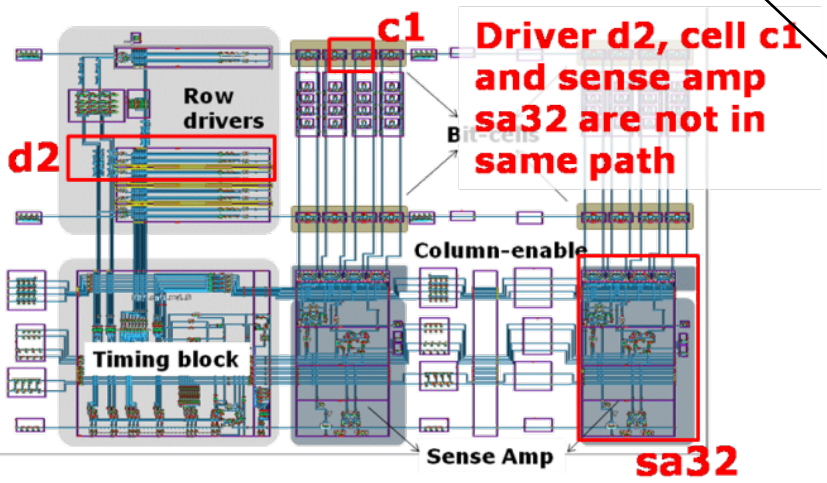
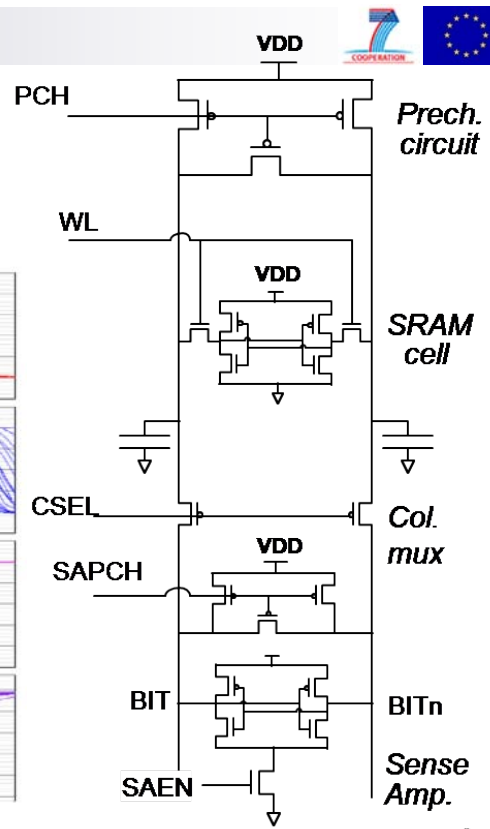
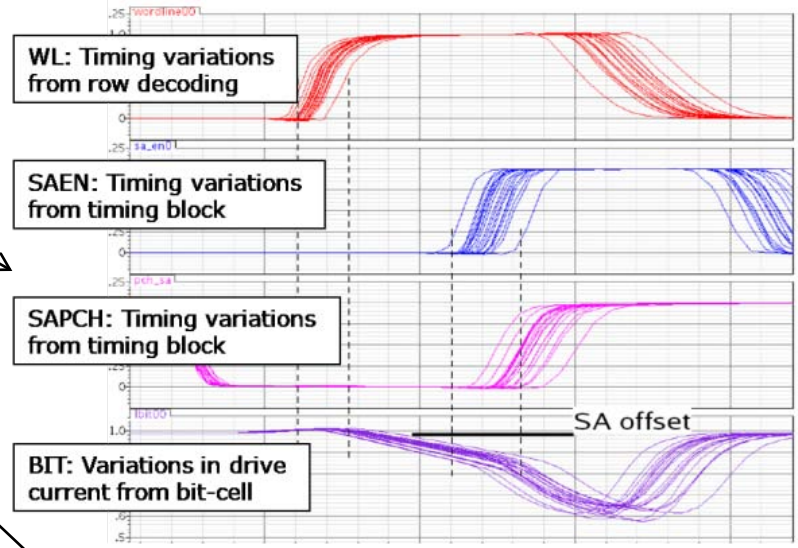
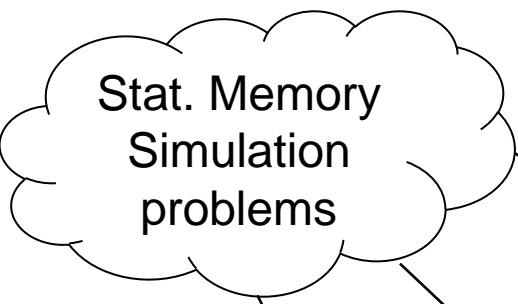
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- **Task 2.2: Statistical Characterization of Macro-Blocks**
- Task 2.3: Statistical Analysis of Digital Blocks
- Task 2.4: Statistical Analysis of SoC Architectures
- Task 2.5: Variation Aware Information Format

Task 2.2 Context



Statistical Analysis Flow from device to SoC level

Task 2.2 Context: Why are macroblocks more difficult than standard cells



Task 2.2 Context: State of the art

- No complete commercial solutions exist.
- Only two methods address all Interactions, PDF shift and topology.
- Both methods are based on a:
 - Phase I: Commercial simulator calibration
 - Phase II: Correcting statistics for Interactions, PDF shift, Topology
- REALITY partners ARM and KUL chose ARM- and imec-methods, respectively.

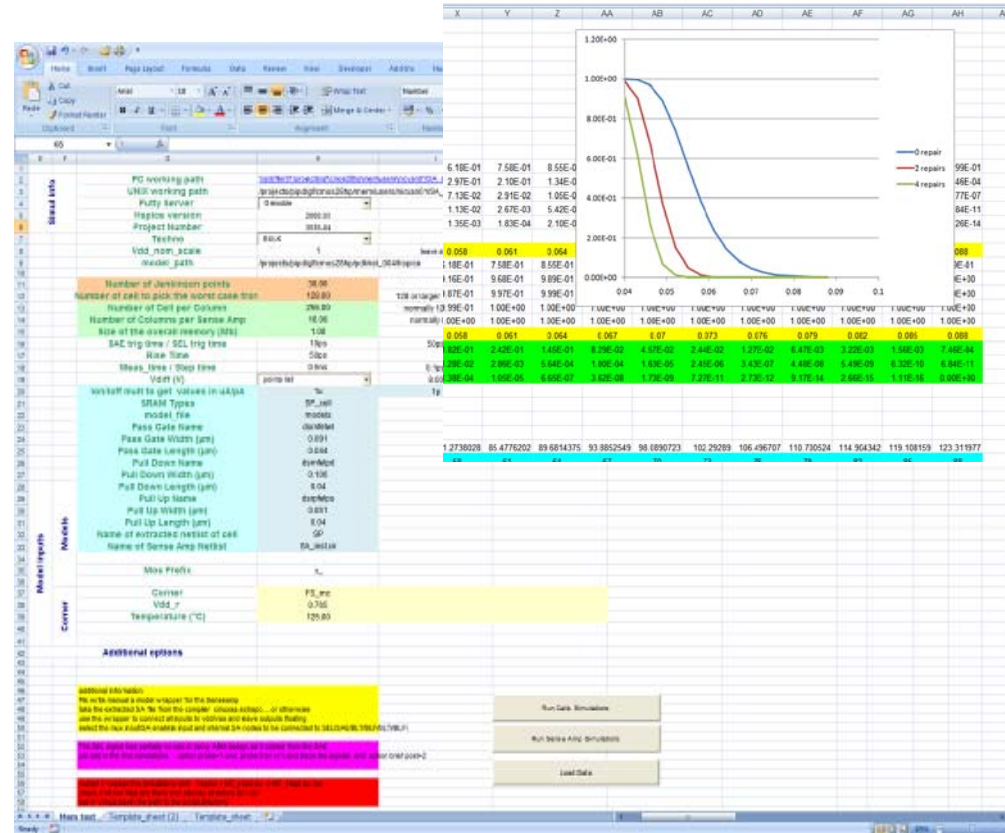
Author	Proceedings	Interactions	Approach	PDF shift	Topology
U Purdue	TCAD2005	Cell	Analytic	NO	limited
IBM-1	DAC2006	Cell	Empiric	NO	NO
U Virginia / Carnegie-1	ESSCIRC2007				
IBM-2	DAC2006	Cell	Analytic	NO	NO
PDF Sol. / Carnegie-2	DAC2009	Cell	Combined	NO	NO
Intel	SPIE2008				
ARM	DATE2007	Cell, Sense Amp	Combined	YES	YES
imec	DATE2010 / DAC2010	all	Combined	YES	YES

Task 2.2: Statistical Characterization of Macro-Blocks

- KUL-Memory preparation for MVAM
 - Slicing netlist to avoid computational overhead
 - Writing testbenches
 - Setup/hold time
 - Memory delay
 - Memory energy
 - Generating island definitions
- Further details, cf. WP3, WP5, WP6

Task 2.2: Statistical Characterization of Macro-Blocks

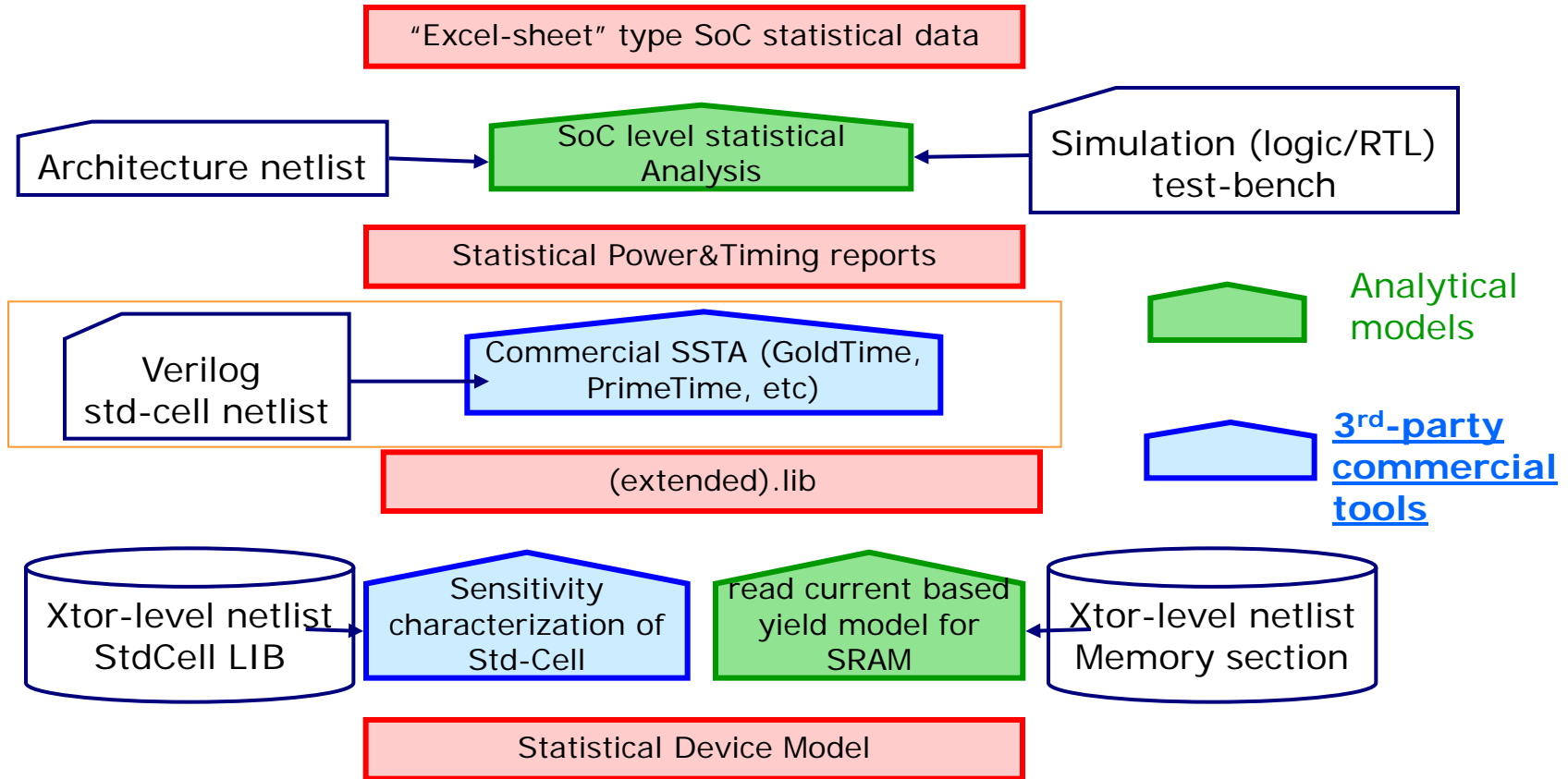
- Read margin using Extreme Value Theory:
 - Validation of the flow
 - Integration in a XL based “easy to use” tool
- Adaptation of analysis to write margin
 - Static read margin analysed using similar principles
 - New dynamic read margin analysis developed



Tasks

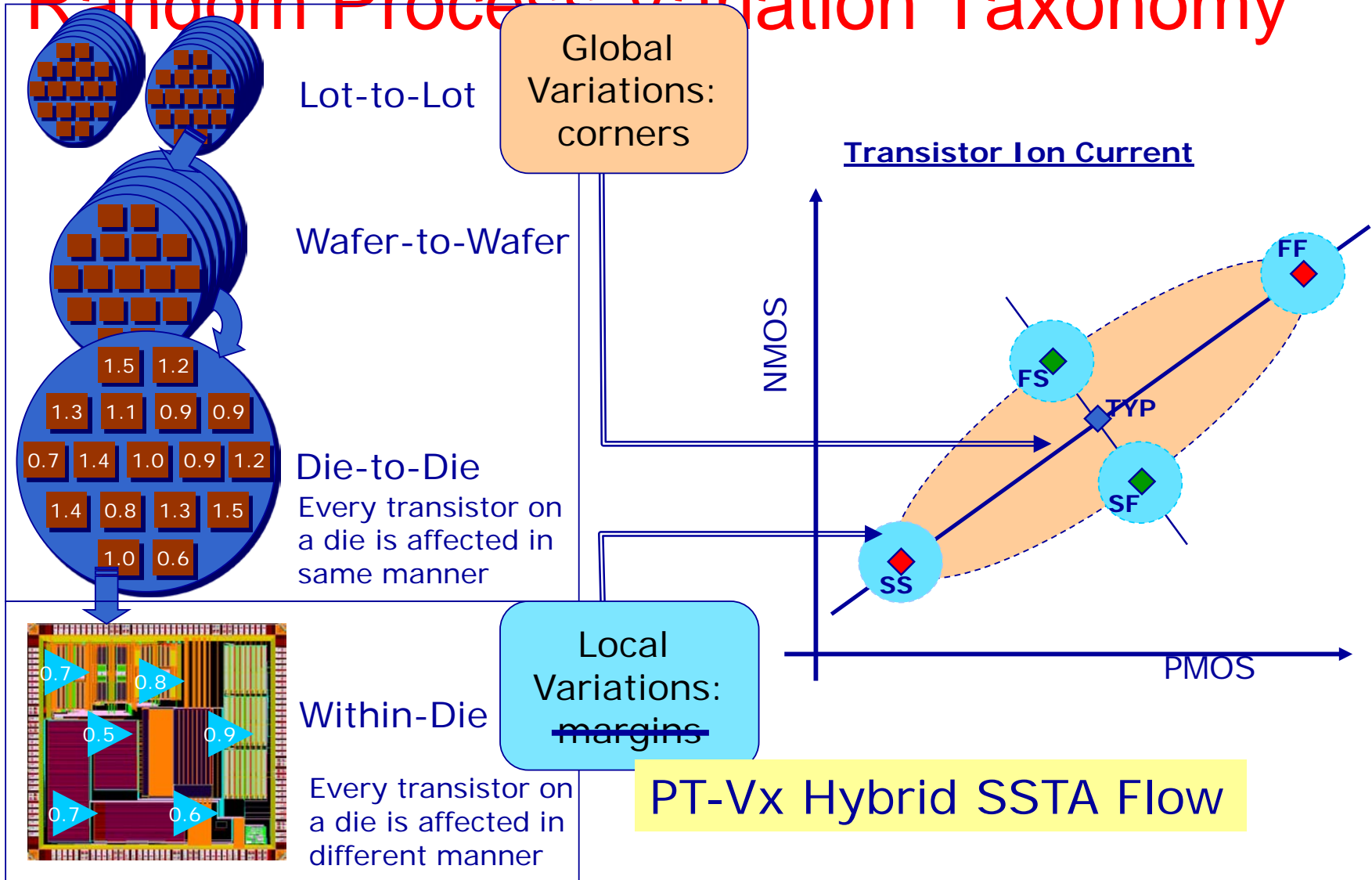
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Task 2.3 Context

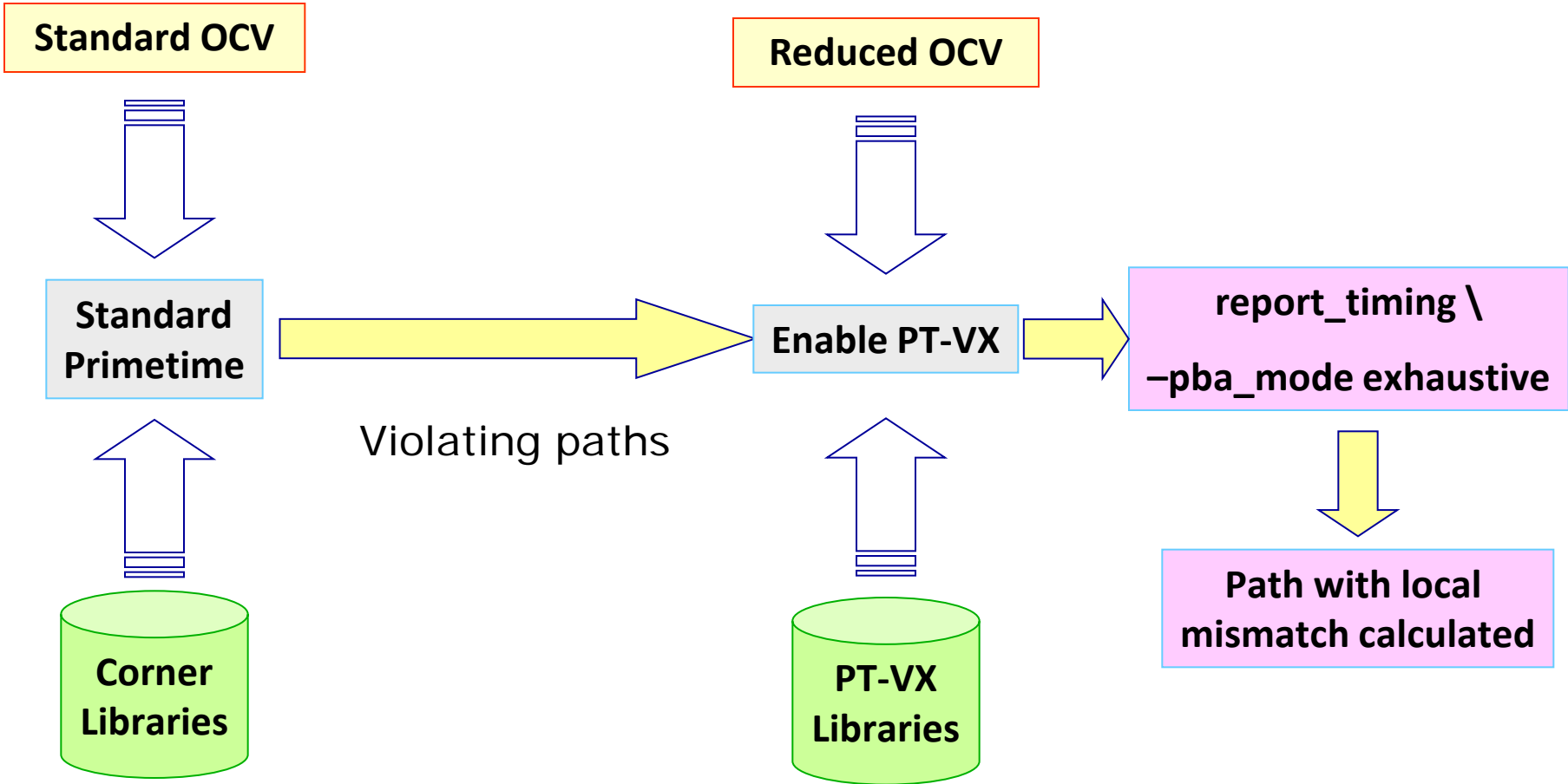


Statistical Analysis Flow from device to SoC level

Random Process Variation Taxonomy

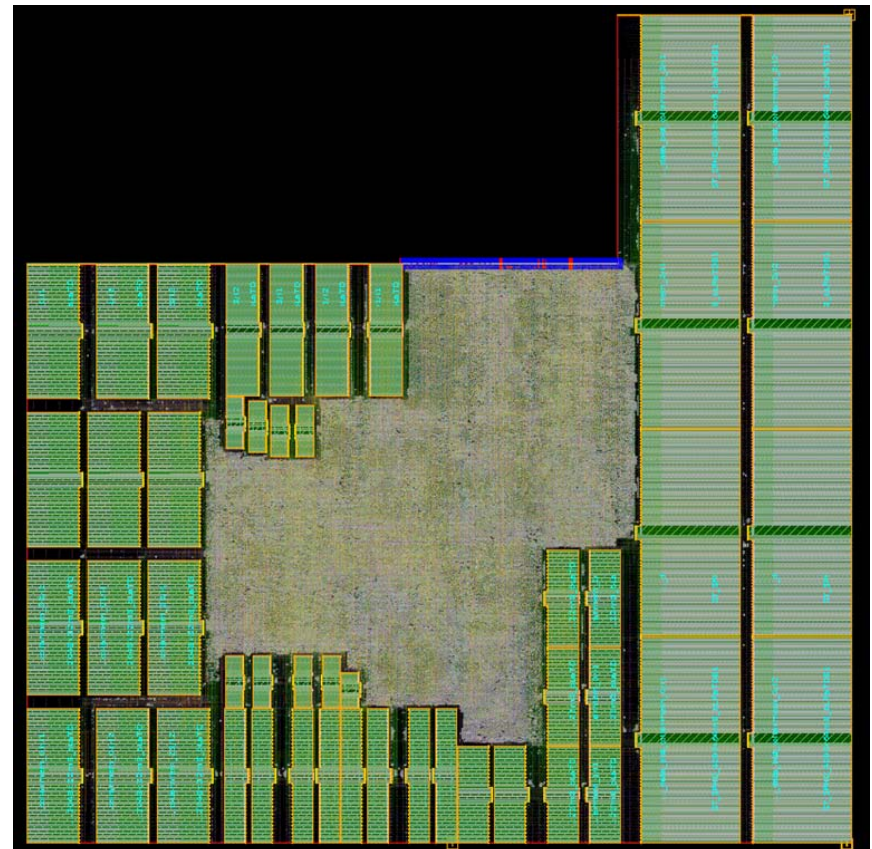


SSTA Hybrid Flow Concept



SSTA Hybrid Flow Exploitation

- ST digital test case in CMOS045LP: R4 core
- 200K-net design
- Main clock period (CLK): 2.2ns
- Highly tuned DB for speed and power
 - Representative of CPU's in most of future designs
- Main clock insertion delay: about 1.3ns



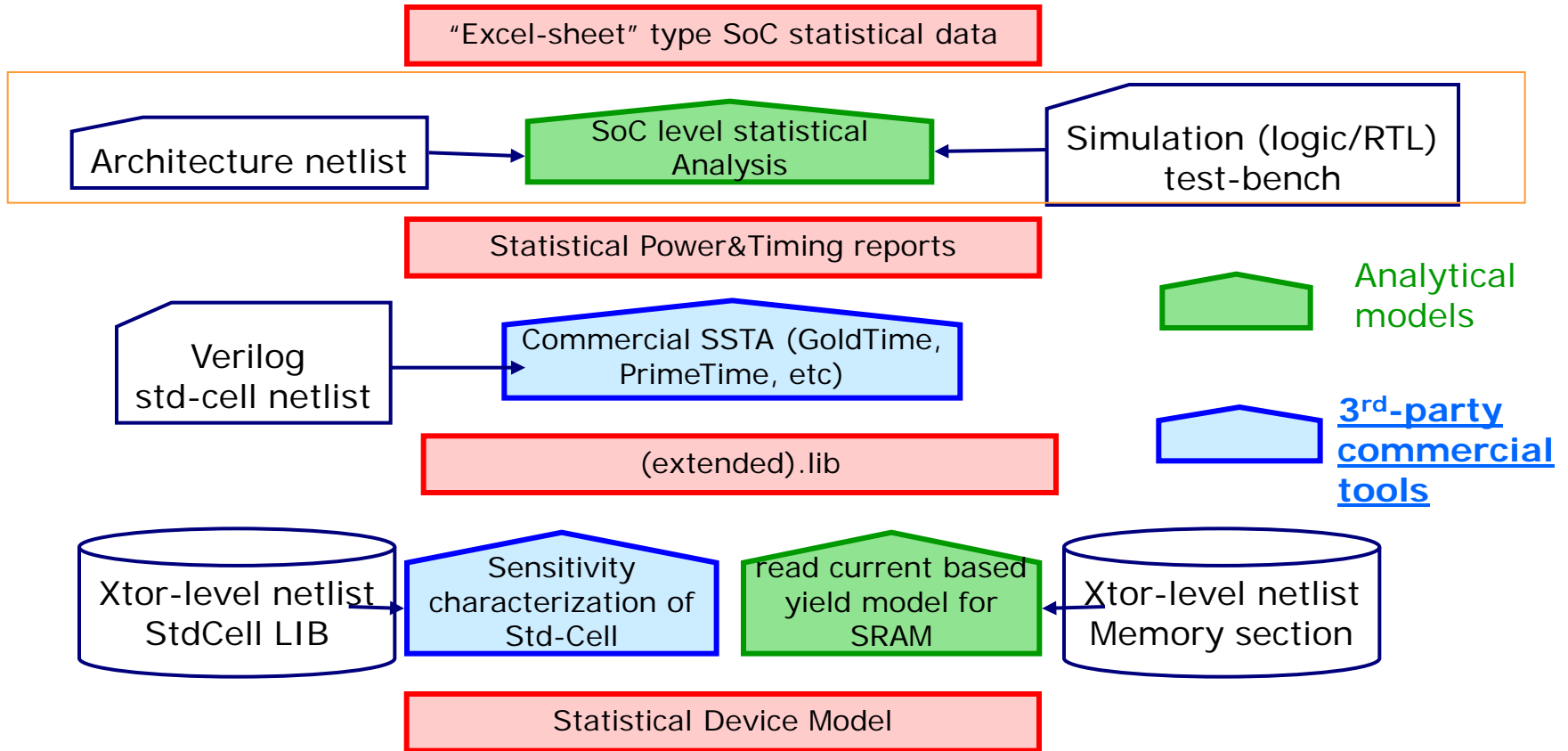
SSTA Hybrid Flow Conclusions

- TAT analysis shows SSTA methodology is not reasonable for large SOC designs
- Very significant user training required
- Understanding statistical reports is a challenge
 - Distributions are not additive
- Moving forward to use AOCVM to model local mismatch
 - Simpler usage model
- Industry is moving toward this approach

Tasks

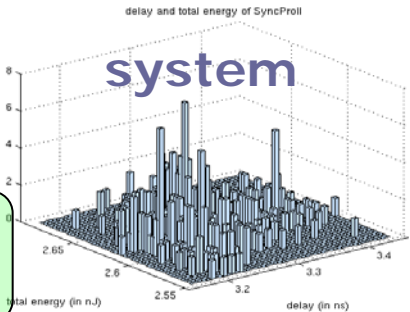
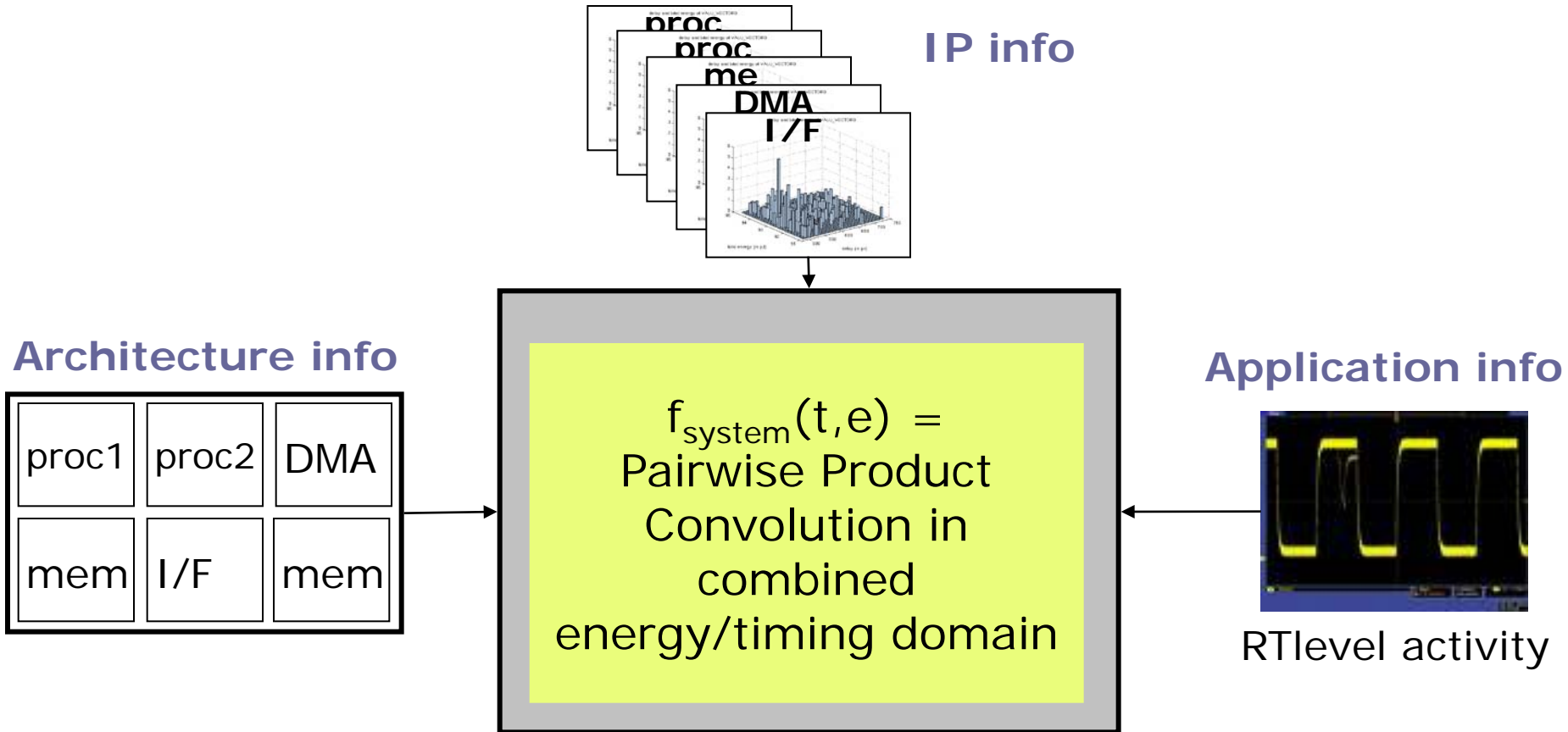
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Task 2.4 Context



Statistical Analysis Flow from device to SoC level

Task 2.4 Integration of Component-level Statistics to Obtain SoC-level Performance/power Variations



The Propagation Operator as Integral

- The combination of the convolution in the energy dimension and the max formulation in the delay dimension of 2 bivariate PDF's is described by the following integral:

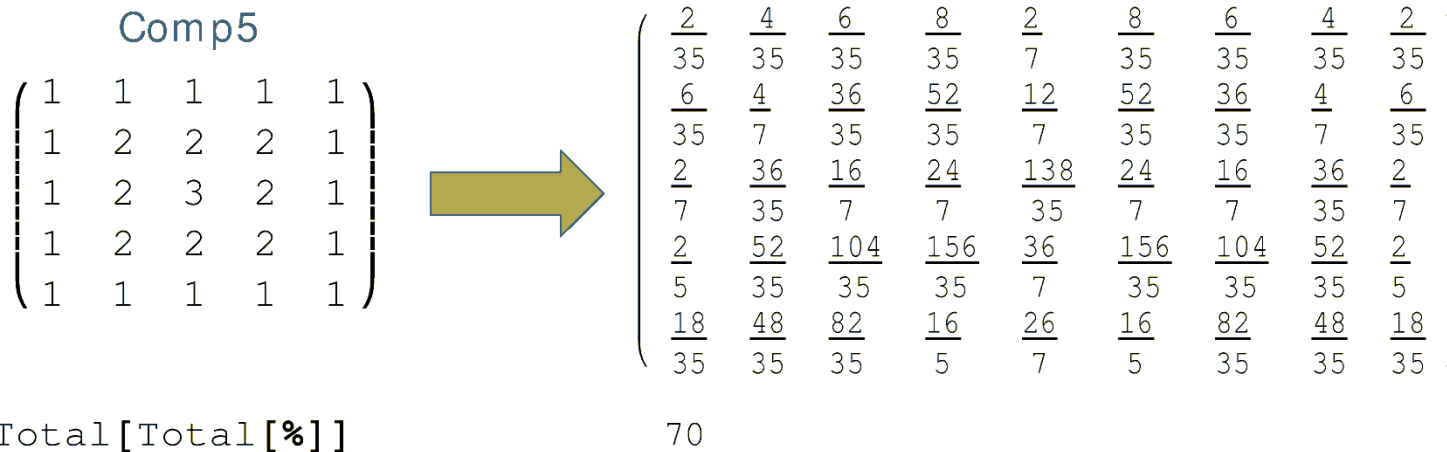
$$f_c[t_d, P_w] = \int_{-\infty}^{\infty} \left(f_1[t_d, P_w - v_p] \int_{-\infty}^{t_d} f_2[u_t, v_p] du_t + f_2[t_d, P_w - v_p] \int_{-\infty}^{t_d} f_1[u_t, v_p] du_t \right) dv_p$$

- Properties of the operator:
 - Commutative
 - Associative
- Operator can be applied onto sequence of modules to compute bivariate architecture level PDF.

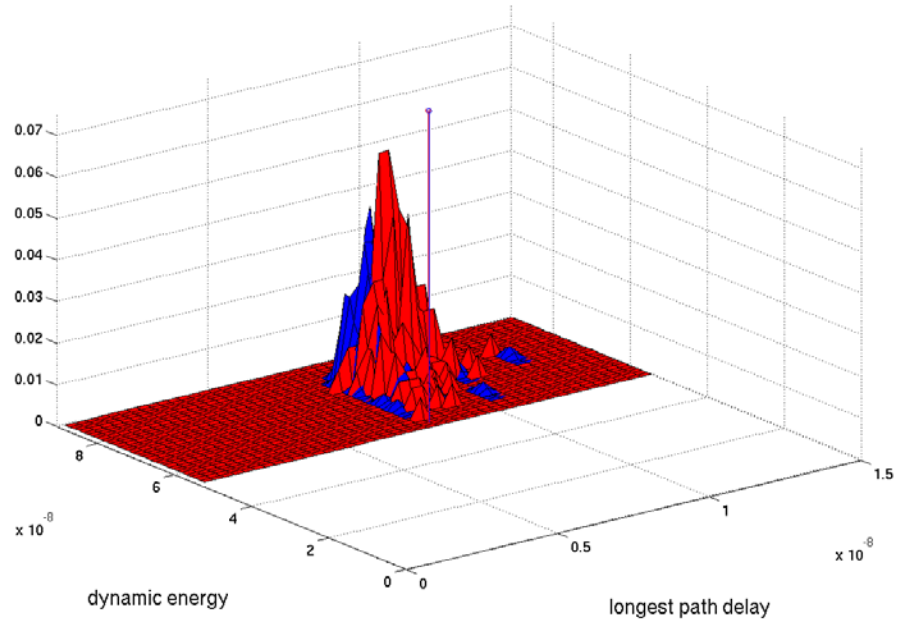
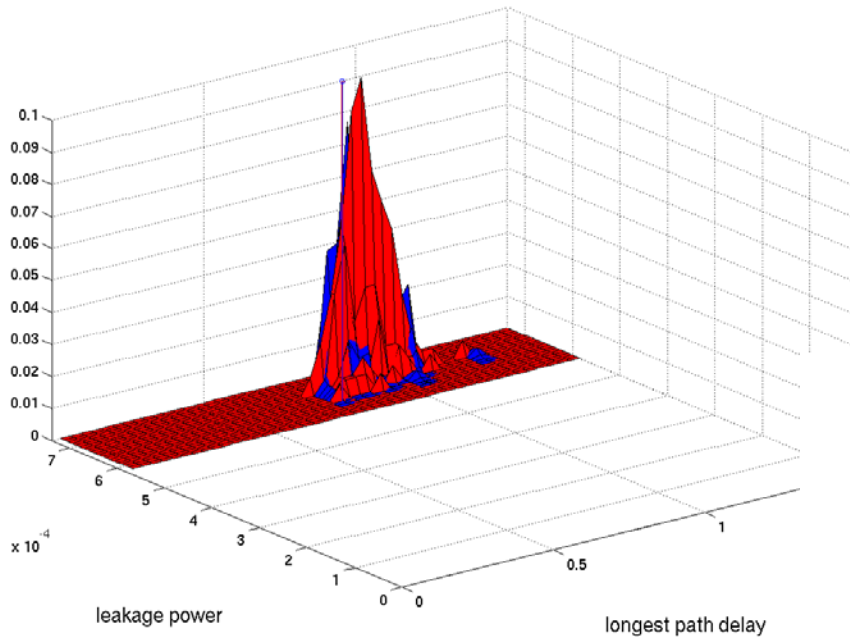
The Fast MaxSum Operator

- To speed up the operator, why not implement it as a specific algorithm to be applied onto both PDF sample matrices?
- The Fast MaxSum operator

MatrixForm[FastMaxSumPDF [Comp5, Comp5]]



Benchmarking the SoC Analysis Technique

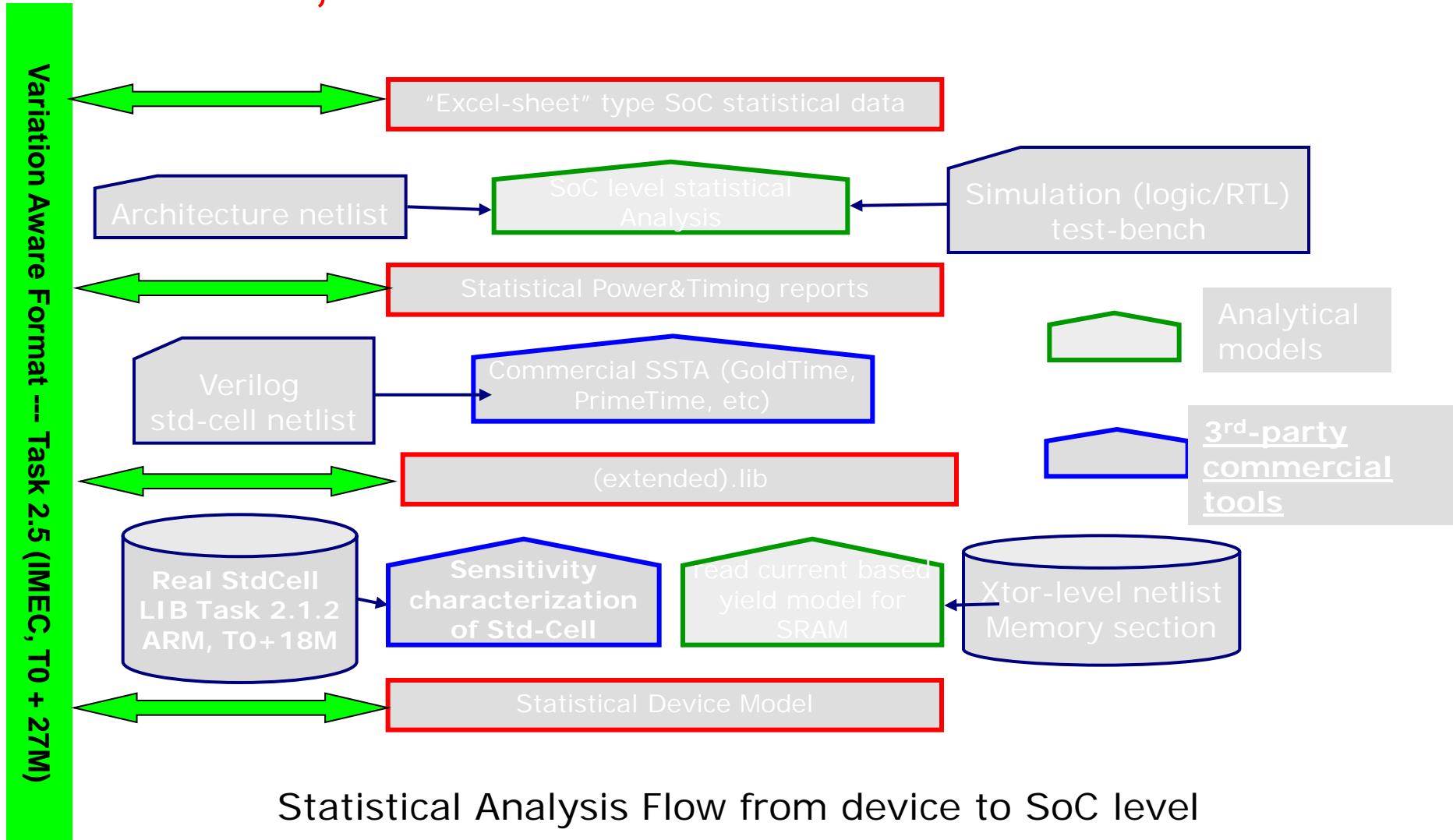


Full system analysis
VS
Partition and system analysis

Tasks

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- **Task 2.5: Variation Aware Information Format**

Task 2.5, Variation Aware Format: Context

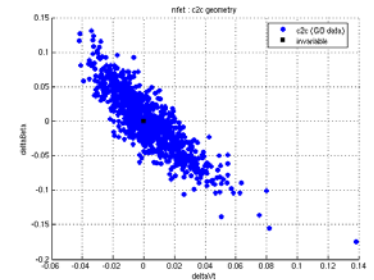


Motivation

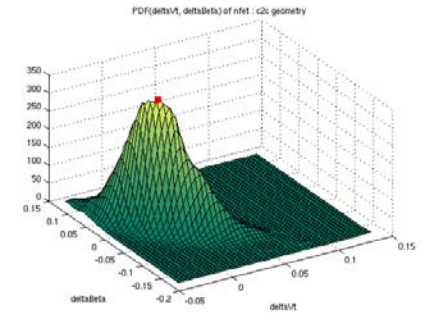
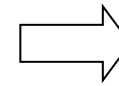
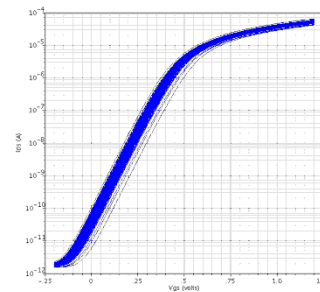
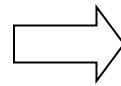
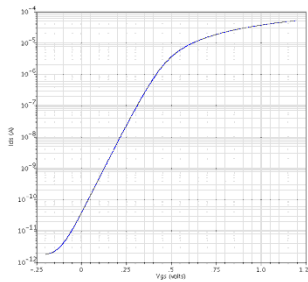
Dramatic increase in process fluctuation calls for an adoption of statistical behavior at any level of a standard design flow.

Imec defines the standard way to

- **Describe** statistical aware models in a unified way for any design level
- **Store and access** (possibly correlated) statistical data in EMC manner
- **Process** statistical data (sample, bin and evaluate statistical metrics)

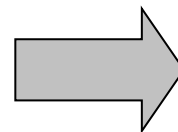


Example: statistical aware MOS model



Required change in **atomic information** accessed by a user

a model parameter represented by a **single value**



a model parameter represented by a **statistical distribution**

Imec Solution – Three Main Parts

1. XML application

1. **Basic building blocks** to keep correlated data with attached statistical information
- **Underlying variability aware models** (MOS model, NBTI, HCD, memory, standard cell, ...)

```

...
<value name="spectre_path" origin="(Author: dobrovol
<container name="cells" type="signature">
  <object dir="D:\users\dobrovol\tadrepos\stdcell\NAND1
  <wmc_set dir="D:\users\dobrovol\tadrepos\stdcell\NA
  <wmc_header type="input_domain">
    <col_header index="2">T2 Vth</col_header>
    <col_header index="4">T4 Vth</col_header>
    <col_header index="1">T1 Vth</col_header>
    <col_header index="3">T3 Vth</col_header>
  </wmc_header>
  <wmc_header type="output_domain">
...

```

2. XML interface (JAVA)

- Exploits standard JAVA SE XML interface to **access XML information chapters**
- Defines higher abstraction layer **to access variability models** with full correlation

The screenshot shows a Java IDE interface. On the left, a list of 'All Classes' includes: Cell, CellLibrary, ChapterBrowser, ChapterName, ChapterType, ColumnHeader, CompareDoubleArray, ComplexVE, CompLibrary, Component, ComponentParamType, Configuration, Container, ContainerType, DelayType, DistTable, DistType, and GaussDist. On the right, the 'Package Class Use Tree Deprecated' view is active, showing the package 'imec.tad.vamif' and the class 'ClassParameter'. Below the class name, the inheritance hierarchy is shown: java.lang.Object, imec.tad.vamif.VamifElement, imec.tad.vamif.ComplexVE, and imec.tad.vamif.Parameter. At the bottom, the class declaration is visible: 'public class Parameter extends ComplexVE'.

BACKUP

Deliverables

■ Delivered Y1:

- D2.1.1: Creation of a 32nm small preliminary library (50 cells) by scaling down a 45nm existing library using “Moor” compliant scaling factors to allow the methodology developments from the partners before availability of accurate 32nm library. (T0+8M)
- D2.2: A methodology and a propagation flow for percolating variability sensitivity in key parameters of the system (e.g., timing, energy) from the device compact model level to the architecture level. Internal sub-deliverables for the consortium are foreseen one per Task (from 2.2.1 to 2.2.3). (T0+12M)

■ Delivered Y2:

- D2.1.2: Documentation and implementation files of the small standard cell library (50-100) based on the restricted design rules to describe the components used to create the demonstration vehicles for other blocks in WP5 using the variability aware modeling flow resulting from WP2. (T0+18M)

■ Upcoming Y3:

- D2.3: Variation-Aware Characterization techniques based on novel statistical analysis techniques and novel Monte Carlo statistical techniques based on standard analysis and simulation tools, for gate-level netlists, macro-blocks and SoC architecture level netlists. (T0+27M)
- D2.4: Variation-aware electronic information format for each level of abstraction and an open framework supporting bottom-up transferring of information from one level to the next one. (T0+27M)

Task 2.1.1 Design of Standard Cell Library

Development and characterization of a 32nm standard cell library under variability impact

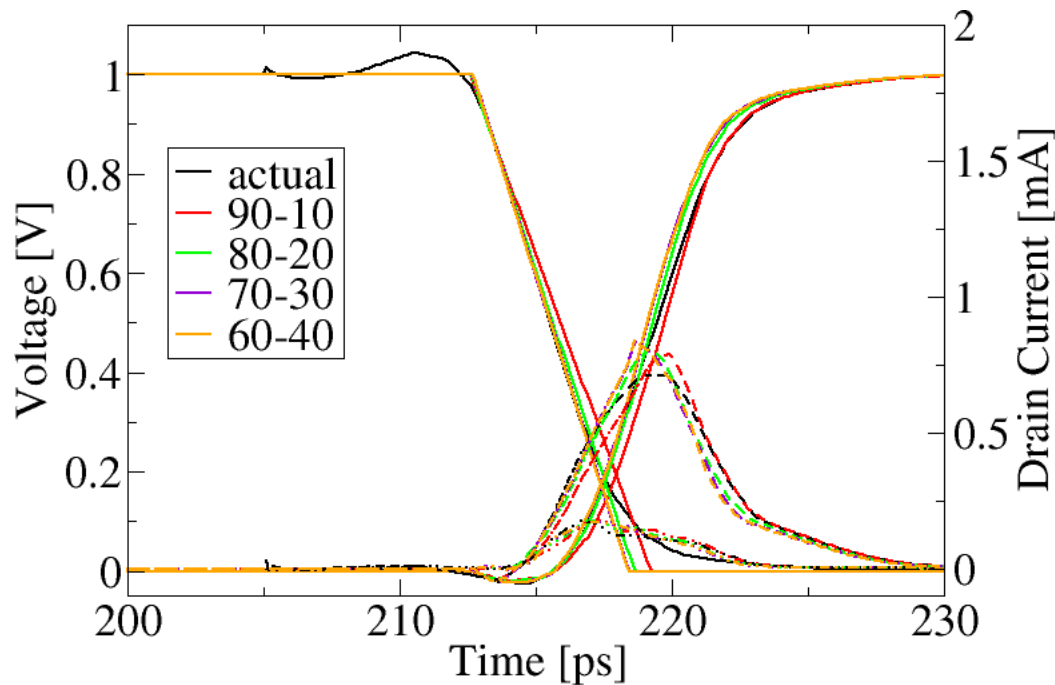
- Originally one library was forecasted
- Now Split in two versions
 - Scaled Library Generation: before availability of technology data this library enables tools developments. DONE 2008
 - Real Library, DONE in 2009
- T2.1.1 closed

Task 2.1.2 Statistical Characterization of Standard Cell Library

What? Statistical Characterization with non-statistical EDA-tools.

Why? To allow for UoG models. To circumvent NLDM.

How? Automatically generated testbeds with smooth signals and UoG-statistical compact models with optimised parasitic extraction.



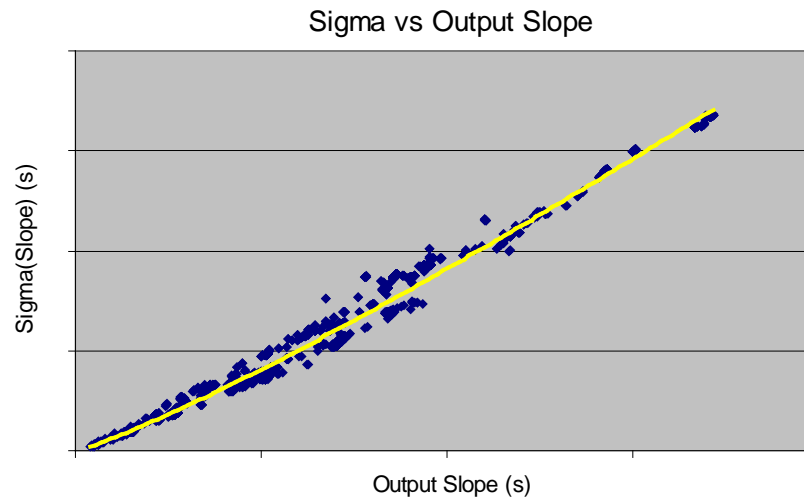
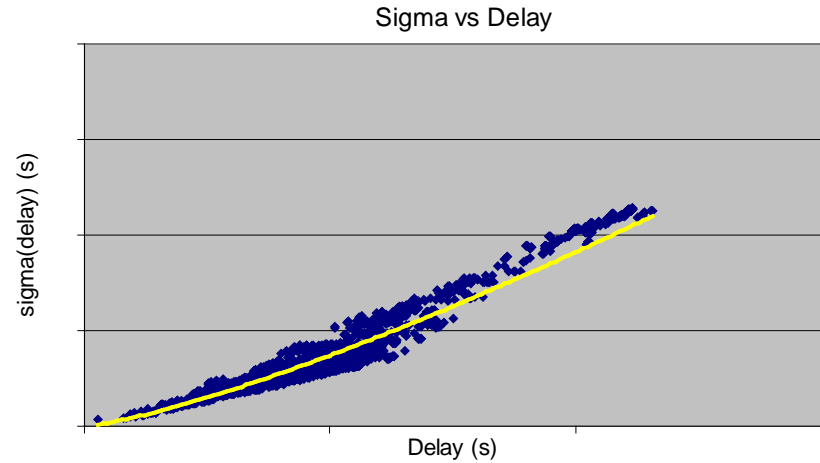
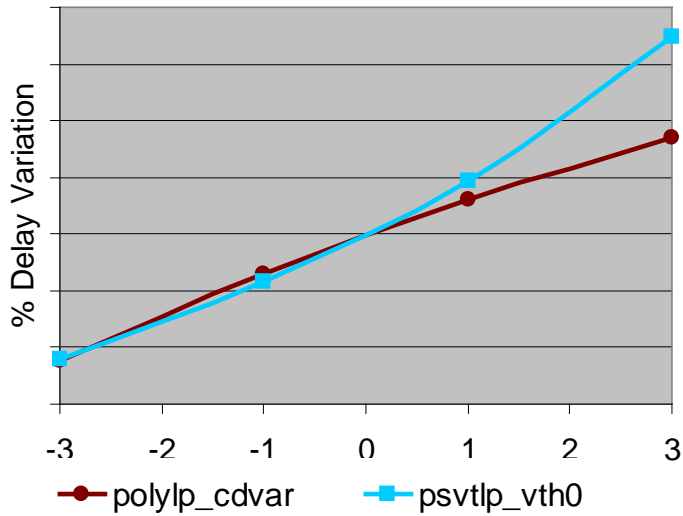
Outcome:

Up to 10% error (timing) of NLDM shown.

Task 2.1.2 Statistical Characterization of Standard Cell Library

- The statistical characterization methodology and flow was extended to CMOS045LP (45nm low-power technology)
 - CMOS045LP IS the most advanced CMOS nanometer technology in production at ST
- An important factor to be considered is the non-linear dependence of cell delay on process variations
 - Poly CD and threshold voltage exhibits a non-linearity (more significant in PMOS devices)
 - Poly CD non-linearity was known in CMOS065LP but threshold voltage was observed in CMOS045LP likely due to large deviations coupled with low voltage and temperature
- Other cell timing characteristics like propagation delay and output slope were analyzed
 - The behavior against process variability is reported in next slide

Task 2.1.2 Statistical Characterization of Standard Cell Library



Hybrid Statistical Analysis Flow

- The potential benefits of SSTA to reduce the design margins and improve the design yield were demonstrated on an industrial imaging processor in CMOS065LP technology in the frame of REALITY
- However the statistical library characterization runtime proved to be a major bottleneck for the industrial adoption of SSTA
- Moreover the design teams were extremely reluctant to change the traditional sign-off methodology
 - Designers do not like distributions!
- Therefore in 2009 the research activity in WP2 was focused on developing a SSTA hybrid flow in CMOS045LP technology
- The within-die (WID) random variations (i.e., device mismatch) were considered

Task 2.1.2 Statistical Characterization of Standard Cell Library

- A practical and accurate technique to reduce the mismatch characterization time was developed and validated
- Based on simultaneous identification of transistors impacting the cell performances, on reduction of the characterization grid size, and on identification of a restricted set of transistor parameters that mostly impact on the device performances
- The approach developed for random mismatch characterization was validated by comparing statistical static timing analysis (SSTA) against transistor-level Monte Carlo analysis on several path delays extracted from industrial digital blocks in CMOS065LP technology designed at ST