

# Multi Layer Metallization

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## *Abstract*

*Scaling down of interconnect will increase circuit density at the detriment of performance if no improvement in both design and technology are introduced. Consequently, new materials improving this interconnect performance will be introduced such as conductor with lower resistivity compared to aluminum alloys and dielectric with lower  $\epsilon$  compared to silicon oxide as well as new architecture for integration.*

## **1 Introduction**

The need of multi-level interconnects is crucial for the future of microelectronics regarding logic or memory applications. The requirements concerning the interconnects for logic application are more and more aggressive in order to improve the functional density and the dynamic performance, see table-1. The number of metal levels increases: 5 for 0.35 $\mu\text{m}$  6 or 7 for 0.25 $\mu\text{m}$  etc... Consequently, the Back End part of the line which is mostly single wafer processing, represents at least half of the full wafer processing. This evolution has a direct impact on the process complexity, process cost, intrinsic yield and on the dynamic performance of the circuits.

In the next years, the IC industry will have to develop and introduce in production new techniques and new materials for interconnects with the following requirements

- increase in interconnect density with new architecture like damascene, local interconnect, borderless contact and via
- decrease in process induced damage regarding the Front End part of the line ; this item addresses soft plasma processes for either dry etching, cleaning or material depositions

- improvement in performance by the introduction of lower resistivity metals like copper or lower  $\epsilon$  dielectric like SOG or polymers

- improvement in metal reliability in terms of electromigration and stress migration.

In this paper, we will pay more attention to the parasitic in interconnects, the introduction of dual damascene as new interconnect scheme and new materials such as low  $\epsilon$  Spin On Dielectric (SOD) for intermetal isolation and copper as low resistivity metal.

Parameter	Technology				
	1998 0.25 $\mu\text{m}$	2001 0.18 $\mu\text{m}$	2004 0.13 $\mu\text{m}$	2007 0.1 $\mu\text{m}$	2010 0.07 $\mu\text{m}$
Number of metal level for logic	5-6	6-7	6-7	7-8	7-8
Mean interconnect density m/cm <sup>2</sup>	50	70	105	125	155
Interconnect length m/chip	840	2400	4100	6300	10000
Minimum metal 1 CD $\mu\text{m}$	0.4	0.3	0.2	0.15	0.1
Minimum contacted metal pitch $\mu\text{m}$	1	0.6	0.45	0.35	0.25
Contact via size $\mu\text{m}$	0.3	0.2	0.15	0.1	0.08
Contact and via aspect ratio	3	3.5	4.2	5.2	6.2
Frequency MHz	450	600	800	1000	1100

Table 1 Evolution of the interconnect parameters<sup>1</sup> with the technological generations

## 2 Limitations induced by interconnect parasitics

While transistor scaling continues to improve in current drivability, metal interconnect are now a significant limiter and are as important as transistors in determining circuit density and performance<sup>2,3</sup>. The limiting factors are the increase in both cross talk noise and RC delay with the decrease in line space and the increase in line length. This corresponds to two regimes of interconnects :

- a local one which is used within the cells and blocks at the minimum pitch allowed by the design rules
- a global one which is used for inter-block communication at the upper levels with relaxed pitch.

The cell and block interconnects will be more sensitive to cross talk while the long inter-block communication will be sensitive to RC delay. Solutions to these problems can be found to some extent by design with the introduction of repeaters for the long inter-block communication and adapted size of the buffers to minimize cross talk.

As technological issues, two approaches can be proposed<sup>4-6</sup>: the adaptation of the metal line aspect ratio depending on the metal level and/or the introduction of new materials with lower resistivity for the metals and lower  $\epsilon$  for the dielectric.

Simulations have been performed on four different architectures for a metal pitch of 1 $\mu\text{m}$  (0.6/0.4 $\mu\text{m}$  line/space) :

- conventional architecture using a 0.8 $\mu\text{m}$  metal stack (0.65 $\mu\text{m}$  AlCu and 0.15 $\mu\text{m}$  barrier + ARC) and deposited oxide for intermetal dielectric with  $\epsilon = 3.9$
- the introduction of an embedded low  $\epsilon$  materials between the aluminum lines
- the introduction of copper with an equivalent line resistance to Al (thinner metal layer) assuming a resistivity of 1.9 compared to 3.1  $\mu\Omega\cdot\text{cm}$
- the introduction of both low  $\epsilon$  dielectric and copper.

The simulations were done in order to extract the propagation delay in a 1cm long bus line and the cross talk capacitance at the minimum pitch.

The results concerning the cross talk capacitance (Figure 1) show that going to either low k material with  $\epsilon=2.5$  or to Cu with the same line resistance gives the same decrease of 25% in cross talk capacitance while going to integrate both Cu and low  $\epsilon$  gives about 50% in cross talk capacitance decrease. Consequently, this decrease in capacitance allows to use longer lines with the same amount of cross talk noise (10 or 20% of VDD for example).

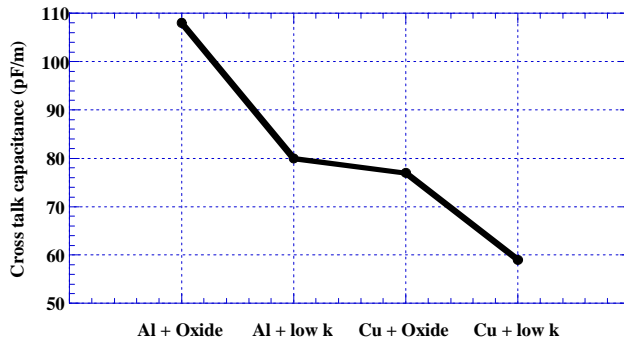


Figure 1 : Evolution of the cross talk capacitance as a function of different architectures

The Figure 2 shows the impact of these different architectures on both the propagation delay time and the power dissipation in a one cm Metal-3 BUS line over substrate for various  $\epsilon$  values. Going from conventional architecture to embedded low  $\epsilon$  or Cu lines with the same resistance as Al gives the same decrease of 25% in delay and power. A 50% decrease in delay and power is achieved when both embedded low  $\epsilon$  ( $\epsilon = 2.5$ ) and Cu are used. For the ideal case where  $\epsilon = 1$ , meaning that ideal stable air bridges are manufacturable, a 80% decrease in delay is obtained showing the limits of what could be obtained by technology improvements.

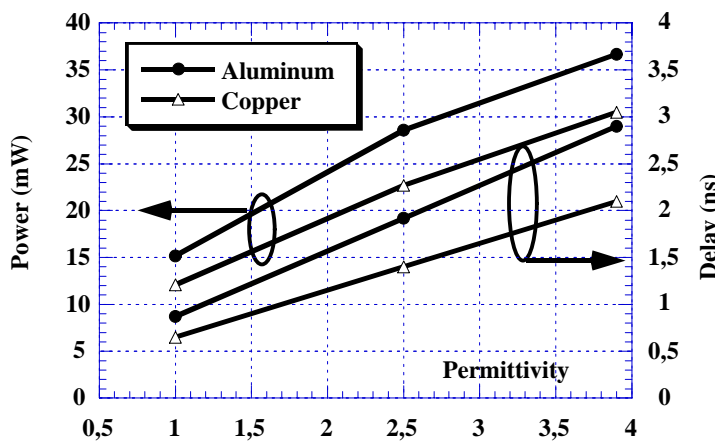


Figure 2: Impact of the introduction of Cu and low  $\epsilon$  material on both propagation delay and power dissipation in a 1cm long bus line

These simulations show that for the future generation  $0.18\mu\text{m}$  and below, and may be for  $0.25\mu\text{m}$ , the introduction of these new materials will be mandatory. These implementations will certainly be done in two steps : the introduction of low  $\epsilon$  previously to Cu.

### 3 Introduction of new materials and architectures

#### 3-1 Low k dielectric

These materials become interesting when the  $\epsilon$  is lower than 3 compared to 3.9 and even 4.5 for deposited oxide. These products can be considered as polymers or mineral ones depending on their carbon contents<sup>7-8</sup>. The elaboration can be performed by either Spin On or CVD. The main requirements regarding the integration point of view are the following :

- stability to
  - thermal treatment up to 425-450°C, oxygen plasma, moisture absorption
- adhesion to
  - deposited oxide, metal Ti, TiN mainly.
- compatibility with
  - oxide dry etching and CMP.
- good gap filling capability

The most advanced materials at the research level are to day the organic aerogel<sup>9</sup> and the air bridge technique leading to  $\epsilon = 1.3-1.6$ . Recent works have demonstrated the integrability of these promising techniques.

The most mature materials with  $\epsilon = 2.5-3$  are silsesquioxane based Spin On Dielectric. Two varieties of these products are available

- a mineral one : the Hydrogen SilsesQuioxane (HSQ)
- an organic one : the Methyl SilsesQuioxane (MSQ).

These products are mostly used with the following process steps :

- metal patterning
- thin oxide liner deposition
- SOD deposition and thermal annealing
- thick oxide deposition, global planarization by Chemical Mechanical Polishing.

The thin oxide liner is sometime not used. In this case , the process is defined as Direct on Metal.

The gap filling and planarization capability of the HSQ are shown on Figure 3. No void and no cracks are observable in the 0.3 $\mu$ m inter metal line spaces.

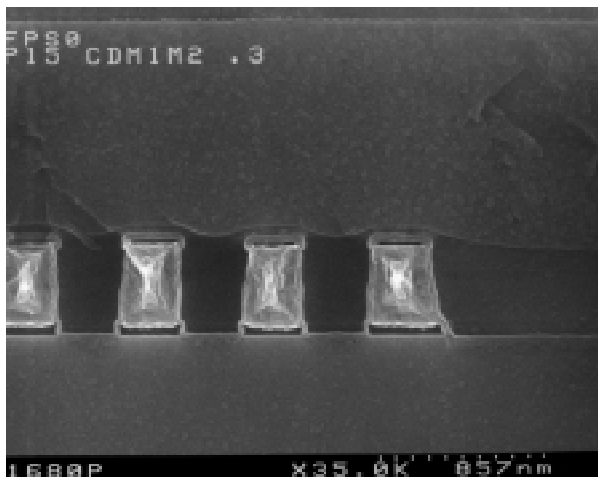


Figure 3-a

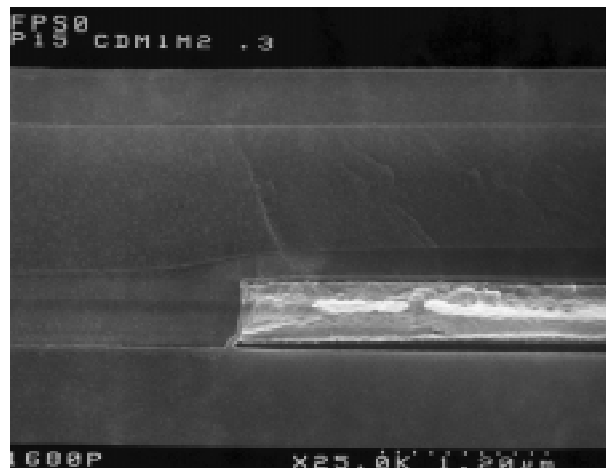


Figure 3-b

Figure 3 : SEM cross section analysis showing

- a- the gap fill capability of the HSQ SOD in 0.3 $\mu$ m metal spaces
- b- The thicker SOD layer on large structures

The planarization capability of these SOD leads to variable SOD thickness depending on the metal density. As the structure is planarized by CMP, the total dielectric to be etched

during via patterning is the same whatever the metal density is. Consequently, the etch process has to be adapted in order to reach an equivalent etch rate for both oxide and SOD. This process adaptation is not easy to find because the SOD are either mineral or organic needing chemistry which are more  $CF_4$  or  $O_2$  based. The Figure 4 evidences this problem, the process was developed for the HSQ leading to good vertical via profile (Figure 4-a) while the same process used for MSQ etching leads to etch stop and bowed via profile (Figure 4-b).

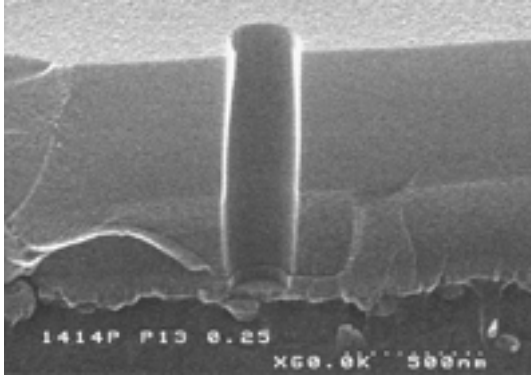


Figure 4-a

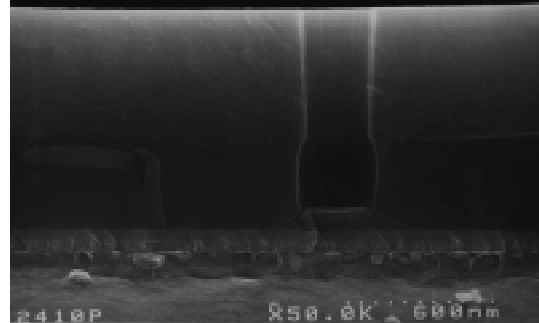


Figure 4-b

Figure 4 : SEM cross section analysis showing the via profile after etching  
 -a- Hydrogen Silsesquioxane SOD  
 -b- Methyl Silsesquioxane SOD

Cross talk capacitance has been measured on dedicated structures processed with either a standard intermetal dielectric or with embedded SOD. The results are shown in Figure 7 : a 20% decrease in the lateral capacitance is obtained whatever the metal space is. This decrease is due to a lower  $\epsilon$  between the lines.

### 3-2 Copper and dual damascene

Copper is a good candidate to reduce the metal resistivity but as Cu dry etching is difficult<sup>10</sup>, a damascene structure is needed to form the interconnects. A barrier layer is needed to prevent from Cu diffusion into  $SiO_2$  and Si. This barrier has to be as thin as possible<sup>11</sup>, in the range of 20 to 40nm, to keep the benefits of Cu.

Self aligned dual damascene architecture has been recently proposed<sup>12-13</sup>. This self aligned structure is based on the etch rate selectivity<sup>14</sup> between SiN and  $SiO_2$  and not on the metal and via litho permutation as previously published<sup>15</sup>. The structure is described on Figure 5

- a-  $0.8\mu m$  oxide -  $0.2\mu m$  SiN bilayer deposition,
- b- DUV litho of holes and dry etch transfer in the SiN layer,
- c-  $0.9\mu m$  oxide deposition,
- d- DUV litho of lines and oxide dry etch down to the substrate (hole + line),
- e- Ti-TiN liner and Cu deposition, CMP of Cu

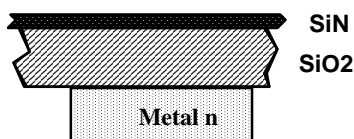


Fig 5-a

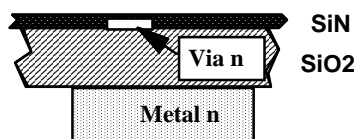


Fig 5-b

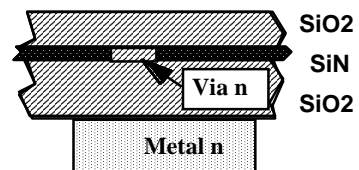


Fig 5-c

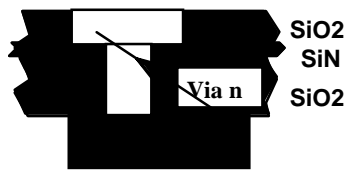


Fig 5-d

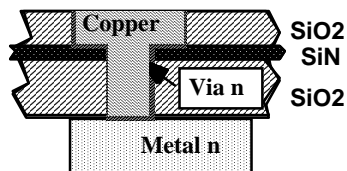


Fig 5-e

Figure 5: Schematic description of the Self Aligned Dual Damascene architecture

The key parameter of this architecture is the so called corner effect : SiN etch selectivity at the via line junction where the sputtering effect is maximum (Figure 5-d). This selectivity is shown on Figure 6 : SiN is still present at the corner (Figure 6-a) and on the large area corresponding to the metal lines (Figure 6-b)

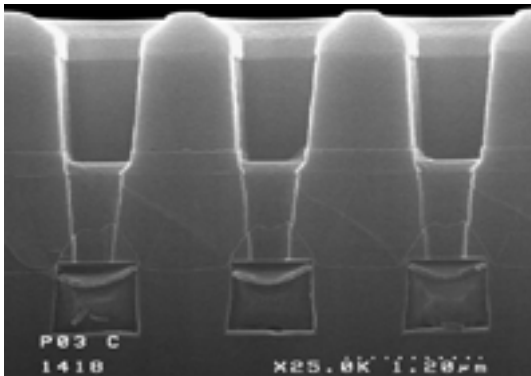


Figure 6-a

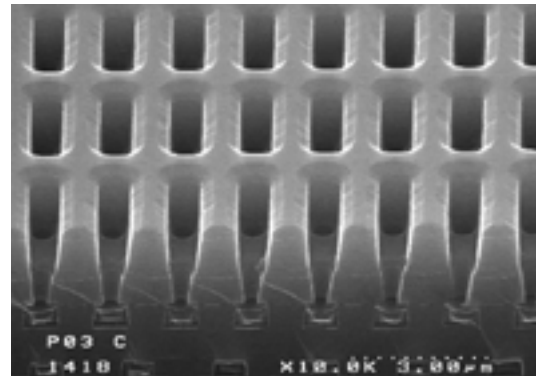


Figure 6-b

Figure 6: SEM micrograph showing the Dual Damascene structure after etching  
-a- cross section -b- semi top view

This process has been implemented on CMOS wafers<sup>12-13</sup>. The compatibility with Si regarding contamination has been demonstrated and a 15% increase in dynamic performance was obtained. Cross talk capacitance was also measured and compared to standard architecture : as for low  $\epsilon$  material a decrease of 20% in capacitance is obtained (Figure 7) whatever the metal space is. These cross talk capacitance measurements are in good agreement with the simulated values (comparison Figure 1 and 7)

## 5 Conclusion

This paper has shown that we will soon reach the limits in technology improvement by the introduction of new materials. Physics has limits :  $\epsilon$  will never be smaller than 1 and superconductors materials are not available for microelectronics.

The synergy between designers and technological engineers has to be more and more efficient in order to use the available technology at its limits. A big effort has to be done in the 3D modeling and simulation of interconnect parasitic to improve the TCAD tools performance for better dynamic circuit simulation. The number of interconnect layers can be increased with careful design rules definition in terms of metal pitch and thickness for dedicated layers such as short range, mid range and long range interconnect.

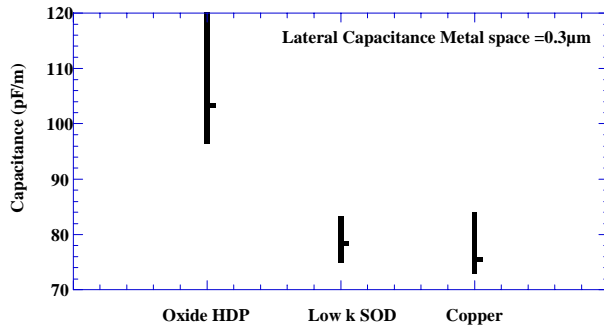


Figure 7-a

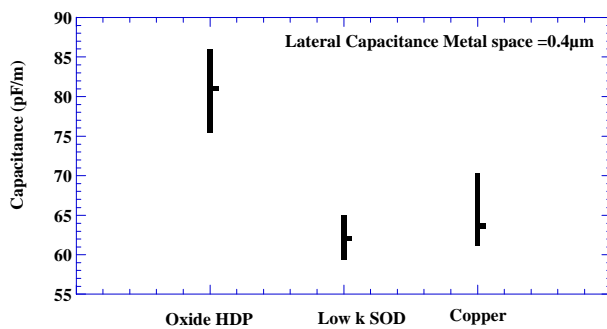


Figure 7-b

Figure 7:  
Evolution of the cross talk capacitance with either deposited oxide, low  $\epsilon$  SOD or Copper for  
-a- 0.3µm metal spaces  
-b- 0.4µm metal spaces

## Acknowledgment

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