Limitations of Double Polysilicon Self-Aligned Bipolar Transistor Structure

K. Inoh, H. Nii, S. Yoshitomi, C. Yoshino, H. Furuya, H. Nakajima, *H. Sugaya,
*H. Naruse and Y. Katsumata
Microelectronics Engineering Laboratory, Toshiba Corporation
*Semiconductor Group, Toshiba Corporation
1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan
Phone:+81-44-549-2335 Fax:+81-44-549-2291
E-mail:inoh@ull.rdc.toshiba.co.jp

Abstract

In this paper, we demonstrate that the sidewall spacer thickness of double polysilicon self-aligned bipolar transistor structure is one of the fundamental limitations in bipolar transistor scaling by using an accurate small signal equivalent circuit. The simulated results show that the maximum fT reduces to half when the sidewall spacer thickness reduces from 0.1μm to 0.025μm.

1. Introduction

Recent advances in bipolar technology employing self-alignment concepts have drastically reduced the bipolar device size and the accompanying parasitic resistances and capacitances. Among many self-aligned structures, double polysilicon self-aligned bipolar transistor structure has been the most popular way to achieve very high speed bipolar LSIs. Moreover, the down-scaling of this structure has led to a very significant decrease in the switching delay of circuits. In scaling down, physical limitations such as punchthrough and Kirk effect can be avoided by increasing the base and collector doping as base width decreases and current density increases. However, an increase of contact resistance and emitter resistance remains serious problem.

The purpose of this work is to predict the limitations of double polysilicon self-aligned bipolar transistor structure. With downsizing of this structure, sidewall spacer thickness becomes thinner. This leads to an increase of the peripheral component of emitter base capacitance, results in a degradation of high frequency characteristics of bipolar transistor.

2. Fabricated Device Characteristics

A SEM cross sectional view of the fabricated transistor is shown in fig.1. The base layer is grown by a low temperature epitaxial technique. The boron doping level is $5\times10^{18}/cm^3$ and the base layer thickness is about 40nm.[1] Typical device parameters are summarized in table.1. An Emitter size of this transistor was $0.3\times1.0\mu m^2$ to achieve low power dissipation. Due to the rectangular profile of base layer by the epitaxial technique, high cutoff frequency and high BVceo were achieved simultaneously. Both shallow trench isolation and down-scaling of transistor also led to very low base-collector capacitance of 2.1fF. However, relatively high emitter-base capacitance (Ceb) of 6.24fF was measured in spite of small emitter size. In order to investigate a cause of this high Ceb, some transistors with different emitter size were measured. As a result, the total Ceb was divided between its area component of 1.041fF and its peripheral component of 5.2fF as shown in fig.2. Thin sidewall spacer, which is caused by down-scaling of transistors, led to an increase of peripheral component of Ceb.

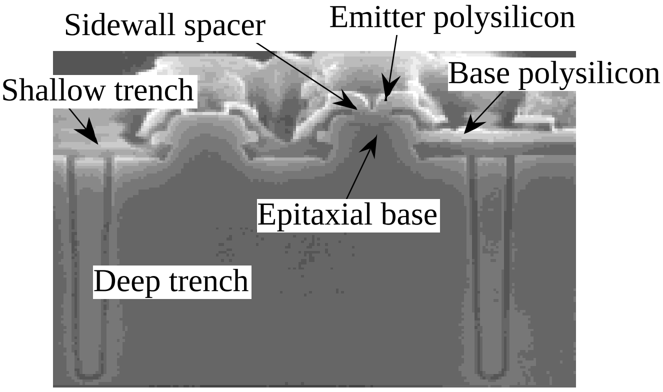
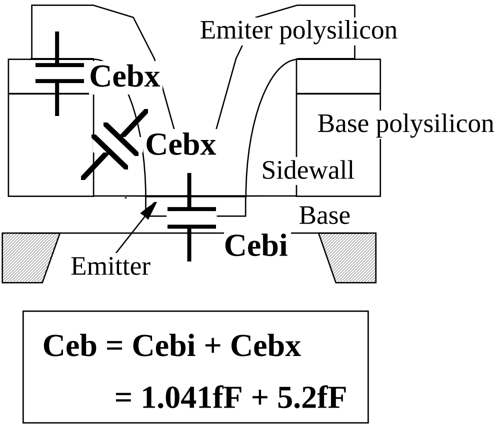


Figure 1. SEM cross sectional view



Ceb = Cebi + Cebx

= 1.041fF + 5.2fF

Figure 2. Components of emitter-base capacitance

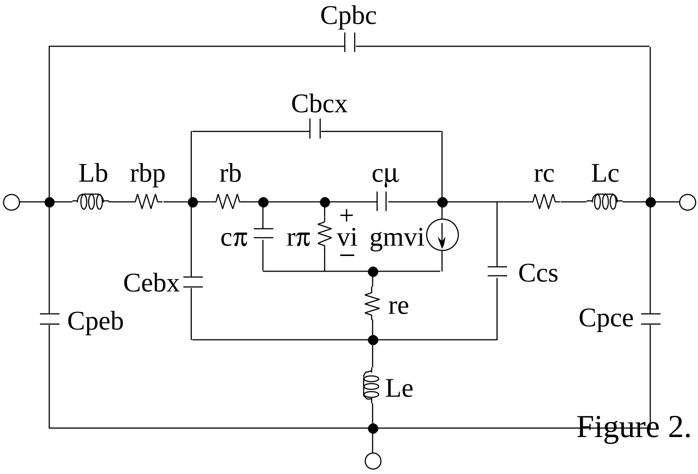


Figure 3. Small signal equivalent circuit of BJT at Ic=1.3mA

3. Small Signal Equivalent Circuit

A small signal equivalent circuit is shown in fig.3. We introduced two parasitic capacitances. Capacitance Cebx represents the peripheral component of Ceb and capacitance Cbcx is related to oxide layer between base polysilicon layer and collector layer. The S-parameter measurement were performed at Ic=1.3mA and Vce=2V from 0.1 to 11.1 GHz. All pad capacitances and series impedances were measured by using open- and short- structures. Table2 shows the extracted parameter values of 10 parallel bipolar transistor. The simulated S-parameters of the equivalent circuit using a set of parameter values in table2 are compared with the measured S-parameters in fig.4. The results show the good agreement.

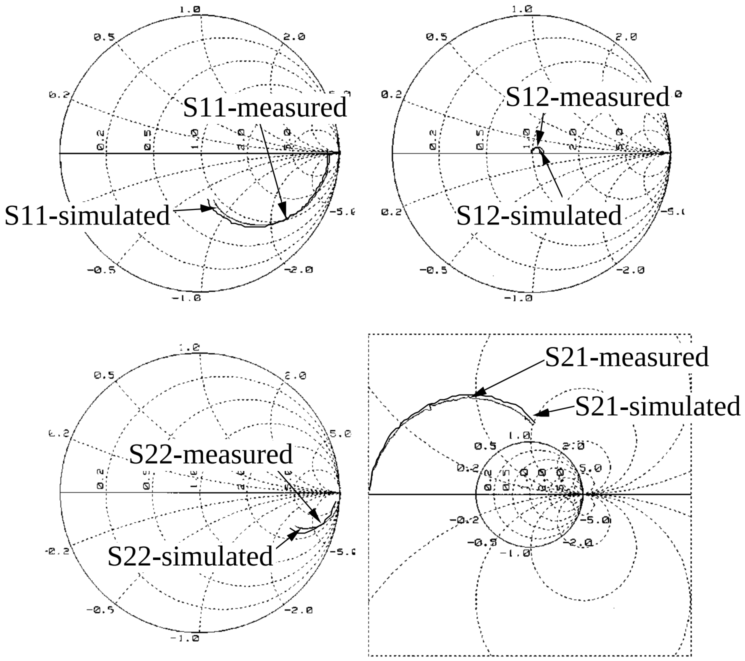


Figure 4. Comparison between measured and simulated S-parameters of the BJT

4. Prediction of Scaling Limits

By using above small signal equivalent circuit, the dependence of emitter scaling on transistor characteristics, mainly high frequency characteristics, was simulated. Parameter values used in the simulation are summarized in table3. The simulated results is shown in fig.5. The maximum fT and fmax are still high when sidewall space thickness is more than

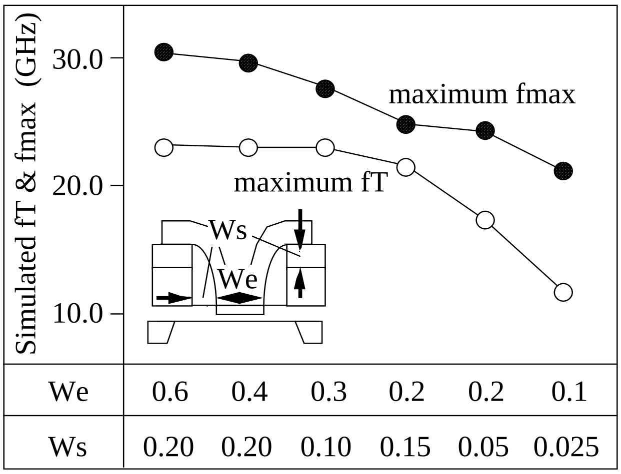


Figure 5. Dependence of simulated fT and fmax on sidewall spacer thickness (Ws)

0.1μm. However, the maximum fT has dropped to 12.5GHz when the sidewall spacer thickness was 0.025μm. This results indicate that the more down-scaling of transistor leads to degradation of transistor performance.

5. Conclusion

We have predicted the limitations of double polysilicon self-aligned bipolar transistor structure. With downsizing of bipolar transistor, sidewall spacer thickness becomes thinner. This leads to an increase of the peripheral component of emitter base capacitance, results in a degradation of high frequency characteristics of bipolar transistor. We conclude that the sidewall spacer thickness of double polysilicon self-aligned bipolar transistor structure is one of the fundamental limitation in bipolar transistor scaling.

References

[1] C.Yoshino et al, Symposium on VLSI Technology, p131, 1995