

A 1V Bootstrapped CMOS Digital Logic Family

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1 Abstract

A new technique that improves the drive capability of digital circuits operating at low voltages is described. A coupling capacitor at the input shifts the potential of the gate to increase the gate-source voltage for higher conductance. Speed increases by 5 folds and the device is capable of operating at voltages below the threshold level in bulk CMOS.

2 Introduction

Scaling the power supply is the most effective means of achieving low power performance in CMOS VLSI. One option is to migrate to a process with a reduced threshold voltage (V_t) in order to maintain a comparable speed performance [1, 2, 3]. This, however carries the penalty of higher leakage currents. This paper presents a technique that speeds up the operation of digital circuits operating at low voltages (less than 1.2V) without the need to lower the threshold voltage. The approach raises the gate-source voltage by lowering/increasing (pMOS/nMOS) the gate voltage instead of lowering V_t . A bootstrap capacitor is used at the input of a MOS gate to shift the gate voltage for higher driving capability.

3 Bootstrapped CMOS

A Bootstrapped CMOS (BCMOS) inverter gate is illustrated in Figure 1. Each transistor has its own bootstrap capacitor to allow the gate voltage to be changed dynamically as the input changes. The diodes for the pMOS and nMOS transistors are for bootstrapping the gate voltages to reference voltages V_d (node gatep) and $V_{dd}-V_d$ (node gaten) respectively, where V_d is the cut-in voltage of the diode. Assume initially the input is at GND, the pMOS transistor is turned on and the gate voltage at node gatep (V_{gatep}) is at a voltage level that allows the pMOS transistor to turn on ($V_{sg} > V_t$). Also assume that $V_{gatep} < V_d$, so that the diode is not forward biased. As the input rises to V_{dd} , node gatep rises correspondingly since it tracks the input voltage through the coupling capacitor. However V_{gatep} can only reach V_d as the diode becomes forward biased when V_{gatep} rises. Node gatep is then clamped to V_d when the input is at V_{dd} . The pMOS transistor will turn off in this instance as the source-gate voltage is less than the threshold of the pMOS device ($V_{dd}-V_d < V_t^1$). As the input voltage falls, V_{gatep} falls in unison and the diode no longer becomes forward biased. Node gatep floats and drops to V_d-V_{dd} when the input voltage is at GND. The gate voltage is thus negative with respect to V_{dd} , turning on the pMOS transistor hard and increasing the drive substantially. This allows the output loads to be charged up faster, increasing the speed of the logic. The operation of the nMOS transistor is similar, except that gaten is clamped to $V_{dd}-V_d$. The higher gate voltage increases the conductance of the nMOS device, reducing the discharge time. Figure 2 shows the waveforms of the input, output, gatep and gaten nodes.

¹ V_t is typically 0.9V for ORBIT's 1.2u CMOS process

4 Design Considerations

4.1 Bootstrap Capacitor

The capacitance at the gate node consists of the gate capacitance (C_{gb}), the parasitic capacitances (C_{gs} , C_{gd}) and the depletion capacitance of the diode (C_{dep}). The depletion capacitance is both voltage and area dependent. Assuming a minimum size diode is used to minimize the capacitance at the gate node, the dominant capacitance is then the gate to bulk capacitance. Let the combined capacitance be represented by C_p as shown in Figure 3. The fluctuation of the gate voltage (V_{gate}) is then given by

$$\Delta V_{gate} = \frac{C_{boot}}{C_{boot} + C_p} \cdot \Delta V_{in} \quad (1)$$

where ΔV_{in} and ΔV_{gate} represent the change in the input and the gate potential respectively. As can be seen from the expression, C_p should be minimized so that the full change at the input is reflected across the bootstrap capacitor. A large ΔV_{gate} will result in a higher drive of the transistor. With $\Delta V_{in}=1V$ ($V_{dd} = 1V$) and an acceptable ΔV_{gate} of 0.8V, C_{boot} will need to be at least 4 times the capacitance of C_p .

If the capacitances for the pMOS and nMOS transistors are assumed to be identical, then the equivalent load at the input of the BCMOS inverter is given by:

$$\begin{aligned} C_{equ} &= 2(C_b//C_p) \\ &= \frac{2C_{boot}}{k+1} \quad \text{or} \quad \frac{2kC_p}{k+1} \quad \text{for } C_{boot} = k \cdot C_p \end{aligned}$$

Decreasing C_p to reduce the input load capacitance implies reducing the size of the gate since it is the dominant capacitor, which will lead to a lower conduction current. Hence it is important to reduce as much as possible the parasitic components in C_p .

4.2 Voltage Supply Limits

In order to ensure that the pMOS transistor does not turn on when the input is high, the source to gate voltage must be less than the threshold voltage. Assume that the pMOS gate voltage (V_{gatep}) swings between V_{ph} and V_{pl} ($\Delta V_{gatep}=V_{ph}-V_{pl}$), where V_{ph} and V_{pl} denote the upper and lower limits of the voltage swing respectively. The condition for turnoff is:

$$\begin{aligned} V_{sg} &< V_t \\ V_{dd} - V_{ph} &< V_t \\ V_{dd} &< V_{ph} + V_t \end{aligned}$$

For conduction to occur:

$$\begin{aligned} V_{sg} &> V_t \\ V_{dd} - V_{pl} &> V_t \\ V_{dd} &> V_{pl} + V_t \end{aligned}$$

From (1), substituting $\Delta V_{gatep}=V_{ph}-V_{pl}$ and $\Delta V_{in}=V_{dd}$,

$$V_{pl} = \frac{V_{ph}(C_{boot} + C_p) - C_{boot} \cdot V_{dd}}{C_{boot} + C_p}$$

Combining the conditions for both turnoff and conduction, the power supply voltage is governed by

$$\frac{C_{boot} + C_p}{2C_{boot} + C_p} \cdot (V_{ph} + V_t) < V_{dd} < V_{ph} + V_t$$

The expression shows that the lower operating limit of the supply voltage is strongly dependent on the relative capacitance between the bootstrap capacitor C_{boot} and the capacitance at the gate node C_p . A higher C_{boot} allows the logic to operate at a lower voltage. Thus the BCMOS logic is able to operate at voltages below the threshold level allowed by the technology.

5 Performance of BCMOS

BCMOS has superior driving capability compared to conventional MOSFETs. Figure 4 shows the simulated conduction characteristics of the BCMOS and conventional MOSFET. The conductance of BCMOS is an order of magnitude higher than a standard MOSFET at 1V. The BCMOS curve is identical to the MOSFET curve except that it is shifted to the left by approximately 0.5V. The driving capability of BCMOS is better than the Double Gate Driven MOSFET (DGMOS [4]) because DGMOS only improves the drive capability of the pMOS transistor. BCMOS is the first reported technique that is capable of operating digital circuits at voltages below its threshold level in bulk CMOS.

In the off state, the gate-source voltages of the pMOS and nMOS devices are maintained at about 0.6V. The devices are in the weak inversion mode and subthreshold currents flow. This accounts for the higher leakage current, which is about 2 orders of magnitude higher than a conventional MOSFET (see Figure 4). This leakage current is negligible if the logic has a high activity factor.

6 Experimental and Simulation Results

An 11-stage ring oscillator was implemented in both BCMOS and standard MOSFET to compare the delay with varying V_{dd}. The circuits were extracted from layouts and simulated with MOSIS 1.2u process parameters. The results are presented in Figure 5. At 1V, the delays of the BCMOS and MOSFET are 12.7ns and 59ns per stage respectively. The BCMOS is about 5 times faster than the conventional logic. The tradeoff is an increased current consumption of slightly more than twice.

To demonstrate the effectiveness of BCMOS, a 21-stage ring oscillator was also fabricated in 1.2u nwell CMOS process. The double-poly double-metal process has threshold voltages of 0.98V and 0.97V for the nMOS and pMOS respectively. The delay over a range of operating voltages are plotted in Figure 5. The ring oscillator was able to operate down to only 0.9V because of the limited size of the bootstrap capacitors (100fF). The bootstrap capacitors were implemented with poly1-poly2 layers. The diodes were constructed by making a p+ diffusion in an nwell. A micrograph of the ring oscillator is shown in Figure 6.

7 Conclusion

A bootstrap approach to increase the current conduction of digital circuits at low voltages is presented. The technique employs a coupling capacitor to shift the gate voltage to obtain a larger source-gate potential for higher drive capability. An analysis of the relative capacitances in the circuit and their effect on the voltage supply showed that the BCMOS is able to operate at voltages below the threshold level. A ring oscillator fabricated confirmed its low voltage capability. Simulations show that the BCMOS is approximately 5 times faster than a conventional MOSFET at low voltage.

References

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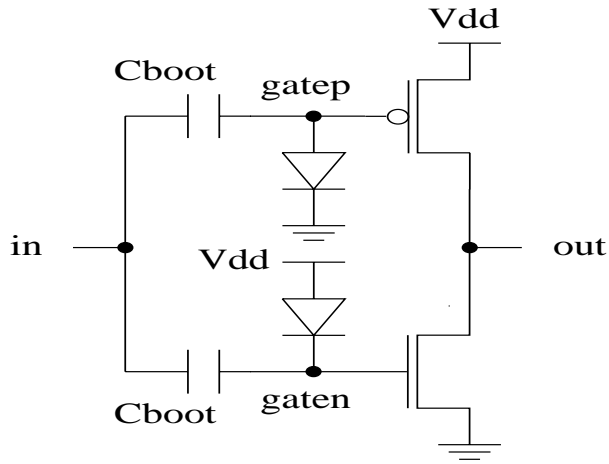


Figure 1: Bootstrapped CMOS inverter.

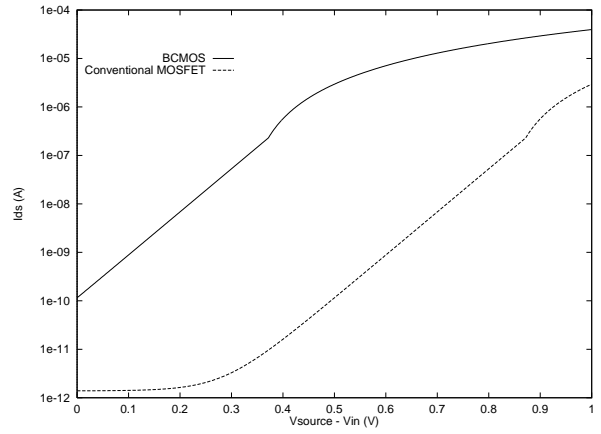


Figure 4: Conduction characteristics of BCMOS and MOSFET.

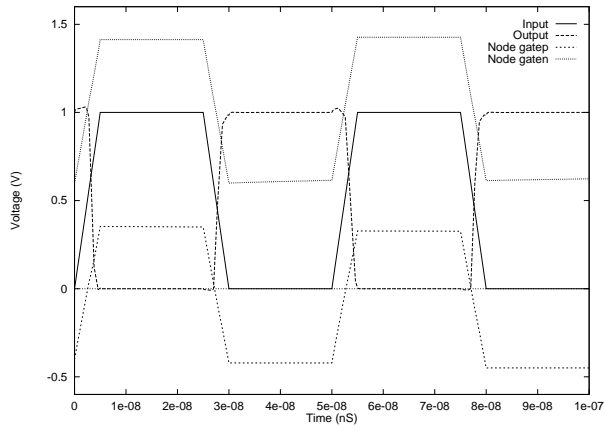


Figure 2: Waveforms of input, output, nodes gatep and gaten of BCMOS.

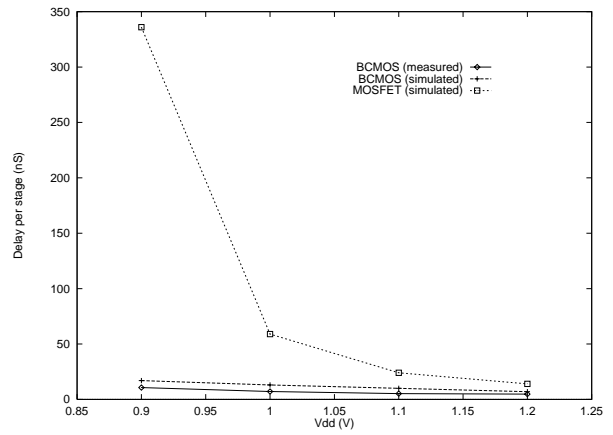


Figure 5: BCMOS and MOSFET ring oscillator delay.

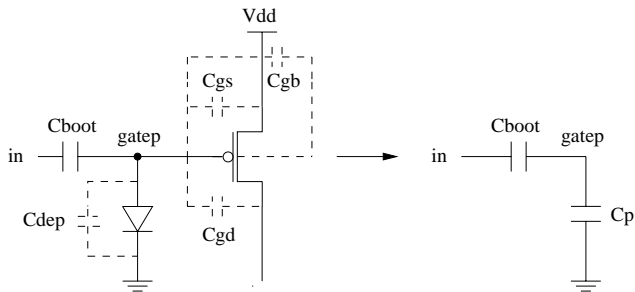


Figure 3: Capacitances at the gate node.

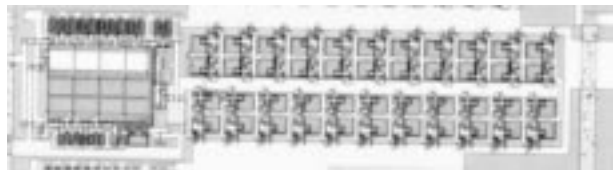


Figure 6: Micrograph of 21-stage ring oscillator.