A Fully-Integrated FM Discriminator for RDS Applications

A. Nitescu-Henry([1]), F. Op't Eynde([2]), S-A Spanoche([3]), D. Claudius ([3]), S-M Popescu ([3])
([1]) *Institut d'Electronique et Microélectronique du Nord,*
ISEN Department, Villeneuve d'Ascq, France
([2]) *Mixed Silicon Structures, Roubaix, France*
([3]) *"Politechnica" University of Bucharest,*
Laboratory of Microelectronic Systems, Bucharest, Romania

Abstract: A fully-integrated low-power FM discriminator, intended for RDS pager applications, is presented. The discriminator is based on the quadrature demodulation principle. The input signal carrier frequency is 0.988 MHz. The circuit features are a large linearity range, a good harmonic distortion and IM3 behaviour and a signal-to-noise ratio compliant with the RDS requirements.

I. Introduction

Traditionally, FM discriminators were implemented either as a quadrature demodulator with a discrete tuned circuit [1], or as a PLL with a quartz filter. Due to the need for external discrete components, it was obligatory to follow the de-facto standard of 10.7 MHz for the intermediate frequency. The current tendency to increase the degree of integration of radio receivers leads to a need for fully-integrated FM discriminators, without any external components. In previous work, several solutions for FM discriminators are presented, including a counting discriminator implemented in a digital form [2], and fully-integrated PLL circuits. Also, solutions for narrow-band FM have already been presented [3]. In this paper, a low-power mixed-analog-digital realisation of an FM discriminator is presented, intended for demodulating standard FM broadcasting radio signals with a 220 kHz bandwidth. The circuit is optimised for RDS pager applications.

Since for a fully-integrated radio receiver, the intermediate frequency is not determined by a limited choice of standardised external components, this intermediate frequency can be optimised towards a lower value, hereby facilitating the integration of the FM discriminator and of the IF bandpass filter. On the other hand, in standard superheterodyne receivers, reducing the IF will render the realisation of the image-rejection filter more complex.

In Section II of this paper, the principle of a quadrature FM discriminator is recalled. Section III presents the practical realisation of a fully-integrated frequency demodulator, intended for an intermediate frequency of 1 MHz. Experimental results are shown in Section IV.

II. The quadrature discriminator principle

The basic principle of a quadrature FM discriminator is presented in Figure 1.

A frequency modulated signal can be expressed as follows:

$$v_{FM}(t) = A \cdot \sin\left(\omega_c t + \frac{\Delta f}{f_m}\sin\omega_m t\right) \tag{1}$$

where $\omega_c = 2\pi.f_c$ is the carrier angular frequency, $\omega_m = 2\pi.f_m$ is the baseband modulating angular frequency and Δf is the maximum FM frequency deviation. For a standard broadcasting FM signal, ω_c is the FM intermediate carrier frequency. f_m covers the baseband between 50 Hz and 60 kHz. The total frequency deviation Δf can be up to ±75 kHz.

The instantaneous frequency of (1) is: $f_{inst} = \frac{d\phi(t)}{dt} = f_c + \Delta f \cdot \cos\omega_m t$. (2)

The quadrature discriminator contains a frequency-dependent phase shifter, introducing a

phase shift that is varying linearly with frequency for instantaneous frequencies around the center frequency f_c. For an instantaneous frequency equal to f_c, the phase shift is -90°.
In a mixer, a multiplication is performed on the two quadrature signals. This function may be implemented with a classical Gilbert mixer. The resulting signal contains the desired demodulated FM signal, plus a strong parasitic signal containing a component around the double of the IF frequency and a DC component. This parasitic signal can be eliminated by appropriate filtering.

III. The practical realisation of the FM discriminator

The block schematic of the presented FM discriminator is given in Figure 2. The structure is implemented in a fully-differential form. The input signal is frequency-modulated around a 0.988 MHz IF carrier.
The FM input signal is applied to an amplifier-limiter permitting the elimination of all spurious AM modulation. The resulting square-wave signal is further applied to a delay element, hereby introducing a frequency-dependent phase shift. The original and delayed signals are then multiplied by a fully-balanced Gilbert cell. Subsequent filtering by several cascaded RC lowpass filters allows to reduce the spurious signal around the double of the carrier frequency (2*0.988 MHz).
In order to obtain an accurate 90° phase shift at 0.988 MHz, the delay introduced by the delay element has to be equal to one-quarter of a 988 kHz signal period. To control this delay, a master-slave system is built with a separate Phase Locked Loop. This PLL contains a ring-oscillator VCO constructed with two delay elements. This VCO is oscillating at 0.988 MHz. The VCO control voltage is tuned by the PLL loop in such a way that each of the delay cells is introducing a quarter-period delay. By replica biasing, the delay element in the signal path is controlled simultaneously.
In the presented design, each delay element is realised as a bi-stable structure shown in Figure 3. The delay can be controlled by the differential pair tail current.
In order to improve the matching between the discriminator and the controlling PLL, a careful layout for the three delay cells is mandatory. The delay cell for the signal path is placed common-centroid in between the two VCO delay cells. All output connections need to present the same parasitic capacitance.
Since the PLL is controlled by a 38 kHz reference signal, the 0.988 MHz VCO output frequency is divided by 26. Resulting spurious signals at 38 kHz and 76 kHz are at frequencies were no signal information is present.
The PLL phase-and-frequency comparator and the frequency divider are the only digital structures in the discriminator.
In Figure 4, the Gilbert multiplier schematic is shown. Since the tail current of the OTA is derived from a bandgap reference, the output signal amplitude is well-controlled and independent of the supply voltage. The discriminated baseband output signal (also denoted as multiplex signal « MPX ») is obtained at the output of an RC lowpass-filter output buffer.

IV. Measurement results

The FM discriminator is realised in a double-poly 0.8μm BiCMOS process. A die photograph is shown in Figure 5. The circuit size equals 1.12 mm^2 and the power consumption is 350 μA for a supply voltage of 2.5 V. The main measurement results are summarised in Table 1.
In Figure 6, the discriminator MPX output voltage is depicted as a function of the input signal frequency. This curve is generally known as the discriminator « S-curve ». The discriminator presents a linear frequency range of almost ± 300 kHz centred around the 988 kHz IF

frequency. This is more than sufficient for radio broadcasting applications with frequency variations of maximum ± 75 kHz.
In Figure 7, the measured discriminator frequency characteristic is shown. Over a frequency range of 57 kHz, the gain variation is 0.7 dB.
Since the presented discriminator is primarily intended for RDS applications, a good linearity is mandatory. Indeed, due to circuit nonlinearities, large signal components in the audio band could create signal harmonics or intermodulation products around 57 kHz, hereby perturbing the RDS information that is present in this frequency band. In order to verify this, the output spectrum is measured for an FM input signal modulated by a 9 kHz sinusoidal baseband signal with maximum amplitude. The measurement results are shown in Figure 8. The measured second and third harmonic distortions are below 58 dB and 60 dB respectively. The output signal noise floor is at 14 $\mu V/\sqrt{Hz}$, which corresponds to an SNR of 20 dB in the RDS band.

V. Summary

A fully integrated FM demodulator is presented, featuring a good frequency linearity, a very performant harmonic distortion and IM3 product, and a Signal-to-Noise ratio suitable for RDS applications. The circuit is operating with a 2.5 V supply voltage and has been designed in a standard 0.8 µm BiCMOS technology.

VI. Acknowledgement

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VII. References

[1] Philips Semiconductors, TDA7000 data sheet, 1991
[2] Rahkonen, T., *et al.*, "A Digital FM Demodulator Chip Based on Measurement of IF-Signal's Period", Proceedings of the 1995 ESSCIRC, Lille, pp. 102
[3] Pardoen, M., *et al.*, "A 0.9V 1.2mA 200MHz BiCMOS Single-Chip Narrow-Band FM Receiver", Proceedings of the 1996 IEEE ISSCC, pp. 348

Measured parameter	Value	Measurement conditions
MPX output amplitude	360 mV	f_c = 988kHz, Δf = 75kHz
MPX output THD	-50 dB	f_c = 988kHz, f_m = 9kHz, Δf = 75kHz
MPX output SNR (band: 0 to 100 kHz)	34 dB	f_c = 988kHz, Δf = 75kHz
MPX output SNR (band: 0 to 15 kHz)	45 dB	f_c = 988kHz, Δf = 75kHz
MPX output SNR (band: 54.5 to 59.5kHz)	20 dB	f_c = 988kHz, Δf = 4kHz
IM3 product	-40 dB	f_c = 988kHz, Δf_{total} = 75kHz
output parasitic signal @ 988 kHz	10 mV	f_c = 988kHz, Δf = 75kHz
output parasitic signal @ 2 MHz	640 µV	f_c = 988kHz, Δf = 75kHz

Table 1: The measured FM discriminator characteristics

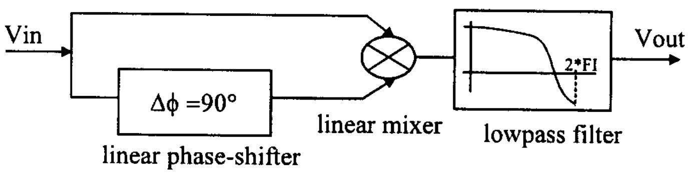

Figure 1. The basic principle of a quadrature FM discriminator

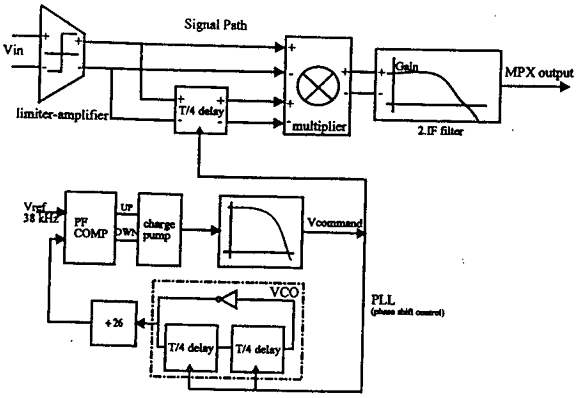

Figure 2. The block schematic of the presented FM discriminator

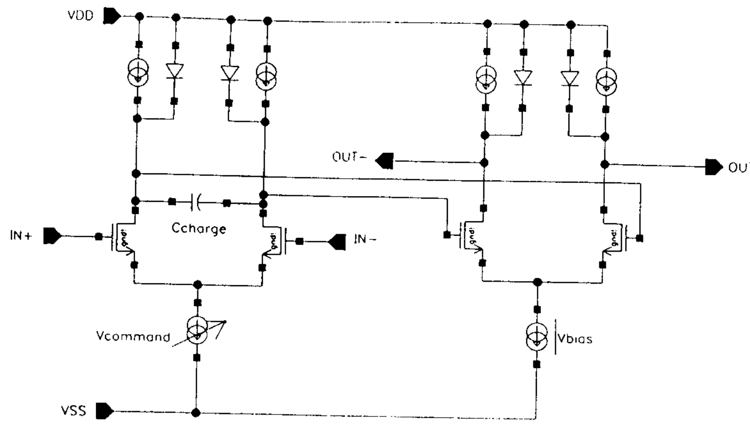

Figure 3. The structure of a delay element

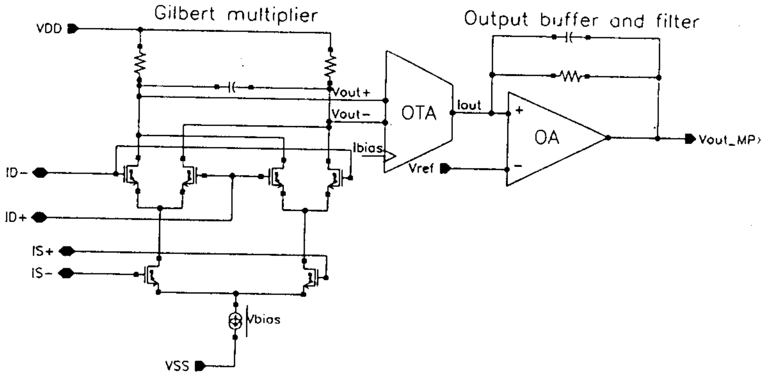

Figure 4. The Gilbert multiplier and output buffer schematic

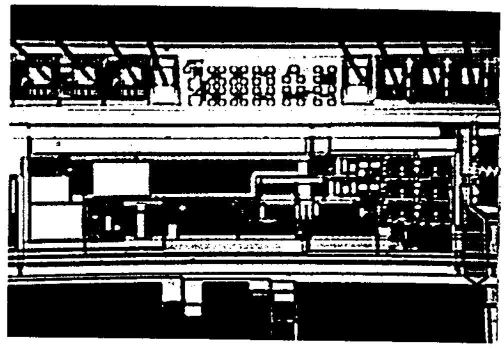

Figure 5. A die photograph of the presented FM discriminator

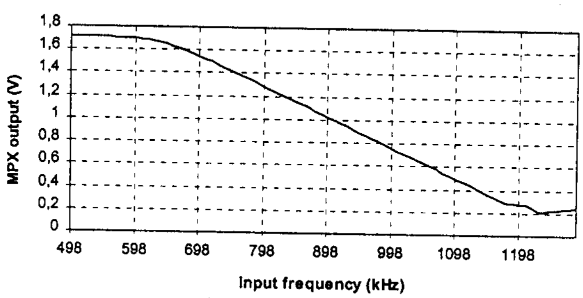

Figure 6. The measured discriminator "S-curve"

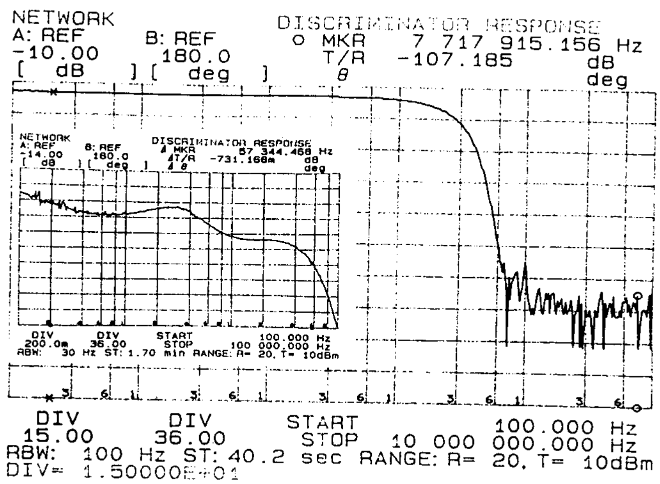

Figure 7. The measured discriminator frequency characteristic

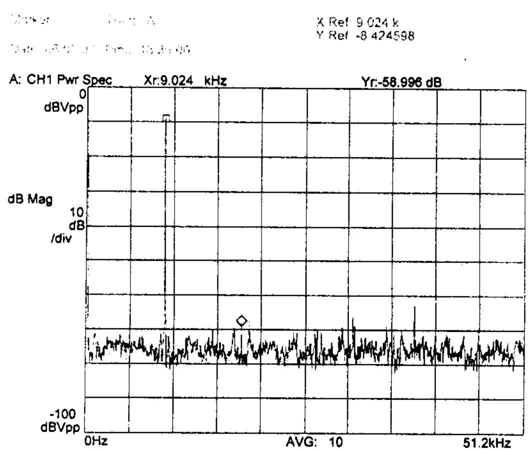

Figure 8. The measured output spectrum for an FM input signal modulated by a 9 kHz baseband wave