

10 Gb/s Single-Chip Data Regeneration with an Injection Synchronised Ring Oscillator and an Automatic Phase Adjustment

Z.-G. Wang, A. Thiede, M. Rieger-Motzer, A. Hülsmann,
B. Raynor, J. Schneider, T. Jakobus, and M. Schlechtweg

Fraunhofer-Institute of Applied Solid-State Physics

Tullastr. 72, D-79108 Freiburg, Germany

Tel.: +49 761 5159 533, Fax: +49 761 5159 565

Abstract: A new concept of high-speed data regeneration was developed by using an injection-synchronised narrowband ring oscillator for the clock recovery and an automatic phase adjusting loop for the optimum data decision. A single-chip data regeneration IC has been realised by using our 0.3 μm gate-length QW-HEMT GaAs technology and characterised on-wafer at STM-64 level (~ 10 Gb/s) of the SDH-standard. Even with a 100 mV, jittered input data signal, high-quality clock and data signals were regenerated. The recovered clock has an amplitude of 280 mV, a rms time jitter of 2.5 ps, and a phase noise of -88.5 dBc/Hz at 10 kHz offset. The regenerated data show fully open eyes with a height of >200 mV. The 1.5×1.5 mm² IC can be operated with a single supply voltage of -3 V with a dc consumption of about 300 mW.

Introduction: Besides the accuracy, the simplicity and the compatibility of digital systems, one advantage of the digital communication is that during and after the transmission a digital signal or a data stream can be regenerated many times with a very small error rate in the repeaters of the branches and in final receivers. The noise and other distortions from branches and circuits can be removed. The data regeneration is, in fact, an excellent feature of the digital communication.

The data regeneration generally includes two basic functions: the clock recovery (CR) used to obtain a clock signal which is synchronous with the input data signal, and the data decision (DEC) used to make a retiming and an amplitude discrimination of the same data signal. For the first function we have developed a concept using a narrowband regenerative frequency divider (NRFD) [1]. With that concept a series of ICs were successfully realised for SDH-based systems at STM-64, 2 \times STM-64, and 4 \times STM-64 levels [2-4]. For the DEC we have realised various ICs for bit rates exceeding 40 Gb/s [5]. Since the same input data signal is operated by both CR and DEC, and in the DEC the data should be decided in favourable time slots defined by the recovered clock signal, these two functions are best treated in one sub-system and realised on a single chip. For this reason we have realised a monolithic IC

including both of the CR- and the DEC-function [6]. One imperfection of the IC is that the phase of the recovered clock signal can only be adjusted manually. In this paper we report our first single-chip data regeneration using an injection-synchronised narrowband ring-oscillator and an automatic phase adjusting (APA) loop.

Block Diagram and Principle: Fig. 1 shows the block diagram of the single-chip data regeneration IC. It mainly consists of four function groups: the input buffer, the CR-branch, the DEC-branch, and the APA-loop. The input buffer includes a stage of broadband amplifier. The CR-branch includes the pre-processor, the injection-synchronised ring-oscillator composed of summing and narrowband amplifiers, the phase shifter, and the output buffer. The DEC-branch consists of two input buffers for the data and the clock signal, two D-latches forming a master-slave D-flip-flop, and one output buffer. The APA-loop consists of the phase shifter and the output buffer of the CR-branch, the clock input buffer and both D-latches of the DEC-branch, two XOR logic cells and an active low-pass filter consisting of an operational amplifier and a feedback RC network.

At first, the input data signal is split into the CR- and the DEC-branches by the input buffer. In the pre-processor of the CR-branch the data signal is processed in such a manner that in the output signal a strong spectral line is generated at the bit frequency f_b of the data signal. The signal is then injected to the narrowband ring oscillator which is designed with a specified centre frequency $f_0 = f_b$. In result, a high-quality clock signal is generated. In the presented IC there is $f_0 = f_b = 10$ GHz.

The recovered clock signal is used to regenerate the data signal. If the decision was made always at the eye centre of the data signal, the regenerated data would have the lowest bit error rate. This optimum condition is maintained by the APA-loop. Since two XOR logic cells build up a phase detector [7], the resulting output voltage represents the phase difference between the input data and the clock signal. Thus, the APA-loop is equivalent to a PLL. By means of the automatic control function of the loop, the phase of the clock signal vs. the data signal will lie continuously at the optimum location.

In the past, injection-synchronised oscillators were seldom used for the clock recovery in digital transmission systems. This might be caused by two problems: i) no suitable oscillator; ii) no suitable technique to correct the static phase error of such an oscillator. In our IC these problems were solved by using a fully-balanced injection-synchronised narrowband ring oscillator* and by introducing the APA-loop. One advantage of this system, against the CR using an NRFD [1], is that the circuit can be simply optimised because of the identically-specified centre frequency of all resonators in the pre-processor, the ring-oscillator and the phase-shifter. This advantage can also be used to optimise the pre-processor in the CR using an NRFD.

Circuit Techniques: Many cells of our realised ICs were utilised for the design of this IC. The LC loop in the 20-to-10-GHz NRFD [2, 3, 6] was especially useful since its centre frequency has met the specified value of 10 GHz. Fig. 2 shows the circuit diagram of the summing amplifier at the front of the ring oscillator. It can be considered as a pair of parallel connected current amplifiers with a common LC resonator as loading circuit. In comparison with the

* patent pending.

tuned amplifier in [2], the tuning part was improved: The drains of EF₅₋₆ are connected to the sources of DF₅₋₆ and the diode D₀ is replaced by EF₇₋₈. At the gates of DF₅₋₆ as well as EF₇₋₈, a high ohmic resistor is shunted and an external voltage can be applied. This improvement brings about two advantages: high impedance to the controlling circuit and the possibility of differential control. The identical LC loop and tuning part was used in all the pre-processor, the narrowband amplifier in the ring oscillator and the phase shifter.

One feature of the IC is that all sub-circuits, inclusive of the active filter, have a balanced structure.

Fabrication: Fig. 3 shows the chip photograph of the 1.5×1.5 mm² IC. For the fabrication the same process as for all ICs in [2-6] was used. The 0.3 μm gate length QW-HEMTs show a transit frequency f_T of ~50 GHz. The two-layer metallization with air-bridges was used for the realisation of the inductors.

Measurement Results: The IC was tested on wafer using two SSGSS- (S: signal, G: ground) and two GSGSG-type 50-Ω coplanar probes. The dc current is about 100 mA at -3 V supply voltage, corresponding to a dc consumption of 300 mW. Fig. 4 shows one measured eye diagram. The input data signal had an amplitude of only 100 mV_{p-p}. Even for such a small input signal with almost closed eyes, both the clock signal and the data signal were well regenerated. The amplitudes of each single-ended regenerated clock and data signal are 280 and 225 mV, respectively. Fig. 5 shows the plot of the phase noise of the recovered clock signal in the frequency range from 10 Hz to 1 MHz off the carrier. The noise levels at 0.1, 1, 10, 100 and 1000 kHz are -63, -83, -89, -107 and -124 dBc/Hz, respectively, better than those in [3]. The peak-to-peak and the rms value of the time jitter are 16 and 2.5 ps, respectively. Some chips functioned at the desired bit rate of 9.95328 Gb/s without any adjustment and kept in lock even when the supply voltage was varied from -3 to -5.2 V. The in-lock frequency range was > 100 MHz. All these results show that our circuit concept is feasible and the realised IC is applicable to SDH-based systems.

Conclusions: A single-chip data regeneration IC has been realised by using our 0.3 μm gate-length QW-HEMT GaAs technology. It is featured by the complete function, the high speed (10 Gb/s), the high sensitivity (100 mV), the low voltage (-3 V) and the low power (300 mW). It can be directly used in an SDH-based system at STM-64 level. It demonstrates that an injection-synchronised narrowband ring oscillator can be used for the clock recovery, and an automatic phase adjusting loop is effective for an optimum data regeneration. The same concept can be adopted for the IC design at higher bit rates.

Acknowledgement: We are grateful to G. Weimann for his support and encouragement and to the German Federal Ministry of Education and Technology for financial support.

References:

- [1] Z.-G. Wang and M. Berroth, German Patent, No. 43 38 873
- [2] Z.-G. Wang et al., Dig. of Tech. Papers of ISSCC'96, pp. 204-205, 1996
- [3] Z.-G. Wang et al., Electron. Lett., vol. 32, pp. 1498-1500, 1996
- [4] Z.-G. Wang et al., Electron. Lett., vol. 32, pp. 2081-2082, 1996
- [5] Z.-G. Wang et al., Electron. Lett., vol. 32, pp. 1855-1856, 1996
- [6] Z.-G. Wang, et al., Proc. of ESSCIRC'94, pp. 176-179
- [7] C.R. Hogge, Jr., IEEE Tran. on Electron Devices, vol. 32, pp. 2704-2706, 1985

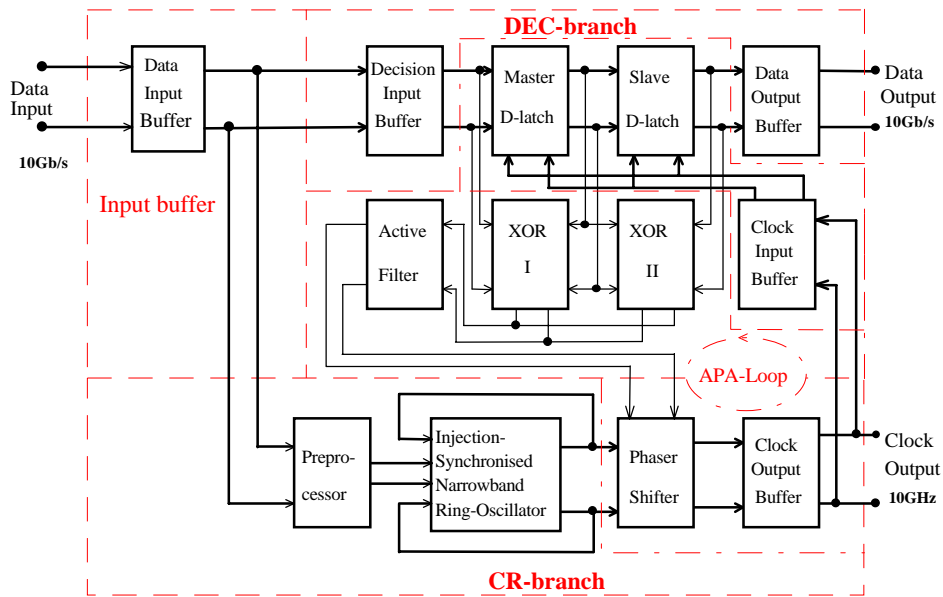


Fig. 1 Block diagram of the 10 Gb/s data regeneration IC using an injection-synchronised ring oscillator and an automatic phase adjustment loop

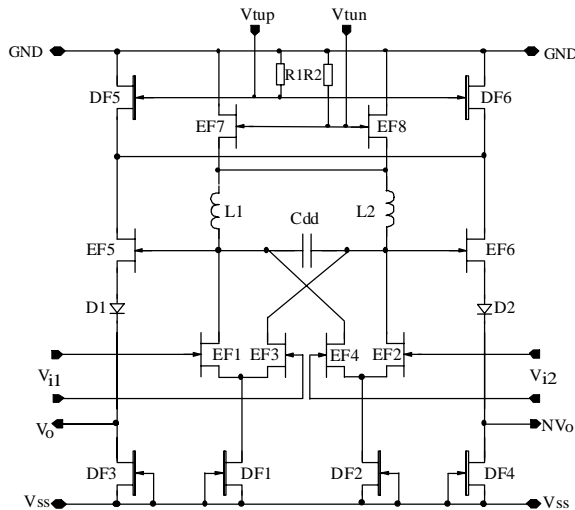


Fig. 2 Circuit diagram of the narrowband summing amplifier

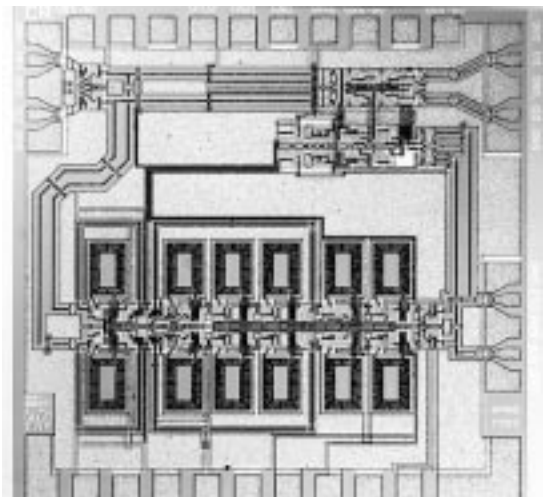


Fig. 3 Chip photograph of the single-chip 10 Gb/s data regeneration

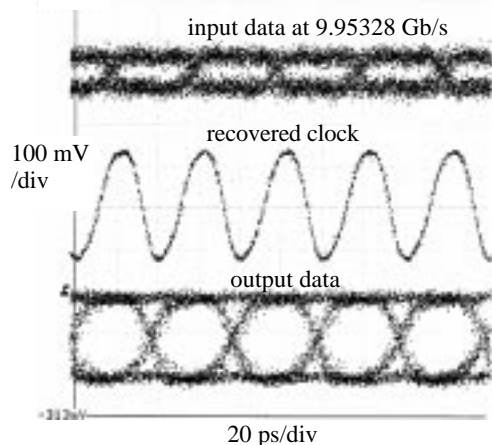


Fig. 4 Eye diagram of the input data signal, regenerated clock and data signal

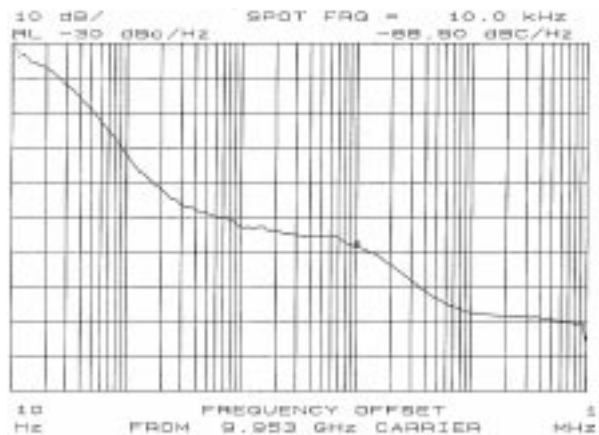


Fig. 5 Phase noise of the recovered clock signal at the carrier of 9.95328 GHz