A Low Noise Folded Bit-line Sensing Architecture for Multi-Gb DRAM with Ultra High Density $6F^2$ Cell

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Abstract

A new low noise sensing architecture for $6F^2$ DRAM cell is presented, employing two noise reduction methods; Divided Sense and Combined Restore Scheme and Noise Absorbing Scheme which eliminate word line to bit line coupling noise and bit line to bit line coupling noise, respectively. The new sensing architecture reduces bit line noise to less than 15% of a conventional scheme with only 0.2% area overhead. The $6F^2$ cell enables the giga bit DRAM to have about 85% chip area of conventional DRAM. The measurement results of the fabricated test chip show stable DRAM operations and the proposed sensing scheme is useful in multi-giga bit DRAM.

1. Introduction

As the advent of giga-bit DRAM, the demand for small cell area ever increases. $6F^2$ cell shown in figure 2 has been reported to be the smallest cell in COB(capacitor over Bit-line) or shielded bit line(BL) architecture[1]. COB structure is widely known to have small *BL* noise. However, the incorporation of $6F^2$ cell into COB was possible only through open *BL* sensing architecture of which low sensing margin limits its application to the practical DRAM. Several *BL* sensing schemes have been proposed for high noise immunity in $6F^2$ DRAM cell only to achieve partially folded bit line sensings[2, 3].

There are two different cell array noises; *Word-line(WL) to Bit line(BL) coupling noise*, δc and *BL to BL coupling noise*, δb[4]. The former is known to be canceled by using folded *BL* sensing architecture. But the *BL* to *BL* coupling noise becomes more dominant as the critical dimension decreases with the integration scale of DRAM. Different methods have been reported for the *BL-BL* coupling noise reduction for conventional DRAM, but not for the $6F^2$ cell DRAM[5, 6]. In this paper, a new sensing scheme for $6F^2$ cell arrangement is proposed to reduce not only *WL* to *BL* coupling noise but also *BL* to *BL* coupling noise. Its fully folded *BL* sensing operation cancels *WL* to *BL* coupling noise and its new noise absorbing scheme reduces *BL* to *BL* coupling noise. Each scheme is described in section 2 and 3, respectively and its application to low noise high density DRAM and the measurement results are discussed in section 4.

2. Divided Sense and Combined Restore Scheme for $6F^2$ cell

Figure 1 shows the diagram of Divided Sense and Combined Restore (DSCR) Scheme which makes the full folded *BL* sensing possible for $6F^2$ cell. The $6F^2$ cell array is composed of two cells and one isolation as shown in figure 2. Three *BL*'s are connected to two sense amplifiers which are located at both side of cell array through the bit line selection switches (*BSi*). Each long *BL* is divided into two short sections by bit line sharing switches (*SSi*).

The data read operation is shown in figure 3. With all *SSi* turning on, *BL0, BL1, BL2* are connected to *BL4,BL5,BL3* to form long *BL*'s, *BL0-BL4, BL1-BL5, BL2-BL3,* respectively. If *WL0* goes high to access *cell A* and *B*, their charge is shared with *BL0-BL4* and *BL1-BL5*, respectively. After the charge sharing, all *SSi* turn off to divide long *BL* into short *BL*'s. The folded *BL* sensing between *BL1* and *BL2* pair and between *BL3* and *BL4* pair are possible because the *BL2* and *BL3* have half Vcc reference voltage. Once the *BL* sensing is completed, *SS1* and *SS2* connects *BL4* to *BL0* and *BL1* to *BL5* to make long *BL*'s. The restoring operation for *cell A* and *B* can be performed by amplifying the voltage differences between Long *BL0-BL4* and short *BL2* pair and between *BL1-BL5* and *BL3* pair, respectively, without performance degradation because the critical sensing operation is already completed. Its timing diagram is shown in figure 3(b). The voltage bouncing on *BL1* and *BL4* comes from the charge sharing between full rail-to-rail amplified *BL1*, *BL4* and half Vcc charged *BL0, BL5*. Since the sense amplifier are in its fully activated state, the voltage bouncing is rapidly removed. Figure 4 shows the simulated waveforms for read and restore operation. *Cell B* or *'H'* is concurrently sensed and restored while *Cell A* or *'L'* is restored after the sensing. The fully folded *BL* sensing of DSCR scheme can enhance the sensing margin compared with previous partially folded *BL* sensing schemes[2, 3]. In addition, a fast sensing can be obtained because only half bit line capacitance is attached to sense amplifier during sensing operation.

3. /*BL* Noise Absorbing Scheme for coupling noise reduction

Noises δc and δb are induced on /*BL* during *WL* activation and charge sharing between *BL* and cell, respectively, as shown in figure 5. The effect of δc can be removed by folded *BL* sensing because it is equally induced on both *BL* and /*BL*. But δb of /*BL* makes sensing signal worse from Vs to Vs - δb. In giga scale DRAM, *BL* to *BL* coupling capacitance has comparable value to *BL* capacitance itself, much larger than *WL* to *BL* coupling capacitance[7]. The difficulty in achieving the high noise margin in sense amplifier comes from the fact that only δb has to be suppressed while δc remains intact. This is because sensing signal ΔV for data 'L' is degraded to be Vs - δc although for data 'H' it is improved to be Vs + δc if both the δb and δc are removed from /*BL*.

Figure 6 is the schematic diagram of the proposed /*BL* Noise Absorbing Scheme. It ties several /*BL*'s together for short time to cancel δb out after *WL* activation. Although all /*BL*'s induce the same δc caused by the *WL* activation, they have random noises of +δb or −δb because the stored data of each cell has random distribution of '0' and '1'. When many /*BL*'s are connected together right after *WL* activation, δb on */BL* is canceled out each other or decreases while the δc of each /*BL* does not change. Average δb on /*BL* after noise absorbing operation can be calculated as shown in figure 7 if assumptions are made that +δb or −δb has the same probability, 1/2, and enough /*BL*'s are connected. When 400 of /*BL*'s are shorted together, the noise decreases to less than 15% of conventional folded BL sensing architecture. This gives lower noise than double TBL scheme that was reported to have 16.7% noise of conventional scheme with the area overhead of around 7%[5]. The area overhead of the new scheme is negligible because only two transistors are added as switches for /*BL* connection. Its speed penalty can be compensated by the fast sensing operation of the DSCR scheme.

4. Test chip fabrication and measurement

Test Chip is fabricated using 0.3μm, 5 ploysilicon 2 metal triple well CMOS process technology of 256M DRAM. 2Kb-cell area of test chip is 1,600 μm^2 which is only 76.2% of that in [8]. The proposed architecture enables giga scale DRAM to have 25% smaller cell array area, 0.1% area overhead for sharing/control switches and 0.05% area overhead for noise absorbing. Total area reduction amounts to around 14.8% of conventional DRAM.

Figure 8 shows a photomicrograph of test chip and its measurement result. The falling edge of *WL* control signal enables a *WL* and the falling edge of *BL* control signal selects one sense amplifier to connect the sensed data to output DQ. Data read from and write to the $6F^2$ cell are observed to be stable with DSCR and noise absorbing schemes.

5. Conclusion

A new low noise sensing scheme for $6F^2$ cell arrangement is developed for high cell density in giga-scale DRAM. The proposed architecture has two noise reduction methods; Divided Sense and Combined Restore scheme for the *WL* to *BL* coupling noise reduction and /*BL* Noise Absorbing scheme for the *BL* to *BL* coupling noise reduction. The noise can be reduced to less than 15% of conventional folded *BL* sensing with only 0.2% area overhead. The $6F^2$ cell reduces the DRAM chip area to 85.2% of conventional DRAM's. A test chip is fabricated and measured to demonstrate that the proposed architecture is applicable to the low noise multi-giga bit DRAM.

References

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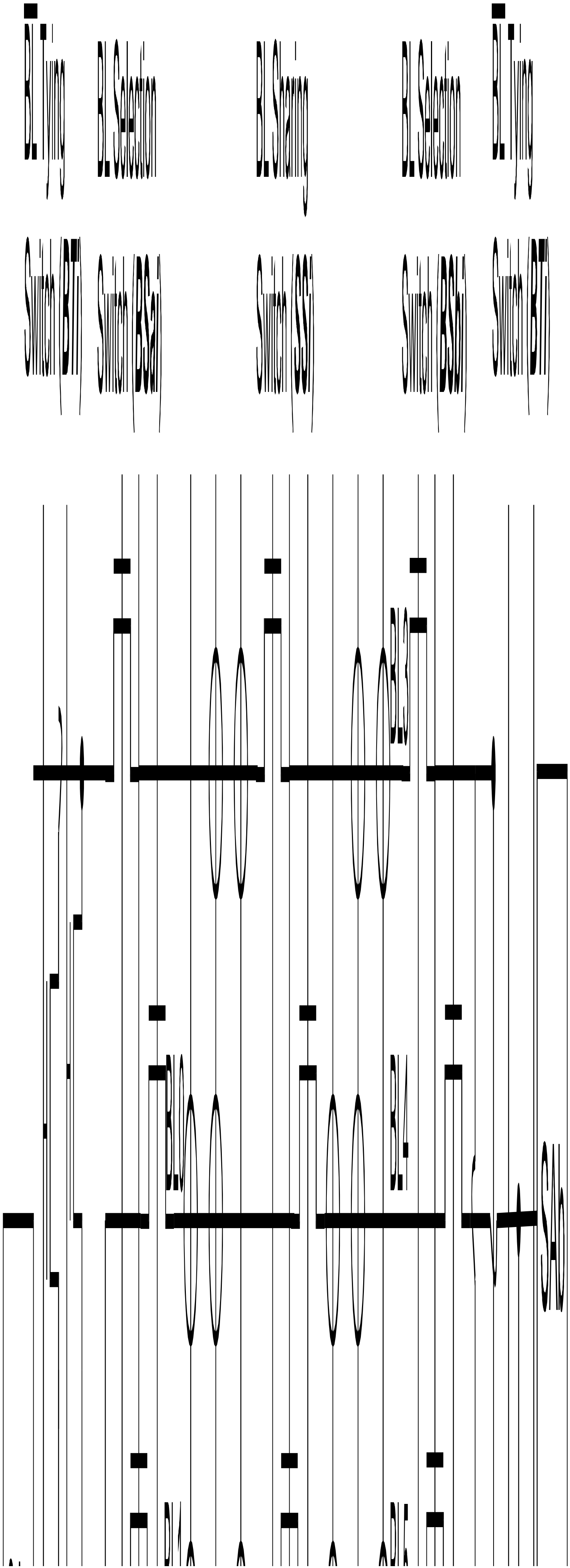

Fig. 2. Cell Layout of 6F^2 cell

(a) Read Operation

(b) Timing Diagram

Fig. 3. Schematic View of Read Operation

Fig. 4. Simulated Waveforms

Fig. 5. Voltage Waveforms of Bit Lines

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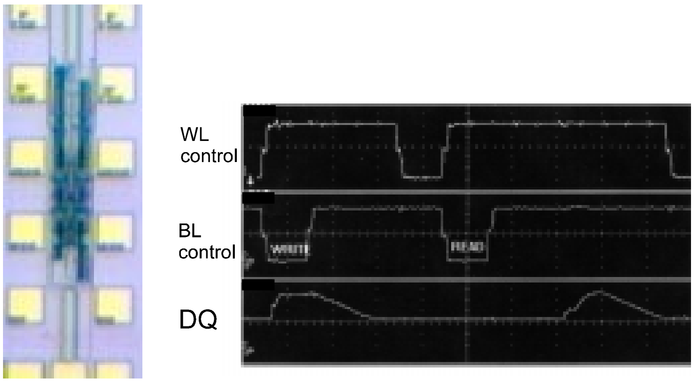
Fig. 6. /BL Noise Absorbing Scheme

Fig.7. Calculation of δb in /BL Noise Absorbing Scheme



(a) (b)

Fig. 8. Fabrication of T/C. (a) microscope of T/C and (b) measurement