

Embedded 5V-to-3.3V Voltage Regulator for Supplying Digital ICs in 3.3V CMOS Technology

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Abstract

A fully-integrated 5V-to-3.3V supply voltage regulator for application in digital ICs has been designed in a 3.3V 0.5 μ m CMOS process. The regulator is able to deliver peak current transients of 300mA while the output voltage remains within a margin of 10% around the nominal value. The circuit draws a static quiescent current of 1mA during normal operation and includes also a power-down mode with only 12 μ A current consumption. The die area is 1mm² and can be scaled proportional to the maximum peak current. Special precautions have been taken to allow 5V in the 3.3V process.

Introduction

Today, many IC designs are being converted from 5V technology (0.8 μ m CMOS and larger) to 3.3V technology (0.5 μ m/0.35 μ m CMOS) or to processes with even lower maximum voltages in the future. However, a 5V supply voltage and 5V I/O are still desired for many system applications. In order to allow 5V operation in 3.3V CMOS without 'high-voltage' technology options some additional embedded circuitry is required as shown in figure 1. The external 5V VDDD is connected directly to a supply voltage regulator and I/O cells. The digital core operates at 3.3V \pm 10% generated by the regulator. For being compatible with existing 5V ICs there's not always an IC pin available for external decoupling of the internal 3.3V supply. Therefore the regulator itself must be able to deliver the stable and accurate internal supply voltage without using an external capacitor while large and steep supply current peaks are drawn by the digital core circuitry. In order to be compatible with external supplies of 5V, 3.3V or anything between, the regulator has to operate correctly for VDDD values of 5.5V down to 3.0V which puts constraints to the drop voltage of the regulator. Since the regulator and I/O cells are designed in 3.3V technology and operate at 5V directly, circuit techniques must be used to prevent these circuits from breakdown.

Previously published embedded regulator circuits are found to be unsuited for this application. These circuits, all designed for voltage reduction in RAM ICs, are too inaccurate, assume a huge internal capacitor and require quite smooth and/or known supply currents [1,2,3,4,5]. Furthermore stability of some depends on the load [3,5] and some have a large voltage drop [2,4]. The fully-integrated series regulator in 0.5 μ m 3.3V CMOS described in this paper overcomes these problems and fulfils the requirements for this application.

Circuit Description

Figure 2 shows the basic diagram of the regulator. The output stage of the regulator consists of an NMOS M1 in source-follower configuration, a gate decoupling capacitor C1 and a bias resistor R1. This output structure implies an inherently low output impedance for all frequencies. A slow but accurate control loop drives the gate to the right DC voltage. (Fast control has no sense because load current variations will always be faster than a control loop could handle) For this reason the output voltage varies slightly with load current. The output voltage margin of $\pm 10\%$ can be used partly for this voltage variation. The remaining voltage margin is necessary for the limited static accuracy of the control loop. For a certain allowable dynamic voltage variation and bias/peak load current ratio optimum dimensions can be found for capacitor and NMOS per unit peak load current. Absolute dimensions are proportional to the actual required peak load current. Note that peak load currents in digital circuits can be much larger ($\sim 5x-10x$) than average current. Transistor M1 is biased close to weak-inversion for maximizing gm/I , which implies a small voltage variation for quite a large current ratio. For $200\mu A$ bias current, $100mA$ peak load current and $400mV$ dynamic voltage variation this results in a W/L of $14000\mu m/0.5\mu m$ for the NMOS and $180pF$ for C1 which is implemented in gate oxide. The large signal output resistance ($1/gm$) for these dimensions is about 2.5Ω .

The required gate voltage V_G for the output stage can be larger than V_{DDD} , especially when V_{DDD} becomes smaller than $4.5V$. Therefore this gate can only be driven by a chargepump. This has resulted in a control loop which consists of a bandgap reference, a comparator, a clamp circuit, a chargepump and a replica circuit for feedback as shown also in figure 2. An oscillator delivers the required clock signal. The operation of the control loop can be understood as follows: The resistive division in the replica branch (M2,R2,R3) scales down the nominal copy of the output voltage. The resulting feedback voltage equals the bandgap reference voltage of $1.2V$ if and only if the nominal regulator output voltage is correct. Now, using its input signals the comparator can decide whether the gate voltage must increase or decrease, which is done via the clamp circuit with the bidirectional chargepump. This way it has been possible to realise a regulator with source-follower output which has a low drop voltage of only a few hundred millivolts. V_{DDD} can even be lower than $3.3V$ although the output voltage will always be slightly lower than V_{DDD} .

The concept of a chargepump driving the gate has certain advantages. The regulator can operate for external supply voltages down to $3.3V$. Furthermore the rest of the regulator circuitry can now principally operate at a lower, process tolerated, voltage. Structures similar to the output stage generate these lower supplies locally because the whole regulator must be supplied from the external V_{DDD} . The chargepump circuit acts as a capacitive voltage doubler (see also figure 5a). For an input voltage of $V_G/2$ the chargepump is in equilibrium and doesn't transport any charge. Because the chargepump is connected to the high gate voltage stress easily occur in this circuit. Safe operation has been guaranteed by keeping its input voltage close to $V_G/2$.

The clamp circuit (figure 3) delivers a voltage to the chargepump which is approximately $V_T/2$ higher or lower than $V_G/2$. The process parameter V_T is used because its well defined and easy usable. Some important DC settings are given symbolically in the diagram. The actual output voltage of the clamp circuit is set by either a source or sink current depending on the decision of the comparator which output is connected to the input of the clamp circuit. This voltage clamping has the consequence that the chargepump transfers well defined charge packages of $Q=C_{pump} \cdot V_T$ to or from C1.

Instead of sensing the output voltage directly, a replica branch is used for feedback which guarantees stability independent of the load. This is a great advantage since the exact load is not known. Influence of process variations and temperature at DC settings is cancelled thanks to the matched structure of the replica. The replica also ensures that the output is only controlled for a correct nominal DC setting. This reduces the maximum possible output voltage swing by a factor of two because the loop doesn't react on a varying load current, which is illustrated in figure 4. Without replica it would be impossible to achieve 10% output accuracy together with an acceptable quiescent current, due to the limited gm/I of the output stage transistor. A bandgap reference was necessary to obtain the required static accuracy.

Besides the main control loop the regulator also contains a power-down loop which consumes much less power. For power-down mode the main control loop is almost completely switched off and the bias current in the output stage is reduced to a minimum level in order to save power. Using handshakes the control is smooth and safely taken over by the less accurate power-down loop [1], which only consists of a chargepump and a stacked diode voltage reference (M3-M5), which is shown in

figure 5. An oscillator and some additional biasing are required to make operation possible. Its output voltage is accurate enough to maintain safe operation and to keep f.i. memory contents correct.

Implementation

The implementation of the regulator subcircuits contains several measures against hot-electron effects to ensure safe operation for VDDD up to 5.5V. These include: over-voltage protection with cascodes, voltage division by series connection, voltage clamping, locally generated lower supplies (see for example figure 3) and temporary reduction of critical voltages in case of operation mode changes.

The regulator is implemented in modules for 100mA peak load current each, for easy power scaling. A complete regulator can consist of several modules in parallel depending on the totally required peak load current for an application. In case of overload the output voltage will become only slightly too low due to the source-follower output structure. Every module has its own main control loop except for the bandgap reference and oscillator. This ensures a loop behaviour independent of the number of modules. The modules together have only one common power-down loop for power saving reasons, which is implemented together with bandgap, oscillator and additional biasing and control circuitry in a single common module.

Experimental Results

A 300mA_{peak} regulator has been designed for an XA microcontroller application [6]. The die area of this regulator is 1mm² which is dominantly determined by M1 and C1. A chip photograph of the embedded regulator is shown in figure 6. The measured DC output characteristics of the regulator are shown in figure 7. The measured internal supply voltage of the XA microcontroller IC operating at 20MHz clock frequency is shown in figure 8. In power-down mode the regulator has a nominal output voltage about 2.8V and consumes only 12µA supply current.

Conclusions

An embedded 5V-to-3.3V supply regulator for digital ICs in 3.3V, 0.5µm CMOS technology has been designed. The circuit is able to deliver the steep supply-current transients for digital circuits while the output voltage remains within 10% accuracy. This has been achieved with a circuit which needs no large (external) capacitor across the internal 3.3V. The circuit has a small die area: 1mm² for 300mA peak current. The output voltage remains correct for an external supply voltage down to 3.3V. The replica technique used guarantees stability independent of the load and drastically reduces the voltage ripple at the output. The implementation of the regulator contains several measures against hot electron effects to ensure safe operation for VDDD up to 5.5V.

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- [6] Datasheet Philips Semiconductors 16-bit 80C51XA Microcontroller XA-G33

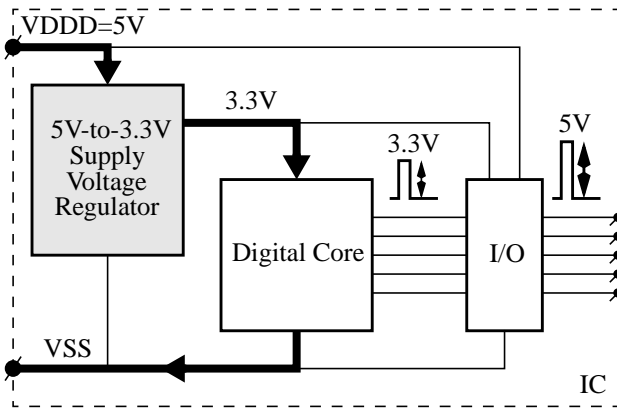


figure 1: Typical IC application of the regulator

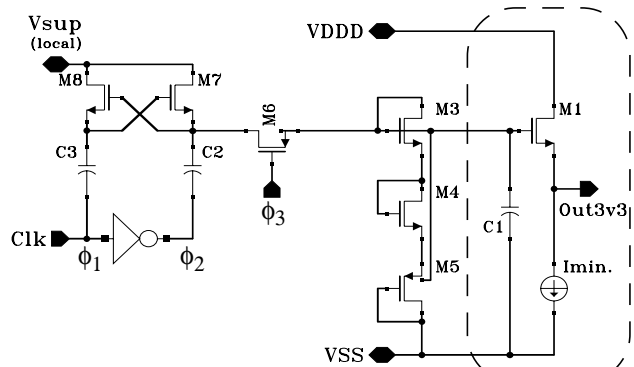


figure 5: a Chargepump

figure 5: b Diodes Stack & Output Stage

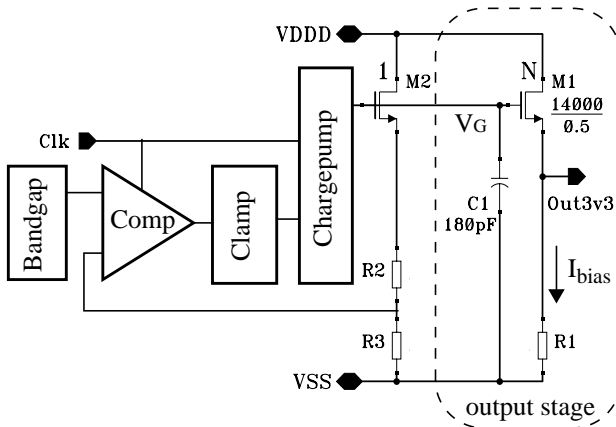


figure 2: Basic Regulator Diagram

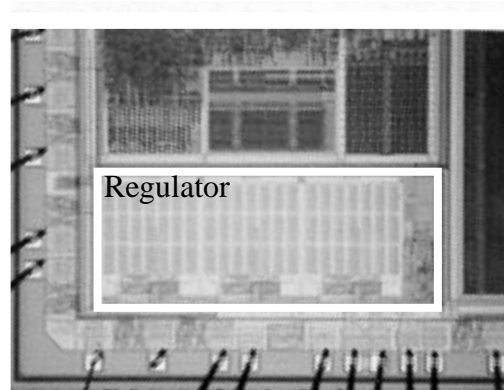


figure 6: Photograph of the Regulator Embedded in an XA μ C IC

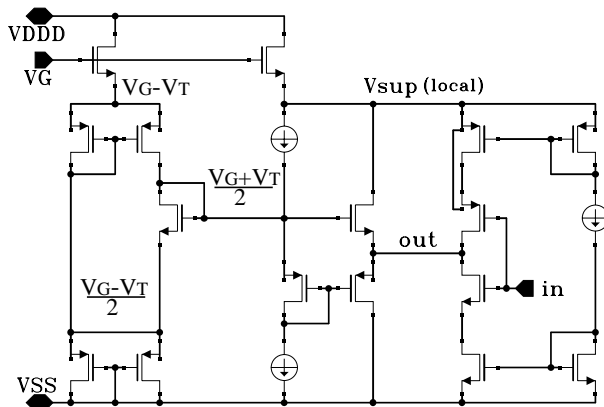


figure 3: Schematic of the Clamp Circuit

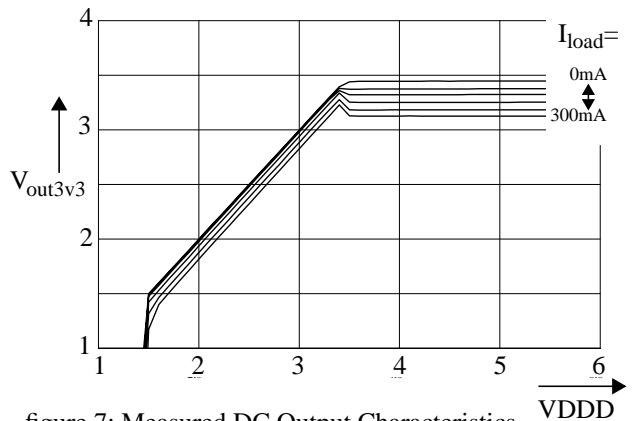


figure 7: Measured DC Output Characteristics for Various Load Currents

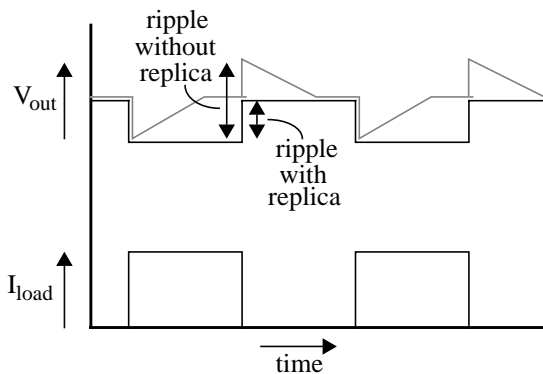


figure 4: Effect of Replica on Output Behaviour

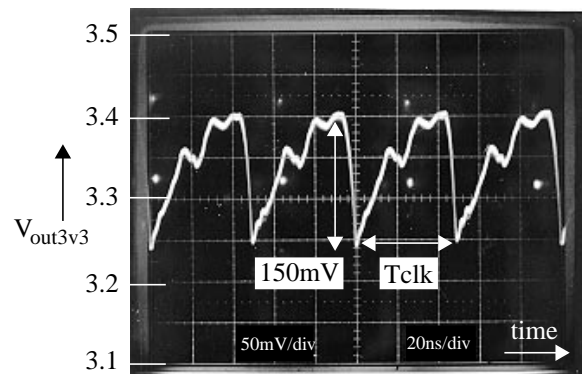


figure 8: Measured Internal Supply Voltage Transients of the XA μ C Operating at 20 MHz