

A -90 dB THD Rail-to-Rail input opamp using a new local charge pump in CMOS

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Abstract

This paper describes the principle and design of a CMOS Rail-to-Rail input operational amplifier with THD performance of -90 dB. The operation of the opamp is based on a standard two-stage Miller configuration and is capable of driving a low ohmic load (32 Ω). THD levels below -90 dB has not yet been shown with existing Rail-to-Rail techniques. The Rail-to-Rail functionality is achieved with a new area efficient on chip charge pump circuit for the generation of the supply voltage for the input differential pair.

1.0 Introduction

Today, analog circuits in a mixed signal CMOS IC's have to operate in a noisy environment, furthermore the supply voltage tends to decrease in the newer process generations. Therefore signal swings must be as high as possible which makes the use of Rail-to-Rail input and output analog circuitry useful. The use of inverting amplifiers with a virtual earth technique network is also capable of handling large swing signals but, has some disadvantages with respect to input impedance and design flexibility.

For an amplifier a Rail-to-Rail output stage is generally not a major problem. The design of a high performance Rail-to-Rail input stage is much more difficult. Several methods exist to design a Rail-to-Rail input stage. The most simple form is given in figure 1 and consists of a composite P and N channel differential pair. The disadvantage of such a input stage is that unity gain bandwidth, slewrate and transconductance vary with the common-mode input voltage. There are several techniques known to overcome these problems: most of these techniques rely on accurate modelling of the MOS transistor [1],[2] however the use of this model will be limited in future sub-micron CMOS processes. Also MOS characteristics independent techniques [3] can not overcome the major problem for high performance Rail-to-Rail input stages which is the bad distortion figures. The limiting factor of these input stages is the difference in offset voltage of the P and N channel transistors which are respectively active in the lower and upper part of the Rail-to-Rail input signal. A difference between the offset voltage of 1 mV will give rise to distortion components if the amplifier is used as a voltage follower. The THD will be in this case about -60 dB which is far from suitable for high quality Audio systems.

2.0 Circuit description

With a normal differential input pair the specifications for Audio systems can easily be achieved, only the common-mode input range of a single differential input pair has to be expanded for Rail-to-Rail operation. Instead of using complex circuitry [1],[2],[3], expanding the common-mode input range can also be done by simply using a higher supply voltage for the differential input pair. The higher supply voltage for the differential input pair has to be generated on-chip, so an area efficient charge pump circuit with no external components has to be designed. In figure 2 a folded cascode Rail-to-Rail input stage is given. The tail current source M_{tail} of the differential input pair must be supplied with a voltage $V_{ddx} = V_{gs}(M_{tail}) + V_{dsat}(M_{tail}) \cong 1 \text{ V}$ higher than the actual supply voltage to keep the PMOS transistor current source M_{tail} in saturation. The design of this folded cascode input stage is not different from a classical folded cascode input stage with respect to gain, noise, distortion and frequency behaviour. To allow this type of input stage, a new current driven class AB output stage has been designed based on the circuit described in [4] for driving the load close to the power supply rails. In figure 2 this output stage is also given. A two-stage Miller topology is used for a number of reasons. Firstly, this topology appears to be the most power-efficient for the expected loads and, secondly, the frequency compensation is rather straight forward for this structure. The quiescent current control in the complementary output transistors M11 and M12 of the output stage uses the principle of complementary DC currents I3 and I4 flow in complementary stacks of diode connected transistors. The quiescent current in the output stage is determined by the aspect ratio between respectively transistor M17 and M11 and transistor M20 and M12. The output current of the input stage is injected into the output stage and splits up and flows in the sources of transistor M15 and M16. When a current is injected into the output stage the gate voltage of the output transistors M11 and M12 will rise which will turn the NMOS output transistor M12 on and the PMOS output transistor M11 off. This operation is reversed for the case when the current is pulled out the output stage.

As mentioned before, the Rail-to-Rail operation of the designed opamp is achieved with a local higher supply voltage (V_{ddx}) for the input differential pair. This is done by an on-chip charge pump circuit which has a low output voltage ripple while the integrated capacitors are still small. The well known conventional charge pump circuit as given figure 3 was derived from the circuit described in [5]. This circuit operates as follows: when the input clock signal V_{in} equals V_{dd} ("high") the charge pump capacitor C_a will be charged by transistor M1. When V_{in} is "low" the capacitor C_b will be charged by transistor M2 and the capacitor C_a will act as a voltage source, lifting the voltage V_a to twice the supply voltage V_{dd} as illustrated in figure 3. PMOS transistor M4 conducts current when V_a is high and V_b is low and M3 vice versa. When a very small current must be delivered the output voltage will be close to $2 \cdot V_{dd}$. When a larger current has to be delivered the ripple on the output voltage will rise. With equation 1 the ripple voltage V_r of this charge pump can be calculated [6].

$$V_r = \frac{1}{2} \cdot \frac{I_o}{C_o \cdot f_o} \quad (\text{EQ 1})$$

The tail current which is needed for this opamp design is about $60 \mu\text{A}$. If an output voltage ripple of 5 mV is required the capacitor C_o must be 1.2 nF with a clock frequency of 10 MHz . Such a large capacitor makes this charge pump unsuitable for on-chip implementation.

To get rid of this large buffer capacitor a new charge pump is designed by using two conventional charge pump circuits. In figure 4 the simplified schematic of the conventional ("old") and the novel ("new") charge pump is depicted. As mentioned before the output voltage ripple in the "old" situation is controlled with the buffer capacitor C_o . In the "new" situation charge pump 1 is used for driving the gate of NMOS transistor M_{buf} and charge pump 2 is used for delivering the actual output current. The output voltage ripple on node V_x has the same relationship as given in equation 1, however the output voltage ripple on node V_{ddx} is reduced with a factor $g_m(M_{buf}) \cdot r_{ds}(M_{buf})$ which has a typical value between 30 and 100. This means that the buffer capacitor C_o in this charge pump can be the same factor smaller for an output voltage ripple equal to that of the "old" version of the charge pump. In figure 5 the complete charge pump is given with the waveforms. The waveforms on node V_a and V_b are the same as given in figure 3. The buffer capacitor C_o has a value of 14 pF

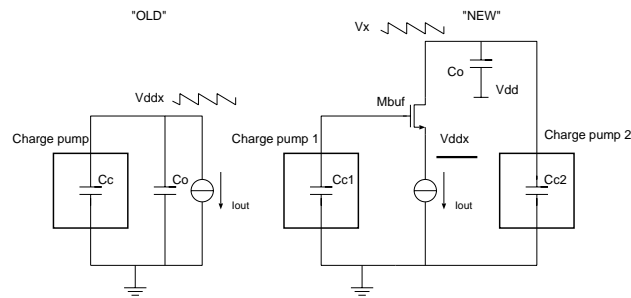


Figure 4 Simplified schematic for a conventional and the novel charge pump

with the given transistor dimensions and output current the output voltage ripple will be about 5mV. The output current delivered by this type of charge pump is determined by the size of the charge pump capacitors however it is restricted, because the NMOS transistors M5 and M6 (equivalent to Mbuf in figure 4) must stay in saturation for proper operation of the charge pump.

3.0 Experimental results

The opamp has been realized in a 0.5 μm CMOS technology. A photograph of the opamp with local charge pump is given in figure 6. The area of the charge pump is 0.08 mm^2 and the area of the opamp is 0.4 mm^2 . The THD performance of the opamp is better than -90 dB for an input voltage level of 2.8 V_{pp} (1 V_{rms}) and a supply voltage of 3V. This measurement is done without heavy loading of the output stage in order to reduce the crossover distortion of the output stage. When the opamp is loaded with a 32 Ω load the THD performance drops to -81 dB due to this crossover distortion. Clock feed-through and noise levels due to the on-chip charge pump were below the noise floor of the opamp. A summary of the experimental results of the opamp is listed in table 1.

4.0 Conclusions

A Rail-to-Rail input and output operational amplifier has been successfully implemented. The performance including distortion of the opamp is comparable to the same opamp with a non Rail-to-Rail input stage in virtual earth configuration. The authors believe that this is the first time that such a Rail-to-Rail opamp can be used for high quality Audio applications. The area efficient charge pump can find its application in many analog blocks which have to be implemented in future low-voltage submicron CMOS processes

5.0 References

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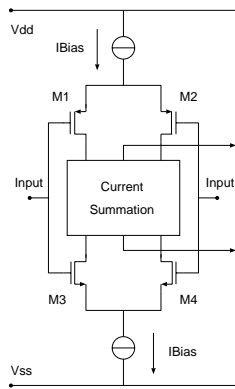


Figure 1 Conventional Rail-to-Rail input stage

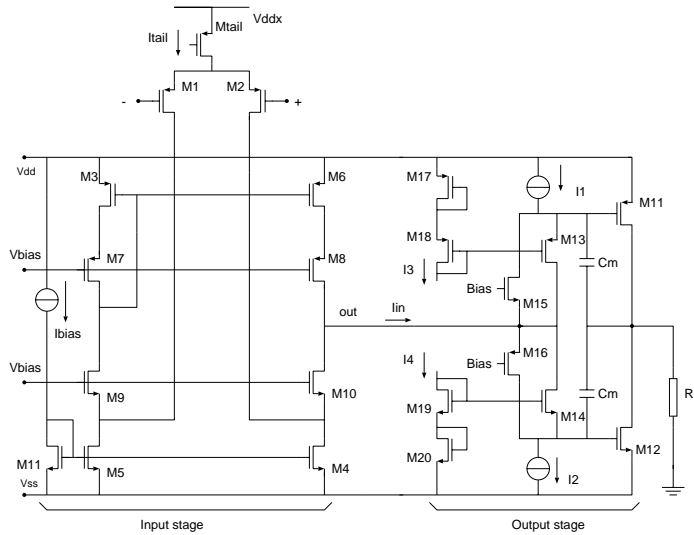


Figure 2 Input pair supply voltage (V_{ddx}) generated with charge pump

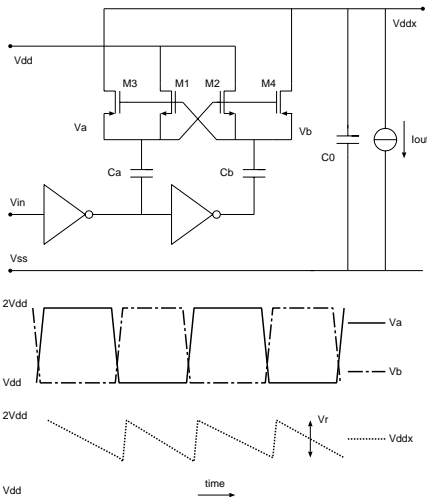


Figure 3 Conventional charge pump with large buffer capacitor

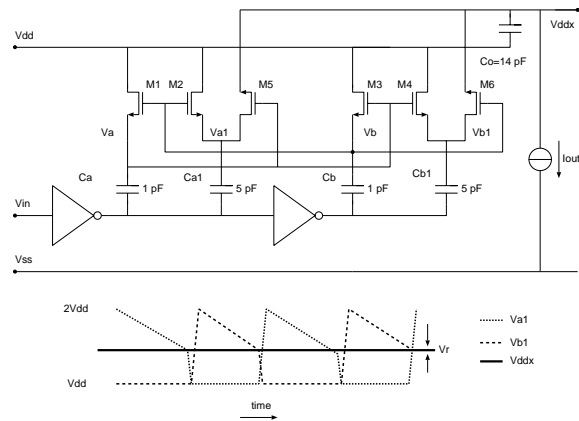


Figure 5 Novel charge pump with small internal buffer capacitor and small output voltage ripple

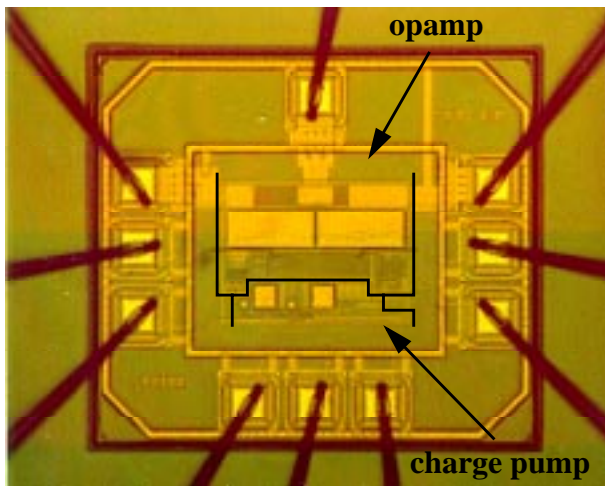


Figure 6 Micro photograph of the opamp and charge pump

Power supply	1.8 - 3.3 V
Iquiescent	750 μ A
DC gain	60 dB
unity gain	6.5 MHz
THD ($V_{dd}=3V$) $V_{in}=V_{out}$	
$V_{in}=2.8 V_{pp}=1V_{rms}$	
load = 10 k Ω	-90 dB
load = 32 Ω	-81 dB
S/N ratio	100 dB
Technology	0.5 μ m CMOS
active die area	0.5 mm ²
Clock frequency	6 - 20 MHz

Table 1 Measured opamp performance summary