

A DIRECT DIGITAL SYNTHESIZER WITH AN ON-CHIP D/A-CONVERTER

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Abstract — A Direct Digital Synthesizer (DDS) with an on-chip D/A-converter is designed and processed in 0.8 μm BiCMOS. The digital parts of the chip are implemented with CMOS design to reduce power consumption. The 10-bit D/A-converter is designed with BiCMOS technology in order to operate at a clock rate of 150 MHz. At the 150 MHz clock frequency, the Spurious Free Dynamic Range (SFDR) is 60 dBc at low synthesized frequencies, decreasing to 52 dBc at high synthesized frequencies in the output frequency band (0 to 60 MHz). The DDS covers the output frequency band in steps of 0.0349 Hz with the frequency switching speed of 140 ns. The chip has a complexity of 19,100 transistors with a die/core area of 12.2/3.9 mm². The power dissipation is 0.6 W at 150 MHz @ 5 V. The maximum operating clock frequency of the chip is 170 MHz.

I. INTRODUCTION

The block diagram of the direct digital synthesizer (DDS) is shown in Fig. 1. The input word to the phase accumulator controls the frequency of the generated sine wave. The phase value is generated by using the modulo 2^j overflowing property of a j -bit phase accumulator. The rate of the overflow is the output frequency. The phase accumulator addresses the sine Read Only Memory (ROM) which converts the phase information into the values of a sine wave. The ROM output is presented to the D/A-converter, which develops a quantized analog sine wave. The filter removes high frequency sampling components and provides a pure sine wave output. As the DDS generates frequencies close to one half the clock frequency, the first image becomes more difficult to filter. Therefore, in practice, the DDS operation is limited to approximately 40 % of the clock frequency.

II. DESIGN REQUIREMENTS

With the used 0.8 μm double-metal double-poly BiCMOS process, as with most IC processes, the accuracy of the current steering D/A-converter without additional calibration techniques is about 10-bit. This was the most decisive factor in this design. To meet the distortion requirements of the 10 bit D/A-converter, the clock frequency is limited to 150 MHz. The phase accumulator

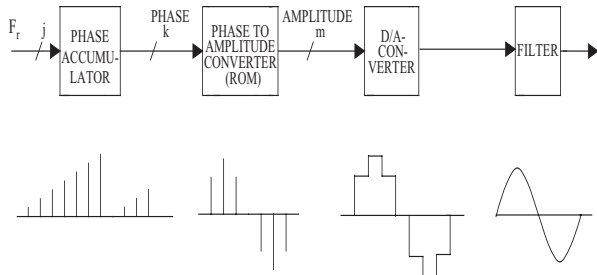


Fig. 1. Simplified block diagram of the direct digital synthesizer, and the signal flow in the DDS.

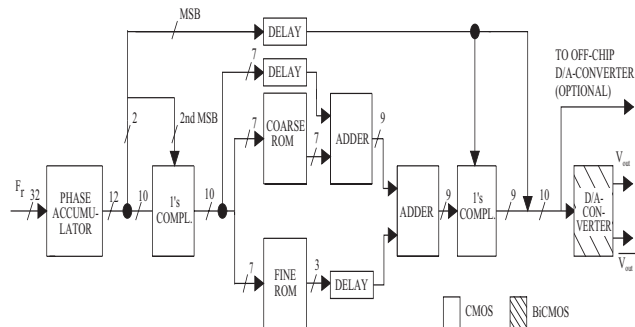


Fig. 2. A block diagram of the DDS chip architecture.

wordlength was chosen to be 32-bits to achieve a frequency resolution of 0.0349 Hz at a clock rate of 150 MHz [1]. Since the amount of memory required to encode the entire width of the phase accumulator would be prohibitive, only 12 of the most significant bits of the accumulator output are used to calculate the sine-wave samples. The phase resolution of 12-bits results in a spurious performance due to the phase accumulator truncation of -72 dBc [1], which will be below the spurs from the 10-bit D/A-converter at 150 MHz.

III. CHIP ARCHITECTURE

A. 32-bit Phase Accumulator

In order to provide operation at 150 MHz, the 32-bit phase accumulator was pipelined in 4-bit stages. In this chip it is possible to set the carry input to the phase accumulator toggle between 0 and 1 periodically. This causes the phase accumulator output sequence to have a maximal numerical period for all values of the input word. It has an effect of randomizing errors introduced by the quantized sine ROM samples and averaging D/A-converter errors.

B. Sine ROM Compression

A straightforward implementation of the sine memory requires a $2^{12} \times 10$ -bit ROM, whose access time reduces the maximum DDS clock frequency much below 150 MHz. Therefore a sine memory compression technique is applied to reduce the size and access time of the sine ROM [1]. The architecture for the sine ROM compression is shown in Fig. 2. The two most significant phase bits are used to decode the quadrant, while the remaining 10 bits are used to address one-quadrant sine ROMs. The coarse ROM provides low resolution phase samples, and the fine ROM gives additional phase resolution by interpolating between the low resolution phase samples in Fig. 2. In Fig. 2 the size of the upper memory, whose access time is the most critical, is reduced by the sine difference algorithm [1]. This saves 2 bits of amplitude in the storage of the sine function, but an extra adder is required at the coarse ROM output [1]. The $2^{12} \times 10$ sine samples are compressed into $2^7 \times 7$ coarse samples and $2^7 \times 3$ fine samples resulting in a compressing ratio of 32 : 1. A FFT of the compressed ROM contents gives the worst case digital output spectral purity of -74 dBc.

IV. CIRCUIT DESIGN ISSUES

A. ROM Block Design

The cycle time of the ROM memory is portioned by placing pipeline stages after the word and bit line decoders and before the output buffer of the ROM to enhance the operation speed. In order to achieve high densities and good speed performances, the ROM memory point matrix is implemented as a wired-nor array [2]. Fig. 3 shows the ROM memory point matrix with associated word and bit lines. By adding ground switches between the transistors and the ground, it is possible to select the word line during the precharging. This increases the operation speed of the memory at the expense of some power dissipation.

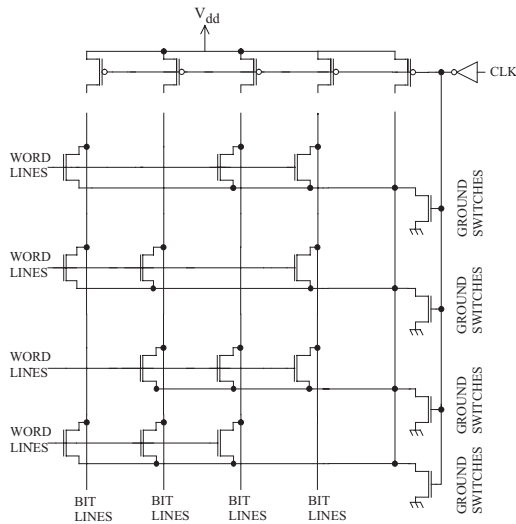


Fig. 3. ROM memory points matrix.

B. D/A-Converter

The designed IC-circuit has an on-chip D/A-converter, which is based on the well-known current steering principle. The on-chip D/A-converter avoids delays and line loading caused by interchip connections. The block diagram of the two-stage current array D/A-converter is shown in Fig. 4. The two-stage current array reduces the number of the current sources and thus makes more efficient use of the chip area. The input to the D/A-converter is converted into a differential ECL signal which is latched before it is fed to the differential pair (current switch). The output currents of the current switches are converted into voltages with resistors. Finally, there is an emitter follower buffering the output. The D/A-converter is implemented with a balanced design, which results in reduced even-order distortion and provides common-mode rejection to noise.

The D/A-converter uses binary weighted MOS-current sources and bipolar transistors as current switches. In the used process, the MOS current switch cannot toggle the current between the complementary outputs at the clock rate of 150 MHz, so the bipolar current switches are used. The problem of the bipolar current switch transistor is a base current error. This effect was compensated for by extracting an equivalent amount of current at the common emitter node of the current switches [3].

C. Layout Considerations

A problem inherent in high-speed CMOS chips is the power supply switching noise. To minimize switching noise from the digital logic to couple to the output D/A-converter, the power supplies for the digital logic and the analog part are routed separately. All different digital parts of the circuit are surrounded by guard rings and the analog parts of the D/A-converter by double guard rings to minimize noise injected to the analog output through the substrate.

To eliminate process and temperature related gradients in the D/A-converter current source transistor arrays, a common-centroid layout is used [4]. The D/A-converter clock controls the latches that drive the output current switches. Therefore it controls the digital-to-analog conversion process and must be considered an analog signal. It's purity has a direct effect on the output spurs. In the layout the D/A-converter clock signal is separated from the digital signals to prevent the switching currents from coupling onto the D/A-converter clock.

V. EXPERIMENTAL RESULTS

The effect of D/A-converter static nonlinearities is investigated in Fig. 5, where the clock and signal frequencies are low. The harmonics are below noise level in Fig. 5, where the carrier to noise ratio is about 75 dBc. So the D/A-converter fulfils the requirement of 10-bit static linearity. At a

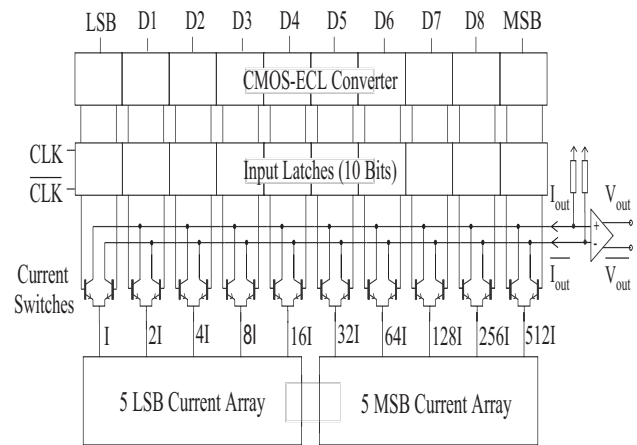


Fig. 4. 10-bit two-stage current array D/A-converter.

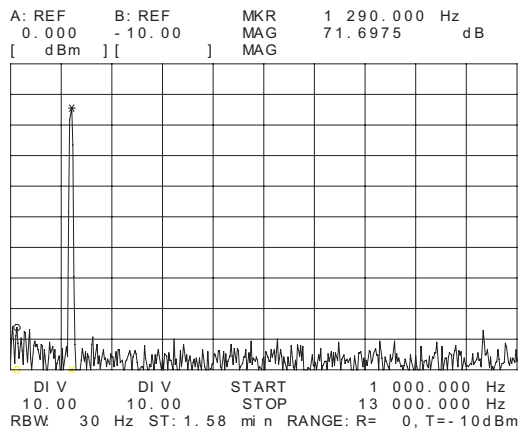


Fig. 5. Spectrum of 1.29 kHz output sinewave, where the clock frequency is 10 MHz.

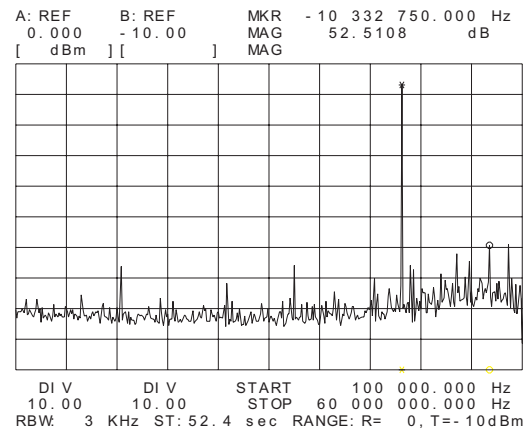


Fig. 6. Spectrum of 45.8 MHz output sinewave, where the clock frequency is 150 MHz.

high clock frequency the effect of glitches will appear in the spectrum and this can be viewed as an increased amount of spurs in Fig. 6. This is because the output voltage is held for shorter periods of time, the glitch becomes a greater percentage of the output energy. The measured Spurious Free Dynamic Range (SFDR) was 52.5 dBc at a generated frequency of 45.8 MHz in Fig. 6, where the clock frequency is 150 MHz. At the 150 MHz clock frequency, the SFDR is 60 dBc at low synthesized frequencies, decreasing to 52 dBc at high synthesized frequencies in the output frequency band (0 to 60 MHz). Reducing the output frequency band from 40 % to 33 % of the clock frequency, the SFDR is increased by 6 dB in average, because the spur energy due to glitches is mostly concentrated at the high frequencies as shown in Fig. 6. The DDS is operating up to 170 MHz clock frequency after which digital errors will occur due to internal timing problems.

VI. CONCLUSIONS

The DDS covers a bandwidth from DC to 60 MHz in steps of 0.0349 Hz with a frequency switching speed of 140 ns. Fig. 7 shows a chip micrograph. Table 1 summarizes chip specifications.

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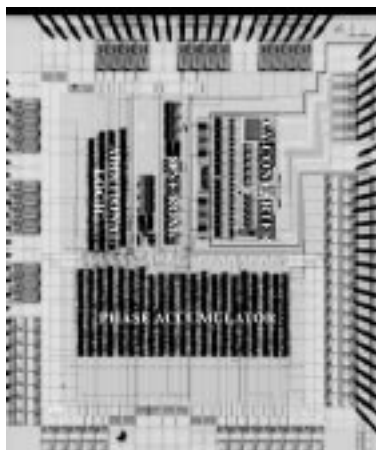


Fig. 7. The micrograph of the chip.

TABLE 1. DDS Chip Specifications

IC Technology	0.8 μ m double-metal double-poly BiCMOS
Max Clock Frequency	170 MHz @ 5 V
Tuning Bandwidth	60 MHz (0.4×150 MHz)
Frequency Resolution	0.0349 Hz (at 150 MHz)
Freq. Switching Time	140 ns ($21 \times 1/(150$ MHz))
SFDR at low f_{out}	> 60 dBc (at 150 MHz)
SFDR at high f_{out}	> 52 dBc (at 150 MHz)
Transistor Count	19,100
Power Dissipation	0.6 W at 150 MHz @ 5 V
Die/Core Size	12.2 mm ² /3.9 mm ²