Robust CMOS Compander

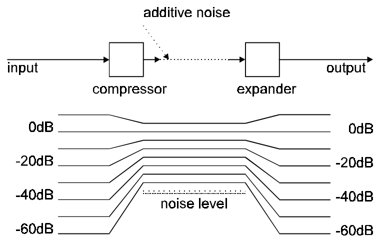
David Hossack
Wolfson Microelectronics
Edinburgh, UK
david@wolfson.co.uk

Abstract

An improved sigma-delta compander topology is described which has been used to implement a robust compander on a CMOS process. No external components are required and test time is reduced when compared to conventional compander implementations.

Introduction

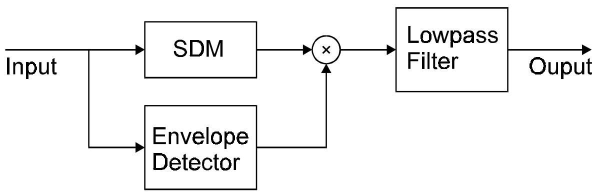
Signal amplitude compression is used to increase the perceived performance of voice communication systems with noisy transmission channels. The technique is essentially an automatic gain control system whereby the amplitude of small signals is increased before transmission and this gain compensated for in the receiver.



Several difficulties are encountered when integrating companding systems on to silicon. One fundamental problem is the requirement to multiply analogue quantities which is most easily accomplished by using bipolar transistors in a Gilbert cell multiplier. The full wave rectifier must have low input offset since the offset will dominate for small signal levels resulting in low level mis-tracking. A further difficulty with the design of the envelope detector is the implementation of the long time constant required for the smoothing filter. This is typically 20ms, corresponding to a -3dB frequency of 9Hz. Offsets arising in this filter give the same problems as for offsets in the rectifier. Typically this filter requires the use of external components.

Sigma-Delta Based Compander

An alternate topology (Figure 1) for the compander function was introduced in [1,2].



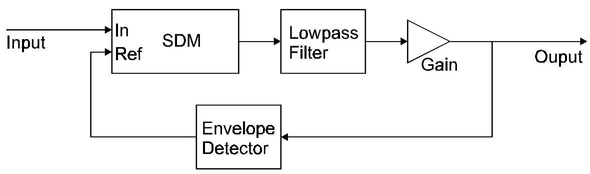


Figure 1 Expander and compressor using sigma-delta modulator.

These circuits exploit the single bit output of a sigma-delta modulator to simplify the multiplier. The lowpass filter required to remove the high frequency noise resulting from the sigma-delta modulator is already present in most communications applications.

Whilst elegantly solving the multiplication problem, there are still difficulties encountered when implementing this system. The problem of implementing the rectifier and time constant circuit with little offset remains but has been lessened in the reported implementation by using offset compensating SC techniques. The conversion of the analogue input signal to a digital form and back to analogue exposes the speech signal to all the quantisation noise inherent in the conversion process, together with other undesirable effects such as tones which plague the implementations of simple low order and low oversampling ratio converters. A further disadvantage with the compressor is that the sigma-delta modulator operates on the uncompressed input signal and therefore requires a noise performance commensurate with the uncompressed dynamic range. The entire compressor loop must have low offset unless AC coupling is possible. The gain required in this loop makes this requirement difficult to meet.

Improved Compander System

An alternate sigma-delta based compander has been developed which allows the complete system to be integrated on a pure CMOS process with no external components.

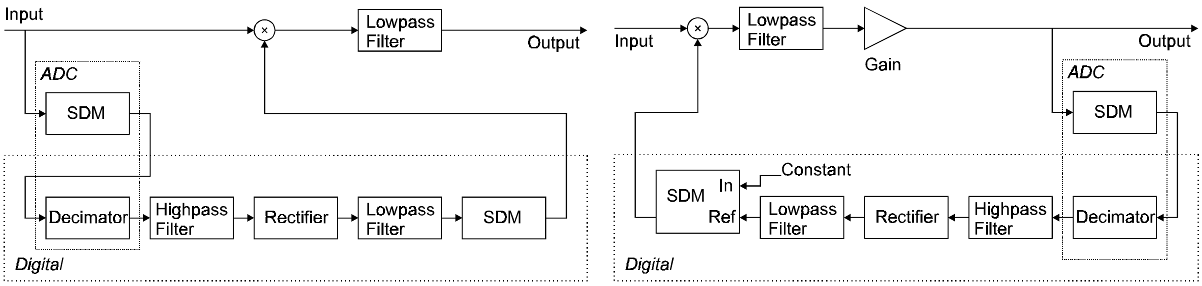


Figure 2 Mixed signal implementation of the expander and compressor.

The significant difference with the new systems depicted in Figure 2 is that it is the low bandwidth envelope signal which is sigma-delta modulated. The speech path remains completely analogue. The quantisation noise of the sigma-delta modulator which appears at the output is scaled by the amplitude of signal. When the signal disappears in the idle channel condition, the output of the sigma-delta modulator is not seen at the signal output.

A further difference with the new system is that the input of the envelope detector is digitised and used to perform the envelope detection digitally. This is achieved with an analogue sigma-delta modulator combined with a digital decimation filter. The signal being digitised has only the compressed dynamic range, and since it is only the signal amplitude which is ultimately required, this part of the system is tolerant of spurious tones and distortion. The digitised signal is high-pass filtered to remove any DC offset before being rectified. The time constant in the envelope filter is implemented digitally. The complete system may be completely integrated with no external components. This solution is very robust. Another significant advantage is that the test time can be considerably reduced since the circuits implementing the high pass and the low pass filters may be tested digitally without waiting for settling of the long time constants involved.

A first order sigma-delta modulator is adequate to provide the signal for the one-bit multiplier. Figure 3 shows the in-band noise versus DC input level on both linear and logarithmic axes and it is seen that the noise is proportionate to the input level. This is a desirable characteristic for the compander application. The simulated SNR and gain tracking error of the expander and compressor are shown in Figure 4 and Figure 5. The saw-tooth patterns in the tracking errors are due to truncation effects in the digital implementation of the filters. The effects on SNR of the 1st order sigma-delta modulator noise characteristics as shown in Figure 3 are clearly apparent. The 1st order digital SDM can be implemented using a single adder and latch.

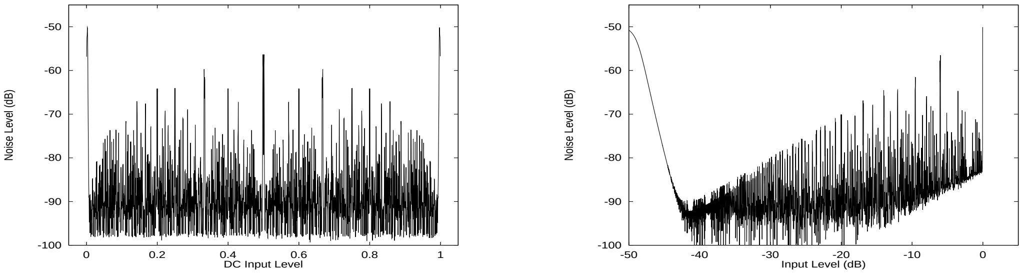


Figure 3 Noise from 1st order sigma-delta modulator (linear and logarithmic axes).

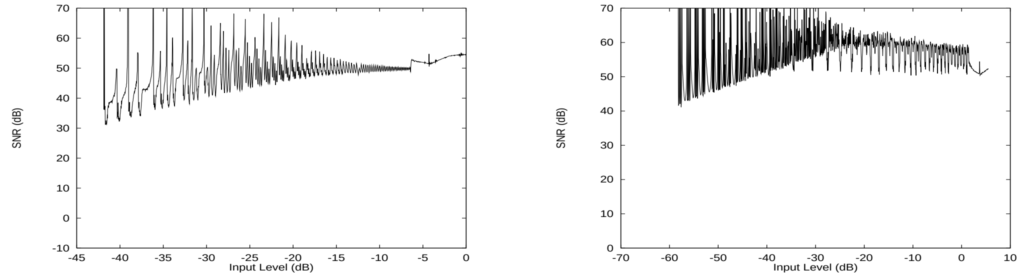


Figure 4 Simulated SNR of expander and compressor.

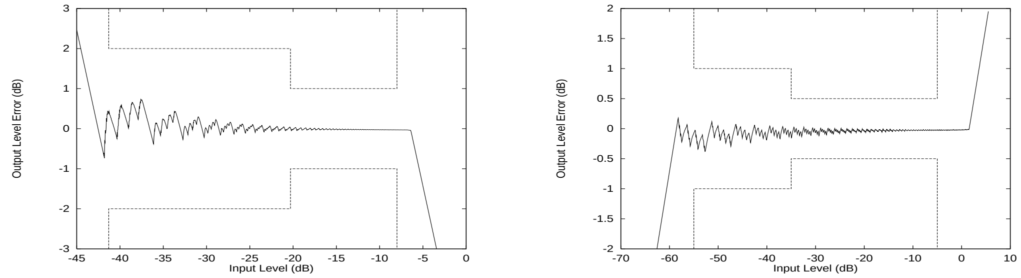


Figure 5 Simulated tracking error of expander and compressor.

Practical Implementation

The compander have been implemented on a 0.8µm CMOS process with double level poly-silicon. The integrated compander requires no external components.

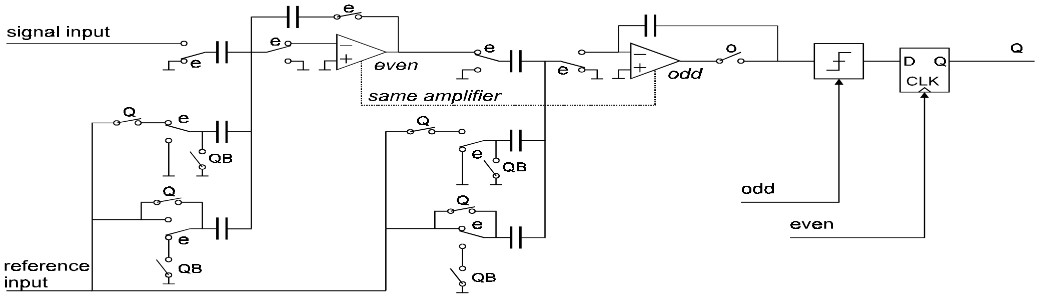


Figure 6 Second order SC sigma-delta modulator using single multiplexed opamp.

The main requirement for the ADC is that it must provide enough resolution to determine the signal level to within 1dB for the smallest input signal, typically -30dB relative to the largest signal. This implies a resolution and noise performance of 10 bits. This is achieved with an analogue sigma-delta modulator, followed by a decimation filter. A second order modulator was designed using a single multiplexed opamp and a second order comb decimation filter was sufficient for the decimator. The clock frequency was 960kHz. The one bit multiplier is built into the front end of the analogue low pass SC filter.

The compressor sigma delta modulator is slightly different to the expander sigma-delta modulator since it is required to produce an output bit stream with a ones density *inversely* proportionate to the input word. This is implemented using a first order modulator except that the input level is fixed at 1/32 and the reference is varied between 1/32 and 1. The range of 1/32 to 1 gives a gain range of -30dB to 0dB.

Much of the digital system was implemented using bit-serial techniques. Because most of the system comprises of shift registers with relatively few taps used, the logic can be laid out very efficiently even when an auto-routing tool is used. The digital circuitry is implemented in approximately 2000 gates for each of the compressor and expander. Each digital section has a single bit sigma-delta modulated input signal and a single bit sigma-delta modulated output. These four lines, together with a clock are the only signals which need to be passed between the analogue and digital parts of the companding system which allows the digital circuits to be placed remotely on the IC die.

Test Results

The specifications required of compressors and expanders typically include the gain tracking error, the signal to noise ratio, distortion, and the attack and recovery times. All the measurements were taken from the first silicon implementation operating on a 3.0V supply.

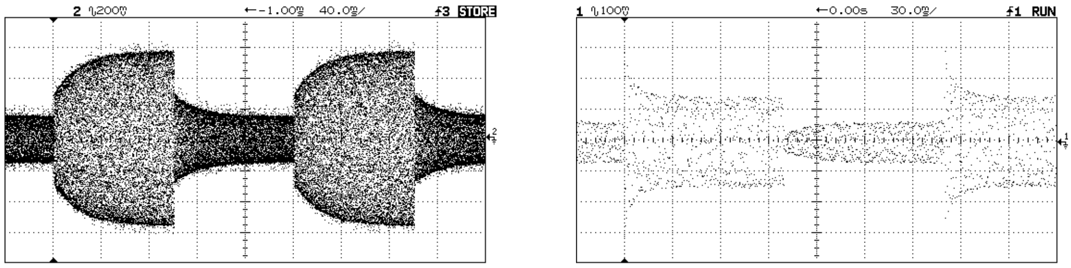


Figure 7 Measured expander and compressor step responses.

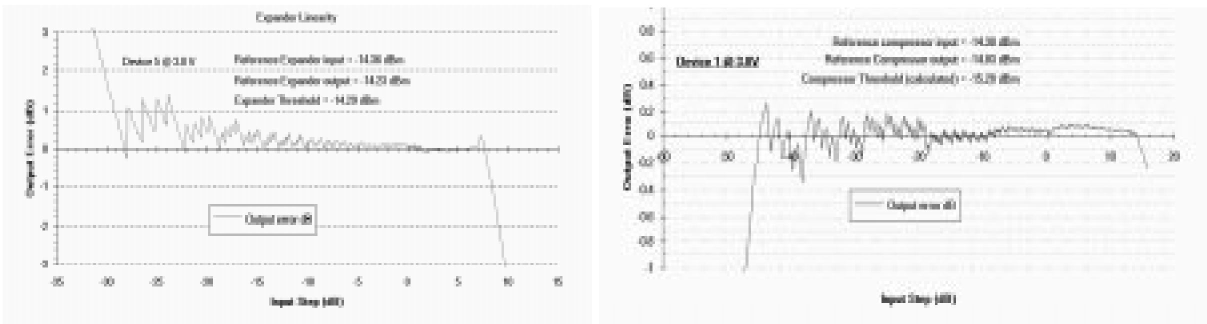


Figure 8 Measured gain tracking error of the expander and compressor.

Conclusions

The compander based on sigma-delta modulation has been designed, simulated, and fabricated with good success. The test results measured were very close to the simulation. This new topology is therefore a good choice for implementing analogue companders on modern CMOS processes.

[1] Karou Takasuka et al, "A Sigma-Delta Based Square-Law Compandor," *IEEE Custom Integrated Circuits Conference*, Boston, Massachusetts, pp. 12.7.1-12.7.4, 1990.

[2] Huang Qiuting, "Monolithic CMOS Compandors Based on ΣΔ Oversampling," *IEEE International Symposium on Circuits and Systems*, San Diego, California, pp. 2649-2652, May 1992.