

# LOW-POWER LOW-VOLTAGE CHOPPED TRANSCONDUCTANCE AMPLIFIER FOR NOISE AND OFFSET REDUCTION

M.A.T. Sanduleanu<sup>1</sup>, B. Nauta<sup>2</sup> and H.Wallinga<sup>1</sup>

<sup>1</sup>University of Twente, Department of Electrical Engineering  
P.O.Box 217, 7500 AE Enschede, The Netherlands  
E\_mail: m.a.t.sanduleanu@el.utwente.nl

<sup>2</sup>Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA  
Eindhoven, The Netherlands

## ABSTRACT

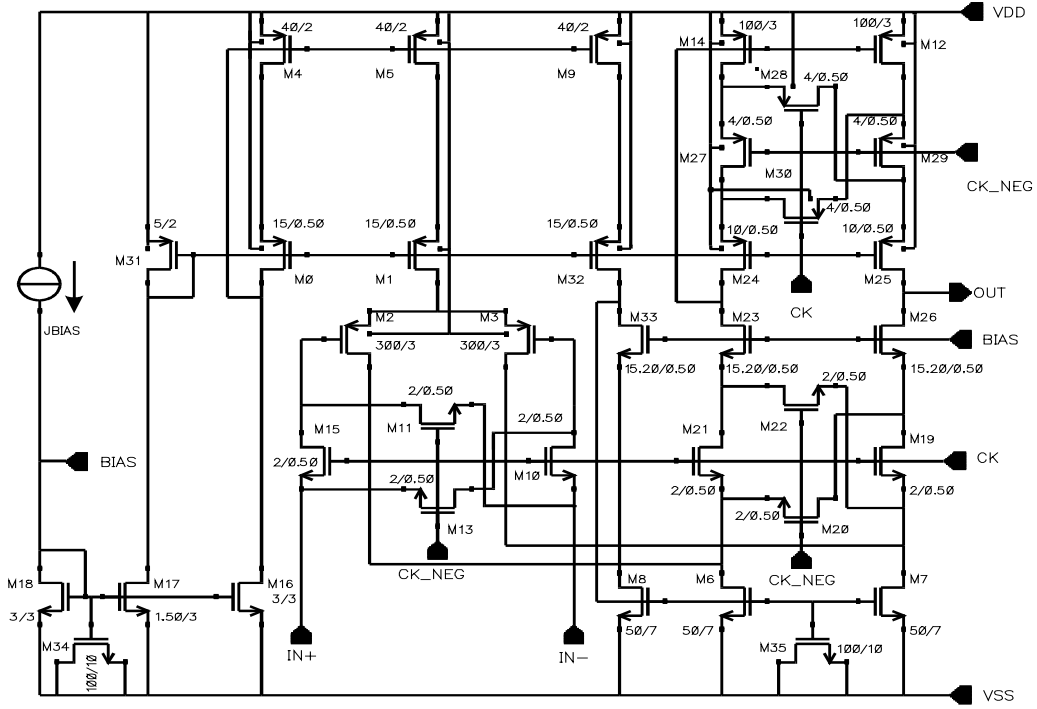
This paper describes the principle and design of a CMOS low-power, low-voltage, chopped transconductance amplifier, for noise and offset reduction in mixed analogue digital applications. The operation is based on chopping and dynamic element matching, to reduce noise and offset, without excessive increase of the charge injection residual offset. Experimental results show residual offsets of less than 150 $\mu$ V at 100kHz chopping frequency, a signal to noise ratio of 95dB, in audio band, for 100KHz chopping and a THD of -89dB. The power consumption is 594 $\mu$ W.

## 1. INTRODUCTION

The CMOS technology for mixed signal applications becomes less and less compatible with analog requirements due to the process tuning towards digital needs. As a consequence for analog functions built in digital CMOS the signal swing reduces with power supply and so does the dynamic range. Besides, 1/f noise properties are worsened for surface PMOST's in comparison to buried transistors, with an order of magnitude, and this under the conditions of a heavy crosstalk via the substrate from digital functions. At 3.3V and a 0.5 $\mu$ m CMOS technology, the substrate bounce can reach 300mV in amplitude with spectral contributions in GHz range, further reducing the voltage swing [1], [4]. In conventional chopper stabilized opamps for 1/f noise and offset reduction, differential amplifiers are being used and bandwidth is limited to few tens of kHz [2]. Switching at the differential output will introduce most of the switching noise and residual offset. This paper presents a chopped transconductance amplifier which circumvents the above mentioned drawbacks. The chopping frequency can reach MHz range without excessive increase in offset.

## 2. CIRCUIT PRINCIPLE

Fig.1 shows the circuit diagram. The input chopper M10, M11, M13 and M15 transposes the differential input signal applied to the terminals IN+ and IN- to the alternate output nodes.



**Fig.1: Circuit diagram**

As a result, the signal is modulated at odd harmonics of the chopper frequency. The second chopper M19, M20, M21 and M22 demodulates the signal and modulates  $1/f$  noise and offset at odd harmonics. A cascoded mirror M24, M25, M12 and M14 performs a broadband differential to single ended conversion. The need for large bandwidth implies small transistor lengths for M12 and M14 and therefore extra offset and  $1/f$  noise. For this reason a third chopper is being introduced in the signal path: M27, M28, M29 and M30. The transistors M12 and M14 are dynamically matched [3] without consequences on signal. The unswitched cascode transistors provide further improvement in switching noise and residual offset by low pass filtering some of the HF noise components generated from chopping and keeping low voltage swings at their sources. In order to minimize substrate interferences, only PMOS transistors and NMOS switches with small dimensions are being used in the signal path [4]. The oxide capacitance of M34 decouples the BIAS line to VSS. Substrate interferences present in the sources of cascode transistors M23 and M26 will be also present at their gates such that gate source voltages of the same transistors can be considered constant for HF substrate noise [4]. For the same reason, the current sources M6 and M7 have their gates decoupled to VSS via a large capacitance.

### 3. NOISE AND OFFSET

Neglecting the noise introduced by cascode transistors and switches, the power spectral density of the white and  $1/f$  noise referred to the input is:

$$S_{v_{w+1/f}}(f) = \frac{8kT}{3g_{m2}} * 2 \left[ 1 + \frac{g_{m6}}{g_{m2}} + \frac{g_{m12}}{g_{m2}} \right] + \frac{k_{FP}}{(W_2L_2)f} * 2 \left[ 1 + \frac{k_{FN}}{k_{FP}} \frac{(W_2L_2)}{(W_6L_6)} \left( \frac{g_{m6}}{g_{m2}} \right)^2 + \frac{(W_2L_2)}{(W_{12}L_{12})} \left( \frac{g_{m12}}{g_{m2}} \right)^2 \right] \quad (1)$$

where  $k_{FN}$  and  $k_{FP}$  are process dependent constants. Large transconductances of the differential input pair give low white noise.  $1/f$  noise can be minimized by increasing the area of the input pair and increasing the transconductance of the input transistors in comparison to the transconductances of M6 and M12. If  $\Delta V_T$  denotes the threshold mismatch,  $\Delta\beta/\beta$  the relative gain factor mismatch,  $V_{GT}$  the effective gate voltage ( $V_{GS}-V_T$ ),  $n$  the slope factor and  $U_T$  the thermal voltage, the offset voltage referred to the input can be computed from:

$$\sigma(V_{Os}) = \sqrt{\sigma(\Delta V_{T2})^2 + n^2 U_T^2 \sigma\left(\frac{\Delta\beta_2}{\beta_2}\right)^2 + \frac{16n^2 U_T^2}{V_{GT12}^2} \sigma(\Delta V_{T12})^2 + 4n^2 U_T^2 \sigma\left(\frac{\Delta\beta_2}{\beta_2}\right)^2 + \frac{32n^2 U_T^2}{V_{GT6}^2} \sigma(\Delta V_{T6})^2 + 8n^2 U_T^2 \sigma\left(\frac{\Delta\beta_1}{\beta_1}\right)^2} \quad (2)$$

The dominant terms in the offset voltage are due to the threshold mismatch of the input pair and the threshold mismatch of M12 and M14. Large phase margins can be obtained when M12 and M14 have small lengths. This increases their contribution to the offset and noise. Dynamic element matching is being used to reduce this effect. Fig.2 shows the simulated static dynamic range of the OTA and the static offset as a function of the bias current JBIAS. The OTA has been configured as a follower with 10MHz gain bandwidth product (GBW). By scaling down the current according to W scaling [1] and keeping the same power supply voltage and GBW, a factor 10 reduction in power gives a 10dB reduction in DR. This can be seen also from the DR\*GBW product of the OTA. If P denotes the total power,  $\Delta$  the saturation limits at the output node, n the slope factor and NEF the noise excess factor DR\*GBW is:

$$DR*GBW = \frac{P}{80\pi n KT NEF U_T} \left(1 - \frac{2\Delta}{V_{DD}}\right)^2 \quad (3)$$

By chopping, the offset of the amplifier is removed in the same way as 1/f noise. Charge injection in the input modulator causes spikes at the input and this gives residual offset. The residual offset in a follower configuration and after low pass filtering can be computed from:

$$V_{os,residual} = -V_{inj} \sum_{\substack{k=-\infty \\ k=odd}}^{\infty} \frac{4}{jk\pi} \frac{T_o/T}{\left(1 + j2\pi \frac{k/T}{g_{m2}/C_{gs23}}\right) \left(1 + j2\pi k \frac{T_o}{T}\right)} \quad (4)$$

$V_{inj}$  represents the amplitude of the spikes at the input,  $T_o$  the time constant of the charge injected, T is the chopping period and  $C_{gs23}$  the gate-source capacitance of M23 and M26. By using Poisson summation rule for series and considering  $g_{m2}/2\pi C_{gs23}$  larger than  $F_{chopp}$ , we get:

$$V_{os,residual} = V_{inj} \frac{g_{m2}/2C_{gs23}}{\left(1/2T_o - g_{m2}/C_{gs23}\right)} \left[ \frac{\tanh(T g_{m2}/4C_{gs23})}{T g_{m2}/2C_{gs23}} - \frac{\tanh(T/4T_o)}{T/2T_o} \right] \cong 2V_{inj}T_o F_{chopp} \quad (5)$$

This shows an increase of the residual offset with chopping frequency and the energy of the spikes.

#### 4. EXPERIMENTAL RESULTS

The chopped transconductance amplifier has been realized in a 0.5  $\mu\text{m}$  CMOS technology. For measurements purposes OTA has been configured as a follower with a bias current of 30  $\mu\text{A}$ . Fig.3 shows the static offset and the residual offset for 6 arbitrarily chosen circuit samples after low pass filtering the output. Without chopping ( $F_{chopp}=0$ ), static offsets of less than 680 $\mu\text{V}$  can occur. Chopping will reduce the offset for relatively low chopper frequencies but increasing the chopping frequency the residual offset will increase.

This is in close agreement with eq. (5). The

residual offset at 100KHz chopping frequency is less than 150 $\mu\text{V}$ . At low chopping frequencies, a minimum in residual offset occurs. Fig.4 shows the signal to noise plus distortion figure (SINAD) for 100KHz chopping and 1KHz input. The input signal at 0dB reaches 2.8Vpp where distortion is high and dominates SINAD. For low signal amplitudes the noise level is higher than the distortion level. The measured signal to noise ratio in audio band (0..20KHz) after chopping is -95dB and harmonic distortion (THD) is -89dB at -15dB signal level. Chopping increases signal to noise ratio with about 6dB. The same performance can be achieved without chopping but increasing the power consumption 4 times (2.4mW) as estimated by eq.(3). Fig.5 shows the chip photo and Table1 a performance summary of the circuit.

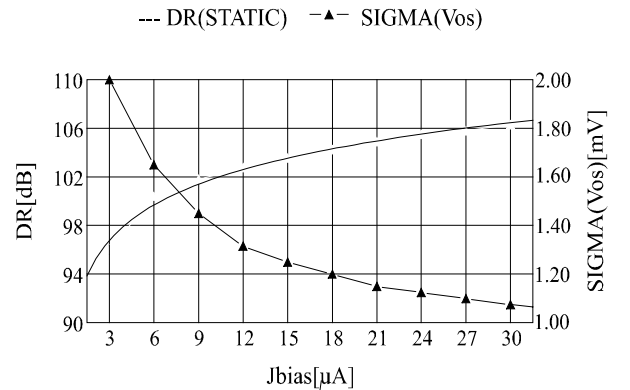
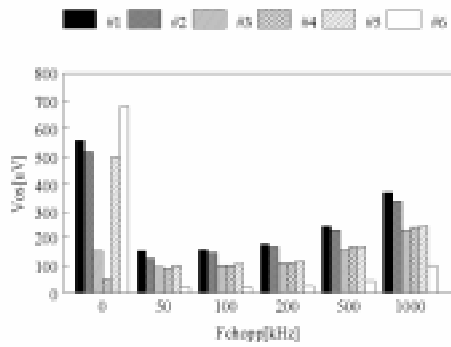
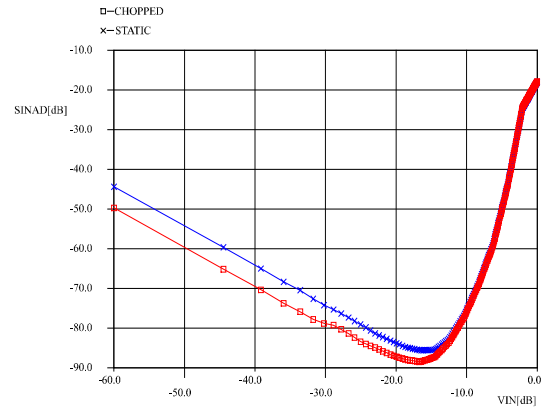


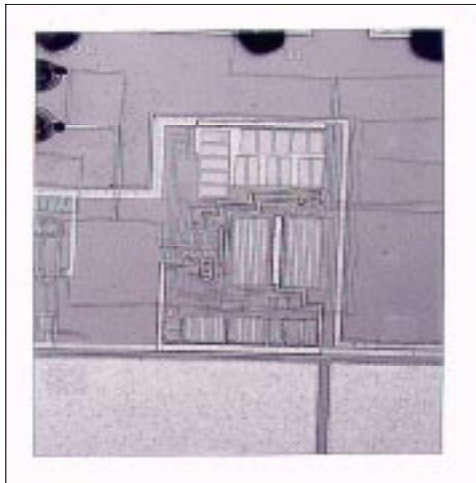
Fig.2: DR(static) and offset(static)



**Fig.3: Static( $F_{chopp}=0$ ) and residual offset**



**Fig.4: SINAD at  $F_{chopp}=93\text{KHz}$**



**Fig.5: Chip photo**

Open-loop gain	>75dB
GBW	10MHz
Offset(static)	<1.1mV
Offset(chopped)	<370 $\mu$ V
Chopping frequency	$F_{chopp} \leq 1\text{MHz}$
$S/N _{F_{chopp}=93\text{KHz}}$	95dB
$S/N _{F_{chopp}=0}$	89dB
Harmonic distortion	-89dB
Supply voltage	3.3V $\pm$ 10%
Power consumption	594 $\mu$ W
Technology	0.5 $\mu$ m, 2PS, 3AL, CMOS
Area	0.0308mm <sup>2</sup>

**Table 1: Performance summary**

## 5. CONCLUSIONS

A low-voltage, low-power, chopped transconductance amplifier for mixed analogue digital applications has been presented. Chopping and dynamic element matching allow low noise and low residual offsets up to 1MHz. The unswitched cascode transistors provide further improvement in residual offset and switching noise by low pass filtering some of the HF components generated from chopping. The sensitivity to substrate noise is taken into account in the design. Experimental results show residual offsets of less than 150 $\mu$ V at 100KHz chopping frequency and a signal to noise ratio in audio band of 95dB at 93KHz chopping. The power consumption is 594 $\mu$ W at 3.3V supply.

## ACKNOWLEDGEMENTS

The authors acknowledge the help of M. Dijkstra from Philips Research during measurements.

## REFERENCES

- [1] B. Nauta, "Analog CMOS low-power design considerations", *Low-Power Low-voltage workshop at ESSCIRC'96*, Neuchatel-Switzerland, September 1996.
- [2] K.C. Hsieh et al., "A low-noise chopper-stabilized differential switched-capacitor filtering technique," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 708-715, Dec. 1981.
- [3] R.J. van de Plassche et al., "A monolithic 14-bit D/A converter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp.552-556, June 1979.
- [4] B. Nauta and G.Hoogzaad, "How to deal with substrate noise in analog CMOS circuits", *European Conference on Circuit Theory and Design*, Budapest, September 1997.