

# A 200 MHz cell for a Parallel-Successive-Approximation ADC in 0.8 $\mu\text{m}$ CMOS, using a Reference Pre-Select scheme.

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**ABSTRACT:** A Successive-Approximation A/D converter cell for a Parallel-SA-ADC is presented. The ADC cell uses a Reference Pre-Select scheme, in order to minimize the decision loop in every binary search step, and make a high frequency operation possible. In binary search, we know that next step is to look at one of two possible references. This is utilized in three steps and the critical decision loop is minimized to “amplify the analog input to a digital signal and open one of two possible switches”. A comparator with differential return to zero output is developed for the fast decision loop. Measurements of a partly working test chip shows that 10 bits resolution at 200 MHz is possible. The ADC cell consumes 75 mW.

## 1. Introduction

Algorithmic A/D converters (pipelined or Parallel-Successive-Approximation A/D Converter, PSA-ADC) have recently become interesting for low power high speed ADCs, where communication electronics is driving the development. The research on PSA-ADC, has reported 10 bits at 70 MS/s, [1], and a product exists at 10 bits, 40MS/s, [2]. This paper considers the development of an ADC cell, aimed for a PSA-ADC, with focus on the speed limits in the SA-ADC structure. We present an implementation of a Reference Pre-Select, *RPS*, scheme, which minimizes the decision loop in the SA-ADC. A basically fast structure is useful when designing low power circuits, since speed can be traded for low power by simply lowering the power supply in the digital parts and lowering  $g_m$  requirements in the analog parts.

## 2. Reference Pre-Select scheme

Binary search among known voltage reference levels is an optimal algorithm for finding the correct digital code. The algorithm has one drawback from implementation point of view: there is a loop which cannot be pipelined. When we go from one comparison to the next, we are depending on the most recent search result. However, the number of possible references is limited. The number is doubled for each step ahead in

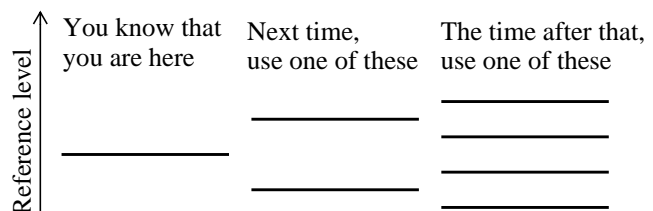


Fig. 1: Binary search Reference Pre-Calculation is possible. For every step ahead in time we look, the number of possible levels is doubled.

time we look, i.e., the “next time” we should use one of two possible levels and the “following time” one of four possible levels, Fig. 1. This can be used to pre-calculate the references as much as possible. The Reference Pre-Selections, *RPS*s, are only depending on “old data”, and are therefore possible to pipe-line and not time critical. By extensive use of Reference Pre-Select, the complexity and time delay in the final decision is minimized. The A/D conversion speed is thereby maximized.

### 3. Implementation

The SA-ADC structure is shown in Fig. 2, [3]. The analog input signal,  $V_A$ , is sampled in node  $Nd$  by opening the sampling switch  $S_S$ , as a charge

$$Q = V_A \cdot C_C.$$

The A/D converter uses three subranging stages (coarse,  $V_{RC}$ , middle,  $V_{RM}$ , and fine,  $V_{RF}$ ) with 3, 3 and 5 bits respectively, Fig. 2. These stages are added in node  $Nd$  through the capacitors  $C_C$ ,  $C_M$  and  $C_F$ . The search algorithm minimizes the charge in  $Nd$  by controlling  $V_R$ , as

$$Q = V_A \cdot C_C - V_{RC} \cdot C_C - V_{RM} \cdot C_M - V_{RF} \cdot C_F.$$

By letting the subranging stages overlap each other and calculate 11 bits, we get one bit redundancy, which is used for digital error correction, [4], and the result is a 10 bits conversion.

The *RPS* is implemented by separating the binary search control logic into three loops with 1, 2 and 3 clock periods length, respectively, Fig. 3. The first loop, *Loop1*, is the most time critical, and is minimized to the task “amplify (compare) the analog value to a digital level and open one of two analog switches, ( $S_a$  or  $S_b$ )”. The nodes  $Na$  and  $Nb$  holds the possible references for the comparison, and one of them is selected. One clock period in advance, *Loop2* has calculated these references and connected them to  $Na$  and  $Nb$ . In the same way, *Loop3* has selected four possible levels.

The comparator is built up by two differential amplifiers and four stages (*Compare*, *Latch*, *Hold* and *Save*) of Clocked Regenerative Comparators, *CRC*, with 1/2 clock period delay in each, Fig. 3. Circuit details for the positive edge triggered, *p*, *CRC* and the buffers are shown in Fig. 4. The *CRC* is designed for maximized  $g_m/C$ . The two differential amplifiers and the first *CRC* forms the *Compare* stage, which amplifies the analog signal. This stage is triggered on the negative clock edge, and input data must be valid for less than 1/2 clock period before the negative edge. The *Latch* stage outputs,  $latch-x$  and  $\overline{latch-x}$  controls  $S_a$  and  $S_b$ , and connects the reference value to the comparator input. These differential outputs are reset to *ZERO* and one of them evaluate to one, Fig. 5. They can therefore directly control the switches. One of  $latch-x$  or  $\overline{latch-x}$  will be high when the *Compare* stage reads the input.  $latch-x$  and  $\overline{latch-x}$  are self timed which makes the design of *Loop1* simple, and thus fast. The buffers and *CRC*s have dummy transistors that make the charge feed-through in the Miller capacitors differential, [5]. As seen in Fig. 5, only one of the data lines change value at reset, and without this compensation, the non-symmetric reset would cause a hysteresis in the comparator.

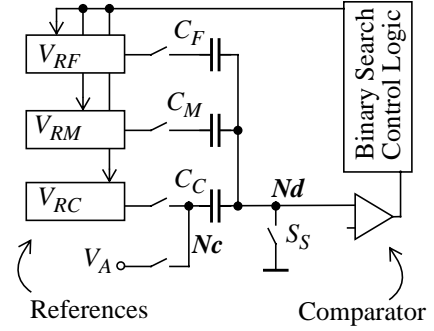


Fig. 2: Principle of ADC with subranging. Notice the nodes  $Nc$  and  $Nd$  for identification in other graphs. The  $S_S$  is the sampling switch and  $V_A$  is the input signal.



shows that *Loop1* and *Loop2*, i.e., the most critical loops, can handle a random data stream at full speed. By studying the level transitions in a slowly varying signal, the non-systematic noise level is estimated to  $< 63$  dB, Fig. 8. The quantization noise ( $> 62$  dB) will therefore dominate the output noise.

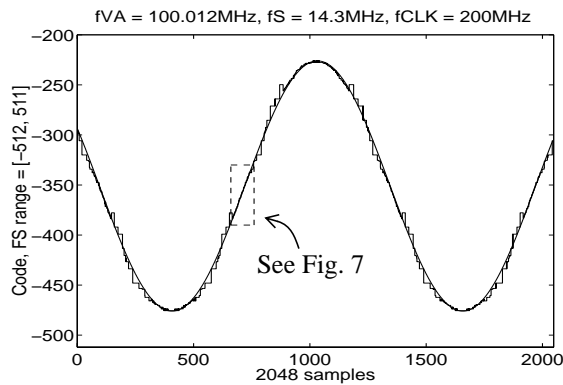


Fig. 6: Reconstructed output from the test circuit. Full scale is  $\{-512, 511\}$ . A part where the first sub-ranging stage is working is used. The second sub-ranging stage works partly, and for some regions, the ADC resolves 10 bits.

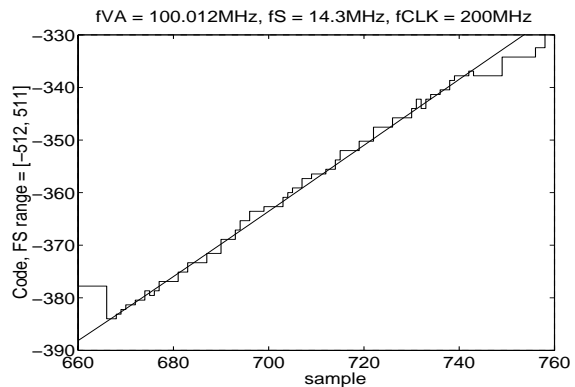


Fig. 7: A code segment where the most of the codes are working. This graph shows that *Loop1*, i.e., the most time critical, is working at 200 MHz, which is a very important result. It also shows that groups of codes are working at full speed.

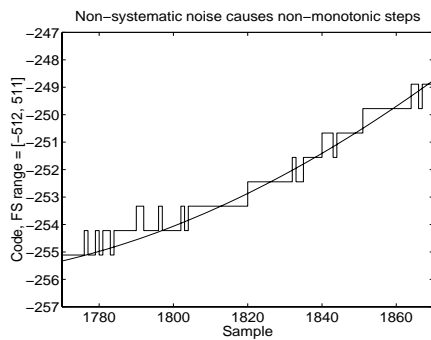


Fig. 8: Detail that shows the quantization step. The random errors origin in random noise, which is less than the quantization noise. *Loop1* and *Loop2* can detect the quantization step for 10 bits resolution.

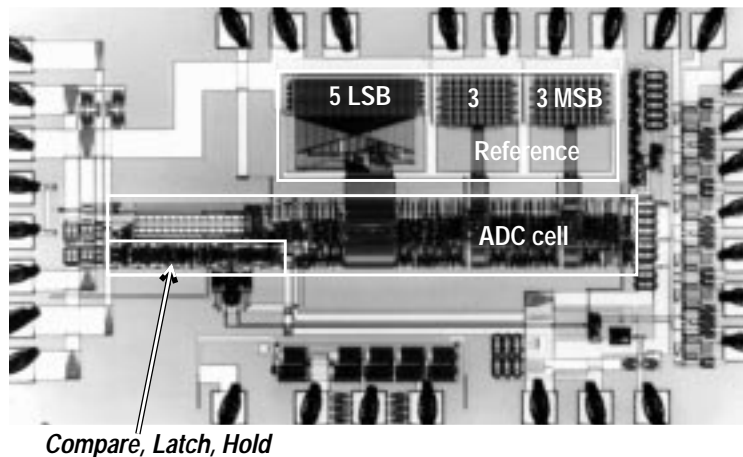


Fig. 9: Micro-graph of the test chip.

## 5. Conclusions

An ADC cell for a 10 bits, 200 MSample/s PSA-ADC has been demonstrated. By a Reference Pre-Select scheme, the critical loop is minimized, and the speed is increased three times, compared to, to the author known, previously reported PSA-ADC cells. Although only parts of the test circuit worked, the critical decision loop is verified by measurements.

## References

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