2.5Gb/s ATM Physical Layer Controller in 0.8μm BiCMOS

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Abstract

This paper presents two integrated circuits which together form a complete Physical Layer (PL) for 2.5Gb/s ATM. The two circuits are a Clock and Data Recovery unit with integrated demultiplexer, and a complex Transmission Convergence unit. The two circuits are manufactured in the same 0.8μm BiCMOS process, and could easily be combined to provide a single-chip solution.

1 Introduction

In the past the standard amount of memory in personal computers and workstations has been steadily increasing, to support ever increasing demands for graphically oriented applications. Today more and more computers are being connected to the Internet, and it is expected that the need for bandwidth will increase analogous to the increased demand for memory, to support new graphically oriented services. Also, it is expected that future networks support not only data traffic, but also a host of other digital telecom traffic, from voice to high-definition television.
ATM is a technology well suited for the Local and Wide Area Networks, designed to support telecom and data traffic with very different characteristics. Commercial ATM components with functions similar to the presented circuits are presently available at bitrates up to 622Mb/s, with economically attractive single-chip solutions only available up to 155Mb/s. In this paper we present two circuits, produced in the same 0.8μm BiCMOS process, which can easily be combined to provide a complete single-chip 2.5Gb/s ATM Physical Layer.
The first circuit presented is a 2.5Gb/s Clock and Data Recovery (CDR) unit [1]. The second circuit to be presented is a Transmission Convergence Unit (TCU), which is implemented exclusive in CMOS except for I/O structures where bipolar transistors are included. The TCU conforms to ITU-T recommendation I.432 [2], and has a transistor count of approximately 75,000. To reduce design time of the TCU, a design methodology utilizing the characteristics of ATM was used and will be described.

2 Design

The Physical Layer of the ATM protocol is subdivided into two layers, the Physical Medium sublayer and the Transmission Convergence sublayer. The characteristics of these two sublayers are quite different, the Physical Medium sublayer are mainly responsible for bit timing, i.e. Clock and Data Recovery, while the Transmission Convergence sublayer handles data processing issues such as cell delineation, cell rate decoupling and Operating and Maintenance operations.

The heart of the CDR unit is a Phase-Locked Loop (PLL), based on a novel Voltage Controlled Oscillator (VCO) generating accurate quadrature clocks [1]. The circuit also includes a 1:8 demultiplexer. The majority of the circuit is implemented using ECL style circuits, except the last stage in the demultiplexer, which uses True Single-Phased Clock (TSPC) CMOS [3].

The PLL in the CDR consists of a Phase-Frequency Detector (PFD), a Loop Filter and a VCO in a standard configuration. To achieve a symmetric pull-in range, the PFD requires a quadrature clock signal [4]. This is generated using the novel VCO structure shown in Figure 1 [1]. The VCO in Figure 1 is based on the work by Razavi and Sung [5]. By using a 6-stage ring, with two ring stages between transconductance amplifiers connected to the same load resistor, and connecting another set of transconductance amplifiers to the remaining ring nodes, an accurate 90° quadrature clock signal is generated at the cost of a lower oscillation frequency. The PLL dissipates approximately 250mW.

A basic tree-structure is used for the demultiplexer. The clock can be supplied by either the on-chip PLL or an external clock generator, enabling testing of the demultiplexer independent of the PLL. The 1:4 operation is implemented in ECL, while the final stage is implemented in CMOS using TSPC latches and flip-flops. Total power dissipation of the demultiplexer is approximately 800mW. All ECL circuits uses differential signals, while the CMOS parts uses normal single-ended full-swing signals. Conversion from the differential low-swing ECL signals to the full-swing CMOS signals are performed in the current mode ECL-CMOS converter shown in Figure 2. Compared to other ECL-CMOS converters, the current mode converter in Figure 2 is slower, but have symmetrical high-low and low-high propagation delays so that the conversion will not introduce duty cycle distortion.

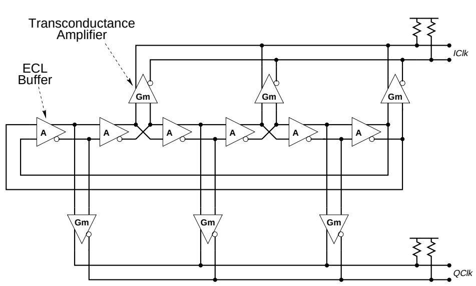

Figure 1 VCO schematic

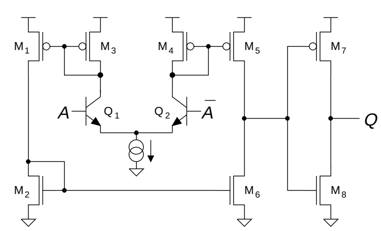

Figure 2 Current mode ECL-CMOS converter

The transmitter section of the TCU performs calculation and insertion of the Header Error Control field in cells, insertion of Operating and Maintenance (OAM) cells in the cell stream as well as scrambling of cells prior to transmission. A simple microprocessor interface is included in the transmitter, to enable the insertion of alarm information and for enabling and disabling of the scrambler.

In the receiver, the cell boundaries of the incoming cells are determined by searching for valid HEC values [2]. After the cell boundaries has been detected, the cells are descrambled and the OAM cells are extracted while the remaining cells are sent to the ATM layer for further processing. A microprocessor interface block continously collects status information about the receiver. Through this interface an external management system can retrieve information such as the number of received user cells, the number of discarded cells due to HEC errors, up-stream alarm information received through OAM cells, as well as state information for the individual blocks in the receiver.

The use of automatic tools for logic synthesis and layout can substantially reduce the design time of an integrated circuit. However, to obtain maximum performance it is necessary to both design and layout critical blocks by hand. By using a systematic approach we were able to partition the design so that the majority of the circuit could be designed using automatic tools, without impacting the overall performance. The methodology used were based on the fact that many events in an ATM circuit are related to cells, not to individual bits or bytes. From a HDL description of the circuit, cell related and byte related behaviour can be identified, and the circuit can be split into blocks operating on cells and bytes respectively. Information in cell related events need only be updated once for every cell, thus circuit blocks operating on cells can use a much lower clock frequency, enabling the use of automatic tools. It should be noted that the circuit blocks which are generated using automatic tools are mainly random logic blocks, which are the most time consuming block, both in terms of logic design and layout. It is estimated that this methodology reduced the design time by more than 50%.

Target operating frequency of the TCU high-speed blocks is 311MHz. To achieve this clock frequency a maximum logic depth of three to five can be accepted, resulting in a fine grained pipelining with a large number of flip-flops. To reduce clock load and area taken up by flip-flops, TSPC flip-flops were used. For blocks operating at lower clock frequencies, static CMOS flip-flops were used.

3 Implementation

Both the CDR unit and the Transmission Convergence unit were implemented in a 0.8μm BiCMOS process. The CDR operates at the high bit rate and therefore is implemented mainly using bipolar transistors. In Figure 3 a micrograph of the CDR implementation is shown. The full CDR circuit with demultiplexer is seen on the left hand side of the micrograph, while a test VCO and CDR (PLL plus a Master-Slave Flip-Flop) are implemented in the lower and upper right hand corners respectively. These test circuits are included to enable individual testing and characterization of the VCO and CDR blocks. The CDR with demultiplexer occupies an area of $0.75 \times 1.5\text{mm}^2$.

Die size of the TCU is $7.2 \times 6.7\text{mm}^2$, with a transistor count of approximately 75,000. A micrograph is shown in Figure 4.

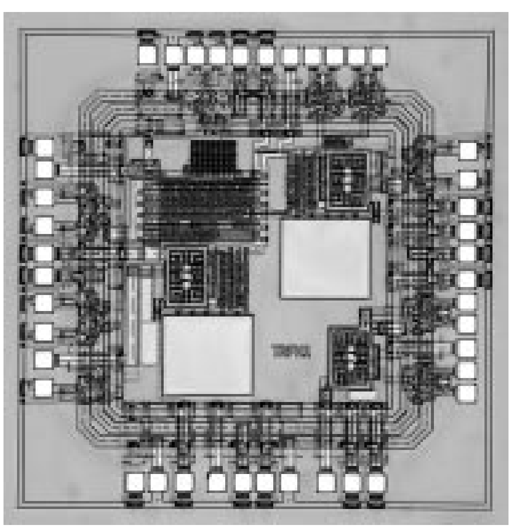

Figure 3 Micrograph, Clock and Data Recovery Unit with Demultiplexer

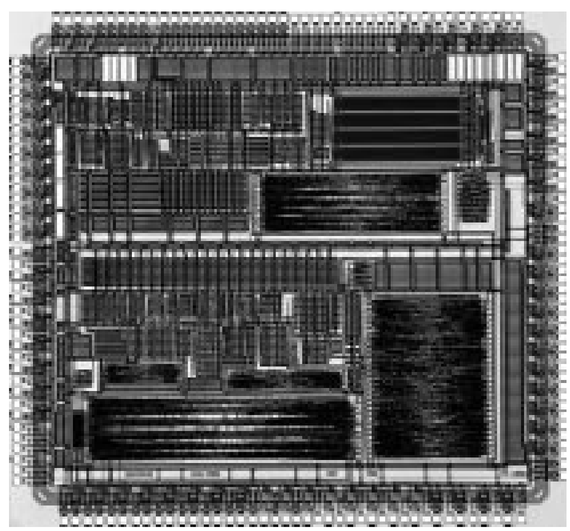

Figure 4 Micrograph, Transmission Convergence Unit

4 Experimental Results

At the present time, experimental results are available for the CDR circuit. Figure 5 shows the spectrum of the extracted clock at 2.5Gb/s, the spectrum is typical of a locked PLL. In Figure 6 the output from the digital oscillope during jitter measurement on retimed data is shown, RMS jitter was measured at 18.1ps. After adjusting for systematic jitter in the measurement setup, RMS was determined to be 11.6ps for the extracted clock, and 14.6ps for the retimed data. The full circuit, including demultiplexer and bit-rotation block, was verified at 2.5Gb/s. The core CDR circuit dissipates approximate 250mW.

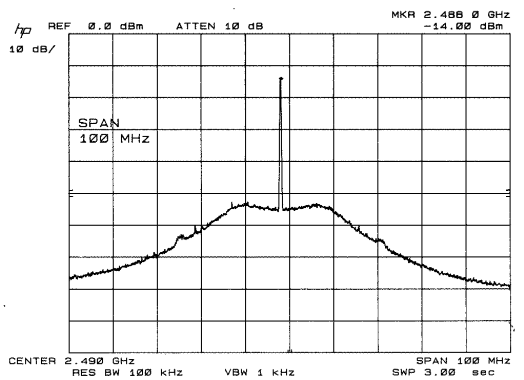

Figure 5 PLL spectrum, locked

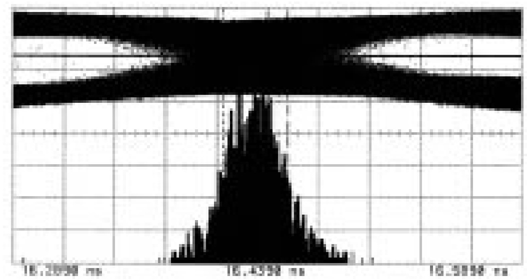

Figure 6 Jitter measurement, σ=18.1ps

5 Conclusion

This papers has presented two circuits, implemented in the same 0.8μm BiCMOS process. A 2.5Gb/s CDR circuit with integrated demultiplexer was presented, the circuit was implemented mainly using bipolar transistors, measured jitter for the extracted clock was 11.6ps. A Transmission Convergence circuit implemented mainly in CMOS, designed for an operating frequency of 311MHz was also presented. Together, these circuits demonstrate that it is possible with current mainstream technology to achieve both the high complexity and high speed of 2.5Gb/s ATM in a single-chip solution.

References

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