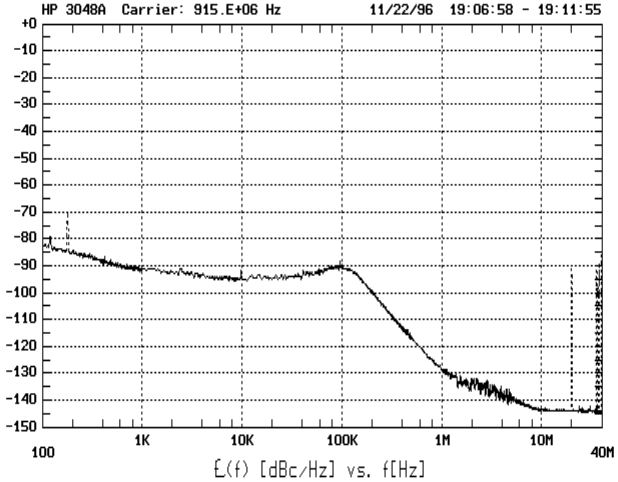

Fig. 3 - SSB Phase Noise at 915 MHz

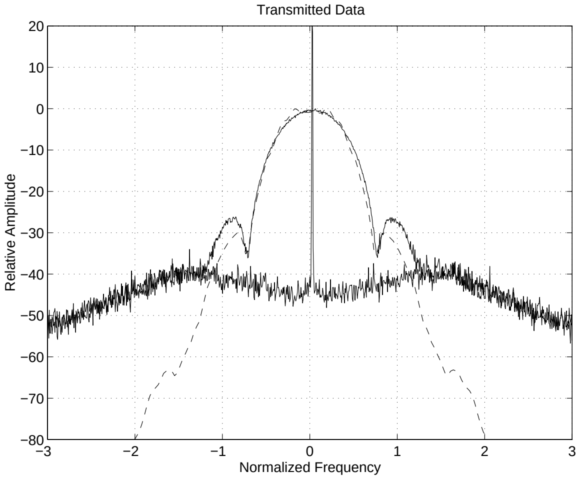

Fig. 4 - GMSK Data Spectrum

CHIP	VDD (V)	POWER (mW)	F_{REF}(MHz)	DATA RATE
CMOS	3.0	14.0 @ 20 MHz	50.0 max	156.25 Kb/s max
			RF_{in}(GHz)	**F_{REF} (MHZ)**
Bipolar	3.0	18.0	1.2 max	300.0 max

Table 1: IC Measurements

4 Conclusions

It has been demonstrated in this paper, that by incorporating a digital sigma-delta modulator, a fractional-N frequency synthesizer can be designed which has good spurious performance, low phase noise, and fast settling times. The synthesizer can be controlled with high accuracy, allowing direct digital modulation at RF with GMSK data.

Acknowledgments

The Authors would like to thank Nortel department 5C60 for supporting the initial synthesizer work, including the bipolar design, and department 5S12 for supporting the CMOS digital modulator work.

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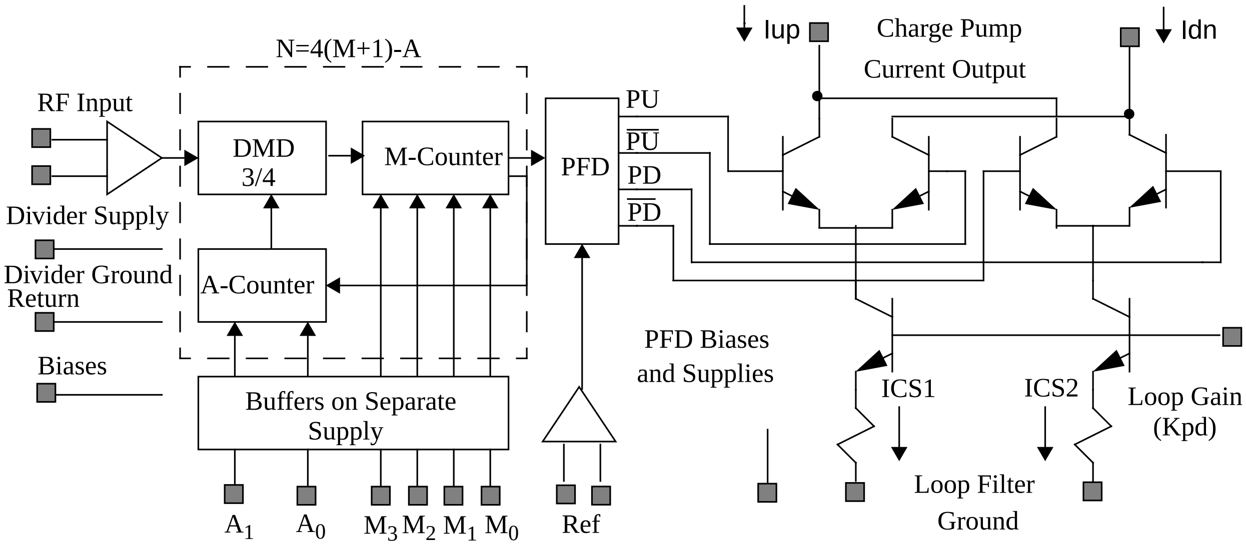

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Fig. 2 - Block Diagram of Bipolar Chip

The phase/frequency detector (PFD) indicated in Figure 2 is a standard architecture similar to the Motorola 4044 or 12040. It is built in ECL rather than CML to allow easy design of a reference voltage for single ended logic gates.

3 Measurement Results

A single-sideband (SSB) phase noise plot for the synthesizer in fractional-N operation at a frequency of 915 MHz is shown in Figure 3. The only spurs present in the output spectrum are the 20 MHz reference frequency feedthrough at -90 dBc and a harmonic of 60 Hz power line noise at -70 dBc. It is important to note that the inband phase noise at the synthesizer output was the same for both integer operation and fractional operation. This means that the sigma-delta modulator does not affect the inband phase noise characteristics of the synthesizer. The phase noise of the VCO was measured separately from the synthesizer and found to be less than -110 dBc/Hz at offsets greater than 10 KHz from the carrier. This means that the inband phase noise floor of the synthesizer, at -90 to -95 dBc/Hz, is due to the bipolar synthesizer chip. A more stringent phase noise floor specification would require higher power in the bipolar chip. A spur free range of 19.6 MHz was achieved, with a settling time that ranged from 30 uS to 60 uS for frequency steps of up to 8.4 MHz.

A plot of the downconverted GMSK transmit spectrum is shown in Figure 4 along with a plot of the theoretical spectrum for GMSK with a BT of 0.5. The horizontal frequency axis is normalized by the data rate. A plot of the downconverted and unmodulated carrier is included as well. From this plot it can be seen that the theoretical and measured spectra agree closely. The level of the sidelobes for the measured spectrum is slightly higher than theory due to the limited stopband attenuation of the Gaussian filter. By comparing the spectra of the modulated and unmodulated carriers, it can be seen that the noise floor of the modulated carrier is due to the inband and out of band phase noise of the PLL and not a non-ideal effect in the GMSK filtering.

Table 1 summarizes the measurement results for the bipolar and CMOS chips respectively. It can be seen that the combined power consumption of the two chips is 32 mW. The synthesizer presented in [3] had a power consumption of 27 mW, but did not include on chip data filtering.

software level and a hardware modulator was never combined with an integrated sigma-delta controlled synthesizer. A recent synthesizer presented in [3] allows high speed modulation outside of the loop bandwidth through the use of a pre-emphasis filter, but the data filter was not integrated along with the synthesizer.

2 Synthesizer Design

A block diagram of the frequency synthesizer of this paper is shown in Figure 1. The design was partitioned such that the high frequency components of the PLL are implemented in a high quality bipolar process and the digital sections are implemented in a high quality CMOS process. The two chips were mounted on a four layer printed circuit board along with an external loop filter and a commercial VCO.

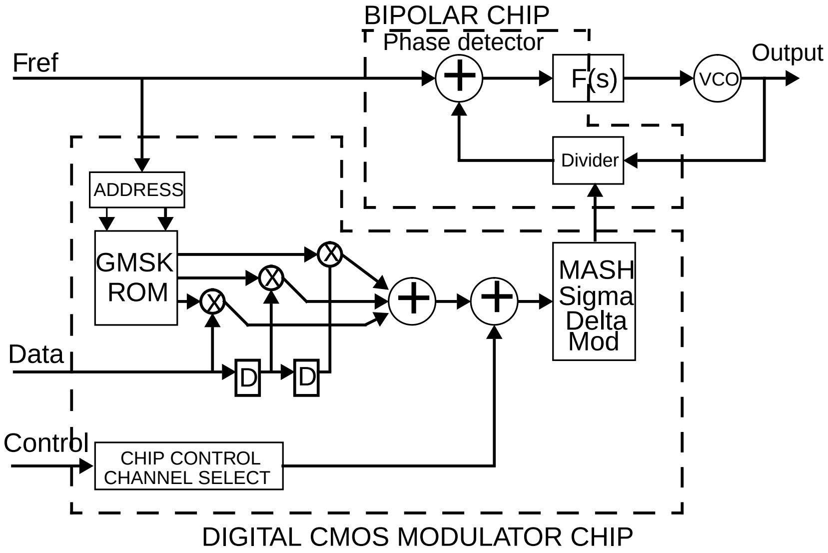

Fig. 1 - Synthesizer Block Diagram

The synthesizer was designed to be part of a frequency-hopping transmitter that would operate in the lower instrumentation scientific and medical (ISM) band from 902-928 MHz. The data rate is 62.5 Kb/s with GMSK pulse shaping with a BT of 0.5. The GMSK transmitter architecture used eliminates the need for the I and Q channels, D/A converters, summers, and upconversion normally used in GMSK data transmission [5]. The tap coefficients were quantized to single bit values using a software sigma-delta modulator prior to storage in the on-chip ROM. These single bit tap coefficients are fed out at an oversampled rate equal to the loop reference frequency. The average value of the tap coefficients is equal to the desired Gaussian pulse and the highpass filtered quantization noise is subsequently filtered out by the PLL. In this way, high resolution is obtained from single bit tap coefficients. The total memory storage space required to store the filter tap coefficients is 960 bits, significantly lower than what would be required if a standard filtering approach was used.

The loop bandwidth was 100 KHz, wide enough to achieve fast settling times and accommodate the transmitted data. The loop filter used consists of an integrator with phase lead correction. Two additional real poles were added to the loop in order to reduce reference feedthrough and out of band quantization noise. The reference frequency was chosen to be 20 MHz, and the sigma-delta modulator consists of a fourth-order MASH architecture incorporating four digital accumulators.

A block diagram of the bipolar chip is shown in Figure 2. The chip consists of a multi-modulus divider and a phase/frequency detector with an output charge pump. The divide ratios range from nine to sixty-four in steps of one, allowing versatility of application. CML logic is used wherever possible in the design and the tail currents were set to the lowest values possible.

AN LOWER ISM BAND FREQUENCY SYNTHESIZER AND GMSK DATA MODULATOR

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Abstract

In this paper a high resolution fractional-N RF frequency synthesizer is presented which is controlled by a fourth-order digital sigma-delta modulator allowing the synthesizer to be digitally modulated directly at RF. For data transmission a simplified digital filter which makes use of sigma-delta quantized tap coefficients is included which provides built in GMSK pulse shaping. The synthesizer makes use of two custom chips, with only a simple off chip loop filter and VCO required. The synthesizer operates from a single three volt supply and the two chips consume a total of 32 mW.

1 Introduction

Future frequency synthesizers for use in mobile radio applications should be suited for VLSI implementation and have low power consumption. In addition to providing a fixed local oscillator (LO) in a receiver, a frequency synthesizer may be called on to be agile in its frequency control, for instance, in spread-spectrum applications. Synthesizers used in such applications must have fast settling times and good spurious performance. Sigma-delta controlled fractional-N frequency synthesis can meet these requirements [1],[2],[3]. Unlike direct digital synthesis (DDS), no upconversion is required and the modulated signal can be synthesized directly at the RF frequency with comparable performance. The high resolution achieved allows accurate modulation of the carrier at RF frequencies.

In the transmission of digital data, some form of baseband pulse shaping is required to control the RF bandwidth [4]. A method has been presented whereby the tap coefficients for a digital pulse shaping filter could be quantized to single bit values, using a software sigma-delta modulator, prior to storage in a ROM [5] with the potential for greatly reducing the required storage space and simplifying the multiplications required to single bit operations. Although the work presented in [5] showed the feasibility of this method the demonstration was partly done at the