1.25 Gb/s CMOS Differential Transimpedance Amplifier For Gigabit Networks

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Abstract: We present a CMOS transimpedance amplifier that operates beyond 1.25Gbit/s data rate. A fully differential architecture is adopted to enhance stability as well as to improve dynamic range and common-mode rejection. A special buffer and careful layout were employed to generate fully balanced differential outputs from a DC-coupled single-ended input.

1 Introduction

Recent advances in computer and networking technologies have revolutionized the way in which people communicate and conduct business. The increasing popularity of the Internet and the dramatic increase in the number of subscriber nodes world-wide, as well as the desire to support wideband multimedia data are stressing the need for a drastic increase in network bandwidth, fueling the current efforts to develop the next generation of high-speed networks such as the Gigabit Ethernet. The emergence of gigabit networks underscores the need for low cost, high-performance components that can support Gbit/s data rates. Although copper cable combined with sophisticated signal processing can provide an interim solution, optical fiber is the preferred physical medium for its robustness and simpler system implementation due to its almost unlimited bandwidth. More importantly, the key interface IC's need to be manufactured using the most widely available, thus lowest cost IC technology such as CMOS. The transimpedance amplifier (TIA) is a critical block of a fiber-optic receiver. Its noise performance, gain, and frequency response largely determine the overall sensitivity and the data rate of the optical link. Here we describe the design and test of a new differential transimpedance amplifer implemented in a commercially available 0.6μm CMOS technology.

2 Differential Transimpedance Amplifier

Although high-speed transimpedance amplifiers have traditionally been implemented using single-ended topologies for simplicity, a differential configuration offers a number of significant advantages, especially in CMOS technology. First, the common-mode rejection property inherent in a differential circuit makes it far more manageable to integrate TIA with noisy digital circuitry or with other TIA's in an array with minimal crosstalk. Second, since relatively low g_m of a MOS transistor fails to provide large enough open-loop gain with a single gain stage, a cascade of gain stages is required. However, in a single-ended implementation, three gain stages are typically used to render overall feedback negative, which results in excessive phase shift and thus poor stability due to the presence of three secondary poles. An extremely large feedback resistor is required to improve phase margin, thus resulting in lower overall bandwidth[1]. The employment of a differential architecture makes it trivial to apply negative feedback with just two gain-stages, resulting in a more stable amplifier compared to the three-stage design. Finally, single-ended amplifiers can saturate with large inputs, which causes asymmetric output and degraded output eye-diagram, unless automatic gain control circuitry is employed to degenerate the transimpedance gain. In contrast, differential transimpedance amplifier essentially works in the same manner as a differential pair in emitter-coupled-logic (ECL), where larger inputs can even be beneficial for faster output switching. Hence, a differential scheme results in good dynamic range with less complexity than a single-ended implementation. A differential architecture does suffer from one drawback, however. For single-ended implementations which use a single photo-diode, a dummy capacitor needs to be connected to the complementary input to ensure symmetry at higher frequencies. This is not a serious concern since a programmable capacitor can easily be integrated on chip to match photodiodes with a wide range of capacitance values.

3 Circuit Design

The design of the voltage gain block is crucial since its open loop gain and frequency response directly relate to the bandwidth and stability of the transimpedance amplifier. Gain-enhancing techniques commonly used in CMOS operational amplifier design are not suitable, since the dominant pole is already located at the input, not at the output of the gain-stage. What is required is a amplifier stage with small, manageable gain and the highest possible 3-dB bandwidth. Gain needs to be stable over process, since gain fluctuations of one stage causes exponential variations in the overall open-loop gain when stages are cascaded. An NMOS differential amplifier with diode-connected NMOS loads provides a stable gain which is to the first order determined by the ratio of the respective widths of the g_m element and the load (neglecting body effect). However, a large gate-to-source voltage is required to keep load devices turned on as well as to support the same current flowing through the g_m element. This severely compromises the voltage headroom, making the configuration not feasible for low power supplies such as 3.3V. We chose to employ PMOS transistors in triode region as loads, in the pseudo-NMOS fashion. Gain is controlled through the implicit feedback in the current source bias generator shown in Figure. 2.

The feedback resistor for the transimpedance amplifier was implemented using a pair of PMOS transistors which is essential in maintaining good stability over process variations. This can be explained as follows. Lower transconductance, thus higher resistance of the PMOS loads causes secondary poles of the gain stages to move to a lower frequency. To preserve good phase margin, the dominant pole has to move down as well, which requires a larger feedback resistor. However, this condition has already been satisfied since the PMOS feedback transistor is more resistive due to its smaller transconductance. Similar mechanisms apply to other process corners.

Although the above transimpedance amplifier is fully differential, it should operate properly with single-ended DC-coupled inputs which is the required condition in most fiber optic links. Especially, the logic “zero” can represent a highly ambiguous state for the following quantizer or decision circuit and unless properly addressed can result in severe duty-cycle distortion or no output switching[2]. This problem can be eliminated by treating the differential amplifier as two single-ended amplifiers in parallel. Since in most applications input data is encoded to be DC-balanced, decision thresholds can be extracted for each half through low-pass filtering and fed to the output buffer. The respective outputs of each half are power-combined by the buffer, thus preserving the beneficial properties of the differential amplifier as illustrated in Figure 2. This is a more feasible solution than simple AC-coupling which requires large off-chip capacitors. The low-pass filter is implemented using a long channel CMOS resistor and polysilicon linear capacitor and results in low-frequency cutoff of about 50KHz. CMOS resistor was used due its better dynamic range compared to a single PMOS device.

3 Test Results

The chip was fabricated using the MOSIS 0.6μm CMOS process with linear capacitor option. To facilitate testing, the amplifier was characterized electrically, by inserting a large series resistor between a 50Ω signal source and the input of the IC. A 320fF capacitor connected at the input emulates the photodiode capacitance. Frequency response of the transimpedance amplifier is shown in Fig.3. The circuit was biased with a single power supply voltage of 3.3V. The amplifier has differential on-chip gain of 67dBΩ and 3-dB bandwidth of close to 860MHz, which improves to 920MHz by increasing the power supply to 3.6V. The differential outputs were matched to within 0.05dB. In bit-error-rate (BER) measurement, BER of 3.3×10^{-10} was achieved at 1.25Gb/s with pulsed input current of 5μA, which corresponds to -23dBm sensitivity. It should be noted that sensitivity is degraded by the thermal noise of the input 50Ω termination resistor and the input series resistor. We predict a 3dB improvement in a purely optical test. The amplifier operates properly without errors with input currents as large as 500μA. The output eye-diagram with 100μA 1.25Gb/s $2^{23}-1$ input is shown in Figure 4. The output buffer worked as designed, producing balanced outputs with a DC-coupled input current as shown in Figure 5. The IC consumes 130mW from a single 3.3V supply.

REFERENCES

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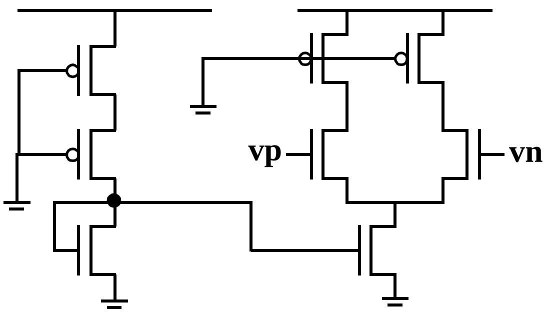


Figure 1: TIA Gain Cell with Bias Generator

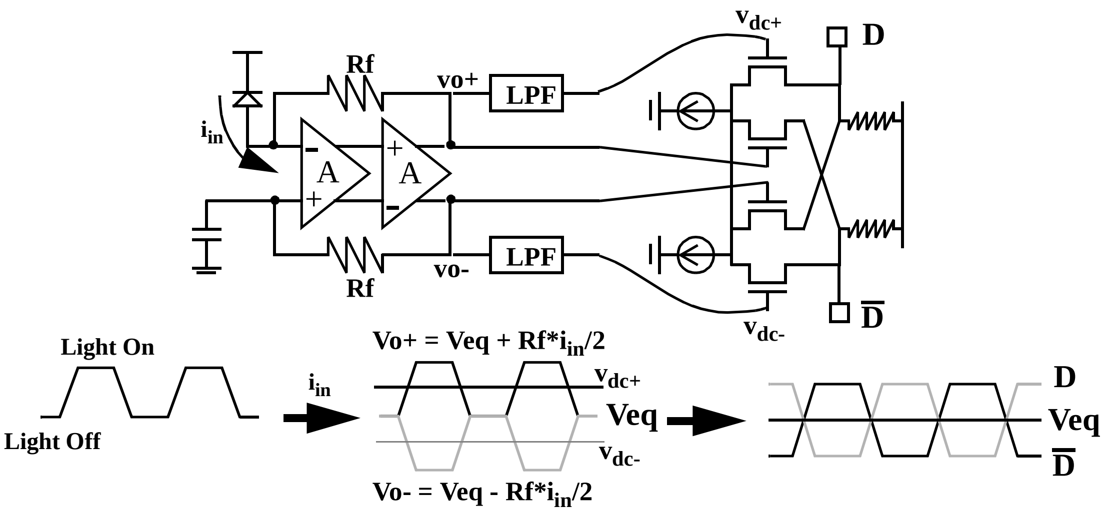
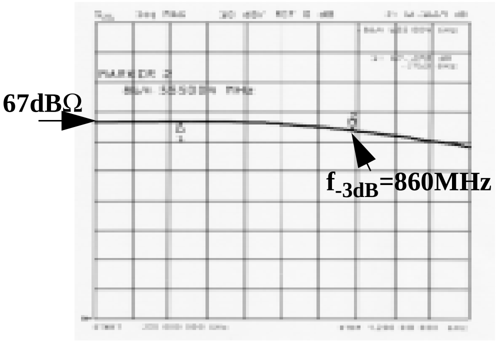


Figure 2: Output Buffer Operation



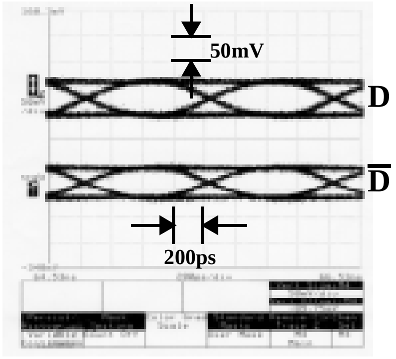
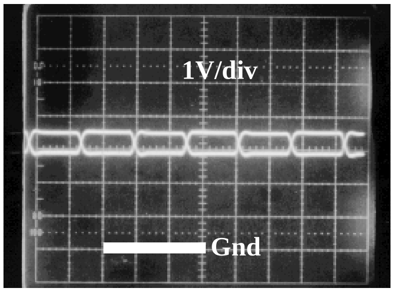


Figure 3: Amplifier Frequency Response

Figure 4: Output Eye-Diagram at 1.25Gb/s



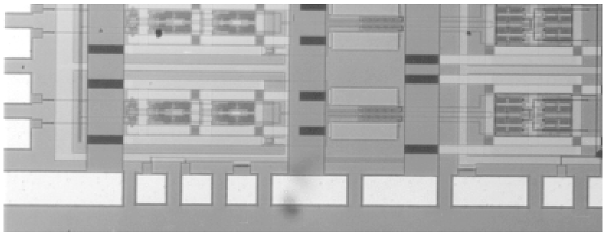


Figure 5: Amplifier Differential Outputs with a 3 MHz DC-coupled Input

Figure 6: Chip micrograph. Active area is $0.5mm^2$