

# A wide band Tuning System for Fully Integrated Satellite Receivers

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## Abstract

The building blocks for a low power tuning system that reduces the phase noise of integrated VCO's are described. The multi-modulus prescaler, the phase frequency detector and the wide band charge pump were integrated in a standard bipolar technology with 9 GHz npn-transistors and 200 MHz pnp-transistors. The maximum input frequency of the multi-modulus prescaler is 3 GHz, the maximum reference frequency of the phase frequency detector is 380 MHz and the -3 dB bandwidth of the charge pump is 41 MHz at a reference frequency of 300 MHz. The achieved performance enables use of noisy integrated VCO's for reception of satellite digital signals.

## 1. Introduction

Direct-conversion architectures offer a high degree of integration at the cost of some specific problems like LO-leakage and I/Q matching. A key circuit for direct-conversion receivers is a fully integrated oscillator with quadrature outputs covering the total input frequency range [1]. For large input frequency range systems (e.g. for satellite reception) this oscillator will likely be of the RC type, because the tuning range and the required accuracy of the quadrature signals is achievable with low power dissipation [2]. Furthermore, a fully integrated RC oscillator decreases the LO leakage and self reception problems. Draw-back of RC oscillators is their relatively high level of phase noise when compared to LC oscillators. To achieve the phase noise specification of modern digital transmission system RC oscillators require wide band phase frequency locked loops (PPLL's) with high reference frequencies for reduction of phase noise [3]. This paper will describe the architecture and circuit implementation of building blocks suitable for a wide band tuning system able to perform phase noise reduction of integrated VCO's: a low power multi-modulus prescaler and a 300 MHz phase frequency detector/single ended charge pump combination (shaded blocks in figure 1).

## 2. Architecture of Fully Integrated Satellite Receiver and its Tuning System

The architecture of the Fully Integrated Satellite Receiver is shown in figure 1. The integrated RC oscillator supplies the I/Q signals for the quadrature mixers, converting the RF signal to base band. The frequency of the RC oscillator is locked to a crystal oscillator with a double loop tuning system [3]. Channel selection is accomplished by switching the division ratio of the main divider in loop 2, in this way stepping the frequency of the VHF VCO. As the RC oscillator is locked to the VHF VCO via the multi-modulus prescaler Nband, its frequency will be stepped as well, and another channel will be converted to baseband.

The advantages of using the double loop architecture is that very wide bandwidths can be employed in loop 1 (reference frequency in the VHF range), enabling a clean-up action on the phase noise of the RC oscillator. Furthermore, by switching the division ratio of the multi-modulus prescaler Nband the necessary VHF VCO tuning range and sensitivity will decrease, because its output frequency range can be used for different RF-input frequency bands. The other advantage of the double loop architecture as presented is that all the oscillators frequencies have an integer relationship, so that the risk of spurious signals due to oscillators coupling is not present.

The input frequency range (950 MHz-2150 MHz) was divided in four bands, corresponding to division ratios in the programmable prescaler of 4, 5, 6 and 7. This determined the tuning range of the VHF VCO to be from 237 MHz to 307 MHz, and therefore the highest operation frequency of the phase frequency detector/charge pump combination PFD/CP1 (307 MHz).

### **3. Circuit design and topology of Programmable Dividers**

The architectural choice for implementation of the multi-modulus prescaler is shown in figure 2. It consists of  $2/3$  divider cells that can be combined to achieve the necessary range of division ratios. As the input frequency for each cell is divided by two by the preceding cell, scaling of power dissipation is easily and reliably accomplished because no long delay paths are present, in contrast to frequency dividers employing the dual-modulus prescaler architecture. Furthermore, adaptation of the input frequency range can be done by adding or removing cells from the chain, without having to redesign (and relayout) the existing cells.

The programmable prescaler in loop 1 has to divide from 4 to 7, so two  $2/3$  bit cells provide the necessary division ratios. The circuit implementation of a  $2/3$  cell as used in the tuning system is shown in figure 3. It is based on the Current Routing Logic (CRL) principle [4]. This type of logic family is very suitable for low power/low cost (small chip area) applications. The circuit shown in figure 3 embodies five D-type flip-flops and three logic gates, all stacked into four current sources (an additional current source is used for generation of a reference voltage for the logic functions). The current level was set at  $500\mu\text{A}$  per current source in the first cell, and at  $250\mu\text{A}$  per current source in the second cell. The programmable prescaler divided properly up to a frequency of 3 GHz, with a nominal power dissipation of 25mW.

### **4. Circuit design and topology of a 300 MHz Phase Frequency Detector/Single ended charge pump combination**

Usually high frequency PLL's apply simple EXOR phase detectors in order to keep power dissipation and complexity as low as possible. However, these traditional PLL architectures have pull-in ranges which are insufficient for many practical applications. Large pull-in ranges require more complex phase frequency detectors (PFD) with higher power dissipation. For maximum flexibility/low cost applications these PFD have to be combined with single ended charge pumps (SECP) instead of complementary ones which require active loop filters.

Traditional PFD/SECP's in standard technologies are limited in their high frequency operation by the slow switching speed of the pnp-transistors in the charge pumps. These limitations can be avoided by a new architecture where the PFD/SECP is mapped in an optimum way on the standard technology (Figure 5). The PFD circuit design has been optimized for high speed and low power dissipation by using dedicated ECL circuit design. It operates up to 380 MHz with a nominal power dissipation of 10mW (5 V, 2 mA). The switching part of the charge pump is using fast npn-transistors in an optimized switching mode. These current switches are succeeded by matched current mirrors using slow pnp-transistors with  $f_t \sim 200$  MHz. Their transfer function dominates the dynamic transfer function of the PFD/SECP. The current mirrors are designed to combine maximum accuracy (base current compensation) with maximum bandwidth.

In order to realize the required single ended charge pump function another npn-current mirror is added in the down-branch. In principle this function introduces an asymmetry, but due to the large difference in cut-off frequencies of the transistors its influence is negligible. The circuit implementation of the SECP is shown in figure 4.

Figure 6 shows the static transfer function of the PFD/SECP vs. phase error for two different reference frequencies. Due to the internal delay of the reset pulse in the PFD the maximum phase error for proper operation becomes a function of the reference frequency. From Figure 6 it can be seen that PFD works correctly within  $\pm 160^\circ$  at 200 MHz, and within  $\pm 60^\circ$  at 300 MHz. Furthermore, it shows that the PFD/SECP has no dead zone, although none of the usual dead zone compensation techniques with additional delay in the PFD reset pulse [5] are included. Additional delay in the reset pulse would prevent the PFD from operating in the VHF range, as required in this application.

Figure 7 shows the dynamic transfer function of the PFD/SECP vs. modulation frequency. The transfer function is dominated by the slow pnp charge mirrors and the capacitive load at their input resulting from the Miller capacitance of the npn current switch. The bandwidth of 41 MHz is independent of the modulation index, and large enough to remove the dominant phase noise of (integrated) VCO's.

Figure 8 shows an application of the integrated PFD/SECP, the programmable prescaler and a VCO operating at 1.75 GHz. The loop bandwidth implemented via an external loop filter was 2 MHz, which is much smaller than the internal bandwidth of the PFD/SECP. With this configuration the jitter of the VCO - or the square root of the integral of the phase noise power density between 1 kHz and 10 MHz - is reduced from  $13^\circ$  to  $0.7^\circ$ .

## 5. Conclusions

This paper described a tuning system including a multi-modulus prescaler and a high frequency phase frequency detector/wide band single ended charge pump which are integrated in a standard bipolar technology ( $f_t \sim 9$  GHz). The tuning system enables wide loop bandwidths and phase noise reduction of (integrated) VCO's.

The tuning system operates on a  $5\text{ V} \pm 20\%$  power supply with a power dissipation of 35mW. Due to the small active chip area ( $\sim 1\text{mm}^2$ ) and to the low power dissipation the tuning system can easily be combined with integrated VCO's, and the total system can be encapsulated in standard low cost packages. This enables mass production with low costs without sacrificing the product reliability and life-time.

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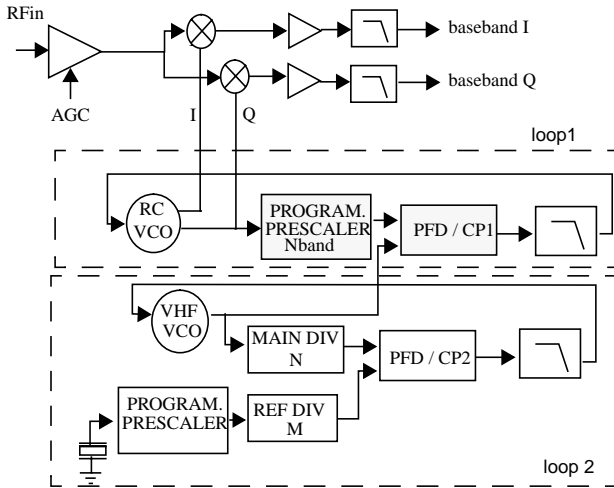
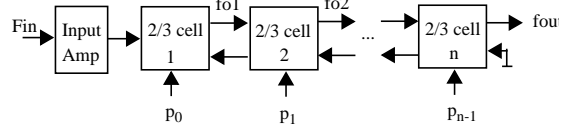


Fig.1 - Block diagram of sat. receiver and tuning system



Minimum division ratio =  $2^n$  for  $P = 0$

Maximum division ratio =  $2^{n+1} - 1$  for  $P = 2^n - 1$

Fig. 2 Architecture of modular programmable divider function

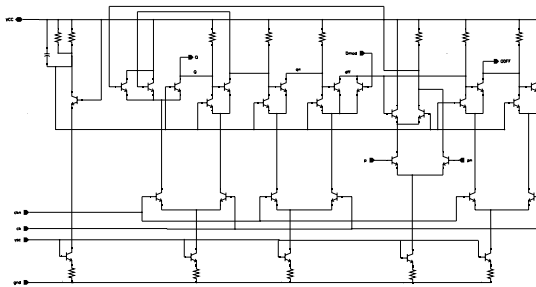


Fig. 3 - CRL circuit implementation of 2/3 divider cell

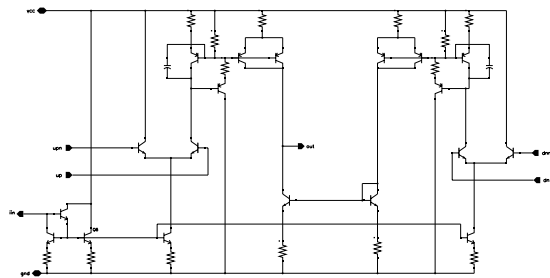


Fig.4 - Circuit implementation of wide band charge pump

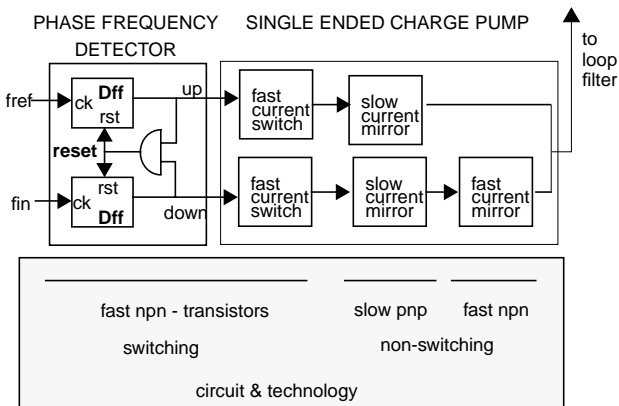


Fig. 5 - Mapping of PFD/SECP function into standard technology

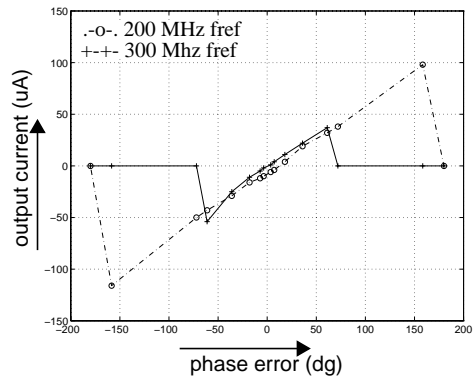


Fig.6 - Static transfer PFD/SECP

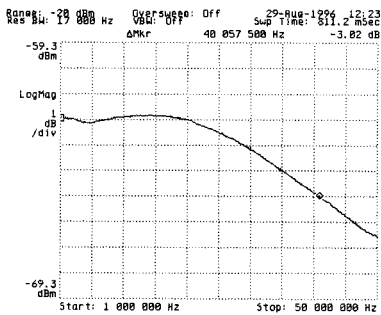


Fig.7 - Dynamic transfer of PFD/SECP at 300 MHz ref. frequency

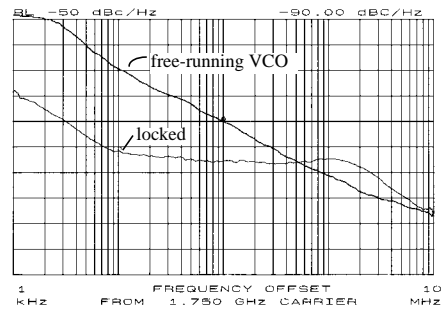


Fig. 8 - Phase noise reduction by use of wide band PLL