

A 3-V DELAY-MODULATED PLL SYNTHESIZER FOR ANALOG FM TRANSMITTERS

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Abstract

An analog FM modulator operating within the loop bandwidth of a frequency synthesizer is presented. Its operation is based on delay-modulating the reference frequency of the synthesizer PLL, thus causing phase modulation in the synthesized carrier. To convert delay-control to FM, modulating input is first integrated. The modulator circuit is implemented in a 1.2 μm BiCMOS process, has 2.8 V supply voltage and 1.5 mA supply current. In in-system tests, the modulator showed 7 kHz/V gain, 20 Hz(rms) residual FM and -31...-37 dB THD on audio band.

1. Introduction

In analog FM transmitters, modulation is often applied directly to the VCO of a frequency synthesizer PLL. This has a couple of disadvantages: firstly, modulation gain depends on the VCO gain. Secondly, the PLL loop tries to force the average output frequency equal to reference frequency input, thus causing a high-pass characteristics to the modulating signal. To allow audio band modulation, the loop bandwidth must be very narrow, which causes long settling times during channel changes. Here an experimental approach is presented where the modulation is applied already in the reference frequency of the synthesizer, thus allowing modulation inside the bandwidth of the PLL and consequently wider PLL bandwidth. The target application is analog mobile communication systems, e.g. IS-90 dual-mode standard [1].

2. Block diagram and requirements of the FM modulator

The proposed FM modulator is shown in Fig. 1a. f_r is the reference signal of the synthesizer, v_{mod} is an analog voltage containing audio and data, f_{out} is the transmitted signal (800 MHz) and LO is a local oscillator that mixes the output signal down to 90 MHz - this reduces the division ratio and makes the required delay range easier to implement. Modulation is caused by a voltage-to-delay converter V/T which creates signal-dependent delay or PM in the reference signal. Because input voltage v_{mod} is required to present FM instead of PM, it is integrated using an SC integrator before it is used to control the voltage-to-delay converter V/T.

Input signal v_{mod} contains both audio and data, and its bandwidth spans from 100 Hz to 10 kHz. Over this bandwidth the voltage mode integration used for FM-PM conversion alone causes 40 dB of dynamic range, requiring the total dynamic range to be too high e.g. for a digital delay line implementations used in [2], [3]. Thus, an analog implementation was considered, and here the noise level of the modulator is set by the required SNR for highest frequency components while the maximum delaying range is set by the largest cumulative phase amplitude of the lowest (sub-audio) frequency components. Also an offset cancellation loop is required to maintain the integrator in the middle of its linear range.

It is obvious that a hard limitation in phase modulation is disastrous for FM, as when the phase can no longer be modulated, also the capability to change the frequency is lost and signal drops back to center frequency. Thus, wide enough phase control range is a necessity. The actual linearity requirements are not simple to derive because here the distortion affects phase, not frequency, which makes the total distortion dependent on signal amplitude, modulating frequency and the amount of accumulated phase. Consequently, the delay range 50% wider than the maximum phase deviation and linearity better than 0.1% of full scale were set as design targets. In short, the design specifications were reference frequency f_r of 500 kHz, division ratio N of 180, max. delaying range from 0 to 300 ns and jitter level of 30 ps(rms).

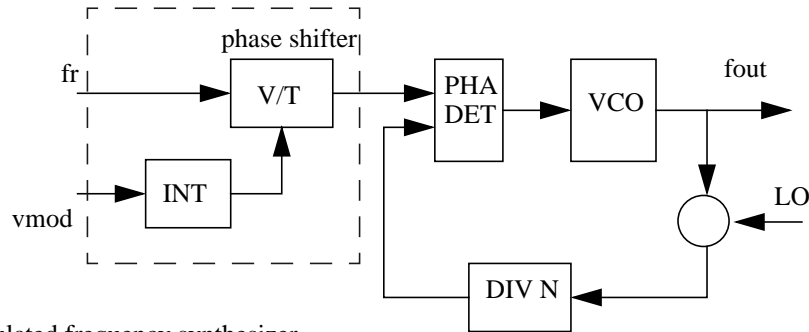


Fig. 1: FM-modulated frequency synthesizer

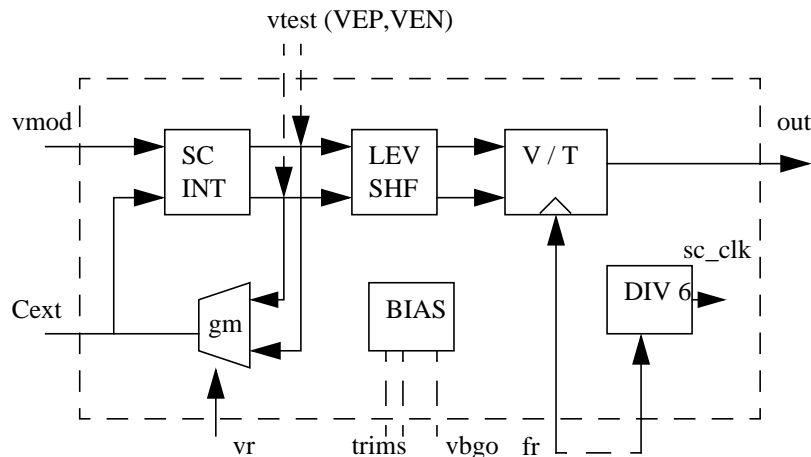


Fig. 2: Construction of the voltage-to-time FM-modulator.

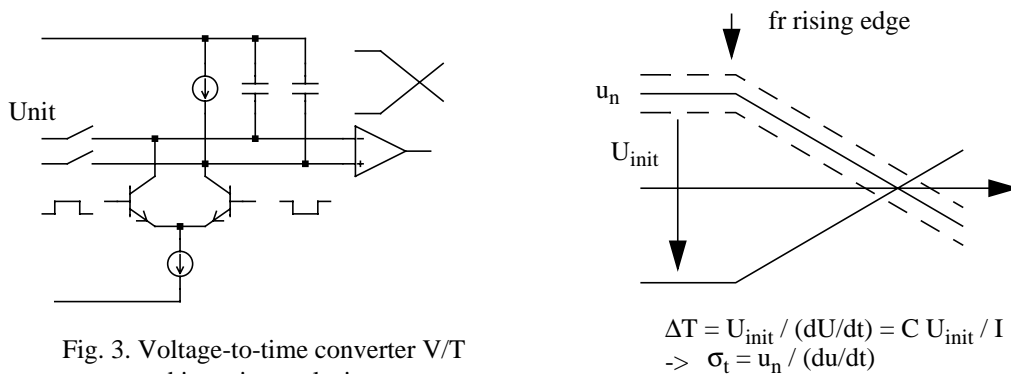


Fig. 3. Voltage-to-time converter V/T and its noise analysis

3. Circuit construction of the modulator

The circuit structure of the modulator is shown in Fig. 2. An SC integrator is used for FM-to-PM conversion and it has continuous time dc feedback to create ac coupling and offset cancellation. Then, signal is passed through a level shifter that converts the balanced output of the integrator to a unipolar control voltage for the voltage-to-time converter V/T.

The operation of the voltage-to-time converter V/T is shown in Fig. 3. A unipolar differential voltage U_{init} is charged in two capacitors forming a differential capacitor $C_{diff} = C/2$. When the delaying is triggered by the rising edge of reference frequency f_r , the capacitors are disconnected from the initiating voltage source and the capacitor with lower voltage gets charged towards supply voltage and the other one gets discharged towards ground. A comparator rises its output when these voltages cross each other. A differential configuration is used to get enough dynamic range in 2.8 V supply voltage environment.

Using this arrangement, a time delay t_D linearly proportional to U_{init} is generated, where

$$t_D = \frac{C_{diff} \cdot U_{init}}{I} \quad (1)$$

Here, the charge/discharge current I can be used to control the gain. The timing jitter of the modulator can be estimated by reducing all noise sources into the voltage U_{init} and dividing it by the slew rate $SR = I/C_{diff} = 1.2 \text{ V} / 300\text{ns}$. According to simulations, a jitter level of 70 ps(rms) was expected. Major contributors of noise were the bandgap reference used to create stable discharge current, input reduced noise of the comparator and noise in the level shifter.

4. Measured results

The modulator was fabricated in a 1.2 um BiCMOS process and tested first in time domain using accurate and proven time to digital converters [4]. In this environment, gain and linearity measurements were made. Next, the modulator was connected as a part of a frequency synthesizer and the performance of the modulated signal was compared to specifications using modulation and audio analysers.

During the measurement of the voltage-to-time converter, the on-chip SC integrator was bypassed and the control voltage was brought to input v_{test} . Conversion gain, delay range and jitter level were measured using a differential input voltage. Linearity was measured by driving the circuit with 1 kHz triangle wave and collecting the histogram of the generated delays. From that, maximum non-linearities were calculated, as shown in Table 1.

Table 1: Performance of the voltage-to-time converter

	Value
Voltage-to-delay gain	195 ns / V
Delay range	30 - 310 ns
Delay jitter	50 .. 80 ps(rms)
Peak non-linearity	
+/- 40 ns modulation	+/- 0.1 % of full scale
+/- 80 ns modulation	+/- 0.3 % of full scale
Dc current consumption	1.5 mA from 2.8 V

The in-system test setup consisted of an integrated circuit containing both the modulator and the synthesizer PLL. The generated 90 MHz carrier was demodulated and its purity was measured using an audio analyser. During these measurements, it was found that due to extremely high impedance levels the on-chip ac-coupling was picking up noise and causing a lot of fluctuation in the dc levels. Thus, in most of the measurements the ac-coupling was not used. The on-chip integrator was still used to perform the FM-to-PM conversion.

The bandwidth of the synthesizer PLL was ca. 7 kHz to limit adjacent channel noise, so it passed the audio band but had some attenuation of the harmonics. During the measurements, both the wideband and audio band (using psfometric filtering) THD was measured. The measured results are collected in Table 2.

Table 2: In-system performance

	Value
Modulation gain	7.1 kHz / V
THD with 500 Hz, 0.5Vp-p modulation	-26 dB total -31 dB on audio band
THD with 1 kHz, 0.5Vp-p modulation	-24 dB total -33 dB on audio band
THD with 2 kHz, 0.5Vp-p modulation	-27 dB total -37 dB on audio band
Residual FM without modulation	150 Hz(rms) total 20 Hz (rms) on audio band

5 Summary

The rf performance of the first prototype is encouraging, but some improvements are still needed. Main problems are the implementation of the very low frequency (<10 Hz) offset cancellation loop which requires complete re-thinking. The non-linearity of the circuit is large but not intolerable. It is dominated by the non-linearity of the level-shifting circuit which consists simply of a degenerated BJT differential pair. This error can be reduced by passing more current through the BJTs and reducing the gain of the level shifter.

Noise behaviour was already good enough, and it too can be improved at the expense of current consumption by reducing the impedance levels in the biasing circuitry and in the level shifter.

References

- [1] TIA/EIA Interim Standard IS-90: Recommended Minimum Standard for 800 MHz Dual-Mode Narrowband Analog Cellular Subscriber Units.
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