

**Read front end of a new AC coupled Preamplifier
for 300 Mb/s Hard Disk Drives
using single stripe Magneto Resistive heads**

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Abstract

This paper describes the read front end structure of a new current bias voltage sense low noise preamplifier designed for Hard Disk Drive applications working at 300 Mbit/s and using single stripe M.R. heads.

The use of AC coupling capacitors together with a gyrator enables to separate the M.R. head biasing circuit from the fully symmetrical amplifier. Common mode signal is then treated as interference and rejected by the amplifier even at high frequencies.

CMRR and supply rejections higher than 45 dB up to 200 MHz has been demonstrated.

1 Introduction

The need to bias a single stripe magneto resistive head to extract the differential signal, make its two terminals assymetrical to the inputs of the preamplifier. When this latter has to deal with both M.R. biasing and M.R. signal amplification in a single structure, it is very difficult to guarantee a high level of common mode rejection especially at high frequencies. That is why such preamplifiers are often called pseudo differential [1]. This lack of rejection at high frequencies degrades for instance the bit error rate.

In the described structure, the magneto resistive head biasing circuit is separated from the amplification circuit by integrated AC coupling capacitors. The biasing circuit symmetry is ensured by passive components.

2 Read front end structure

The schematic diagram of the read front-end is presented in Figure 1. It is composed of a read head biasing circuit and a differential pair.

The magneto resistive head (R_{mr}) is biased with a constant current I_{mr}. A feedback loop enables to control the common mode voltage of the R_{mr} so that it is close to the ground. The impedances at nodes A and B are matched for symmetry.

The differential signal coming out of the magneto resistive head is amplified by a differential pair. This differential pair is perfectly balanced, in spite of opposite voltages at A and B nodes, by the use of AC coupling capacitors. The base currents of transistors T1 and T2 is I_b .

3 Looking for optimization

For low noise constraints, it is necessary to use large transistors in the differential pair with enough tail current. But increasing the tail current, increases the -3dB low corner frequency of the amplifier for a constant capacitor value.

For instance, with $I = 10$ mA and $\text{Beta} = 150$, 2 times 210 pF are required to have 1 MHz of low corner frequency which is huge for integrated circuits. Other implementations have to be considered.

Figure 2 shows how with a quarter of capacitor it is possible to keep the same front end amplifier as in Figure 1 :

Figure 2a shows a differential pair with two AC coupling capacitors connected to the bases.

Figure 2b gives the small signal equivalent circuit looking from A and B.

Figure 2c is an equivalent scheme to figure 2b.

Figure 2d shows a circuit whose small signal equivalent circuit is Figure 2c.

R can be considered as the input impedance of the differential stage.

So going from the circuit of Figure 2a to the circuit of Figure 2d enables to save three quarters of the AC coupling capacitor value, and without reducing the symmetry.

In this new arrangement one base of each differential pair is directly connected to A or B. So, it is needed to have a circuit between the bases of each pair so that they still be balanced. This circuit should behave as an inductor which is made by mean of a gyrator.

4 Gyrator synthesis

The gyrator implementation is described in Figure 3.

It is composed of three differential pairs and of one capacitor. The input of the second differential pair (T3 and T4 transistors) is connected at the output of the gain amplification first stage (first differential pair - T1 and T2 transistors). The signal is then integrated with C_g capacitor, and amplified again with the third differential pair (T5 and T6 transistors). R_b is needed for circuit biasing.

By the mean of this feedback loop, the voltage at node B (fixed by the R_{mr} biasing circuit) is copied to the base of T1 transistor as soon as all the differential pairs are balanced.

At high frequencies, the circuitry is equivalent to an inductor whose value is equal to :

$$L = 2 \times (2Cg) \times \left(\frac{\left(R3 + \frac{1}{g3} \right) \times \left(R5 + \frac{1}{g5} \right)}{g1 \times Rl} \right)$$

with g_1, g_3, g_5 the transconductance of T1, T3, T5 transistors.

5 Complete front-end structure

The final read front end structure of Figure 4 has the same fonctionnality as in Figure 1 but with a quarter of AC coupling capacitor. This is very important because it makes possible the integration of AC coupling capacitors into an amplification gain stage per head to achieve the specified gain, which minimize the parasitic resistors due to the interconnections between components. The outputs of the reader front-end is then multiplexed.

6 Measured amplifier characteristics

Figure 5 shows the frequency responses of the common mode rejection ratio and of the gain. 45dB gain over the 300kHz to 250 MHz frequency band is obtained with a CMRR higher than 47dB up to 200 MHz. The complete read amplifier exhibits an input referred noise voltage of $0.71\text{nV}/\sqrt{\text{Hz}}$ at 20 MHz with a R_{mr} of 41Ω . The preamplifier also includes a writer, with programmable compensation capacitors, which demonstrates rise and fall times (20%-80%) as low as 1ns for a load inductance of 110nH and a write current of 46mA.

Typical measurements on the product are summarized below :

Reader :

For operating conditions $V_{CC} = 5\text{V}$, $V_{EE} = -4.7\text{V}$, $R_{mr} = 41\Omega$, $I_{mr} = 10\text{mA}$,

Read amplifier bandwidth : 300kHz - 250MHz

Read amplifier gain : 45dB - 48dB (programmable)

Input referred noise voltage : $0.71\text{ nV}/\sqrt{\text{Hz}}$ (both voltage and current noise)

Common mode rejection ratio : 58dB at 20MHz, 54dB at 100MHz
> 45 dB in all the bandwidth

Power supply rejection ratio on V_{CC} : 50dB at 20MHz

Power supply rejection ratio on V_{EE} : 45dB at 20MHz

Writer :

For operating conditions $V_{CC} = 5\text{V}$, $V_{EE} = -4.7\text{V}$, $L_h = 110\text{nH}$, $I_{wr} = 46\text{mA}$,

Rise and fall times : 1.4 ns (10% - 90%)

1 ns (20% - 80%)

7 Conclusion

This novel reader architecture has demonstrated a very high level of spurious noise rejections together with a wide frequency bandwidth. The ability to use integrated AC coupling capacitor thanks to the gyrator circuit enables to reduce the parasitic resistors which results in a low input referred noise level. Combined with a fast writer, this MR preamplifier is capable of reading and writing at data rate up to 300 Mb/s (with 8/9 or 16/17 coding).

8 Acknowledgement

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9 References

[1] J. Shier and D. Peterson, "Read/write preamplifiers for magnetoresistive heads", Data storage, pp.63-68, September 1994.

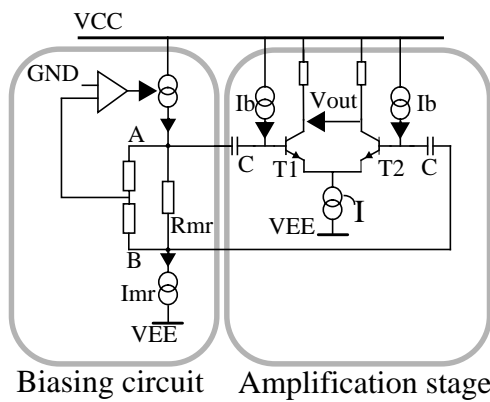


Figure 1 : Circuit diagram of the read front-end

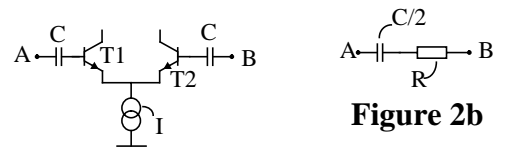


Figure 2a

Figure 2b

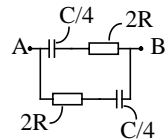


Figure 2c

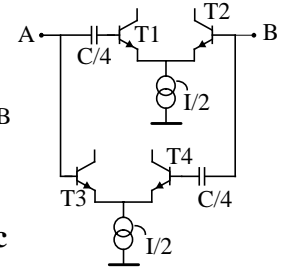


Figure 2d

Figure 2 : Equivalent impedances

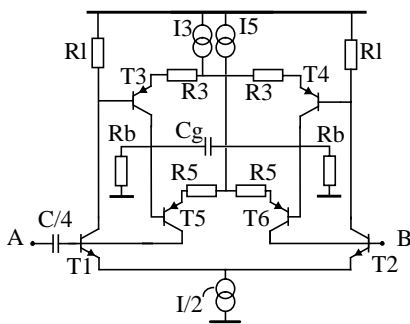


Figure 3 : Gyration implementation

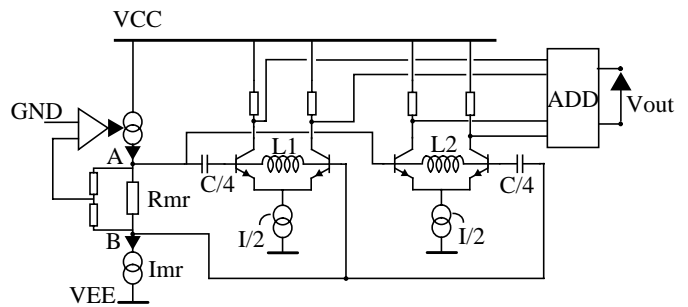


Figure 4 : Equivalent circuit of the reader front-end (principle)

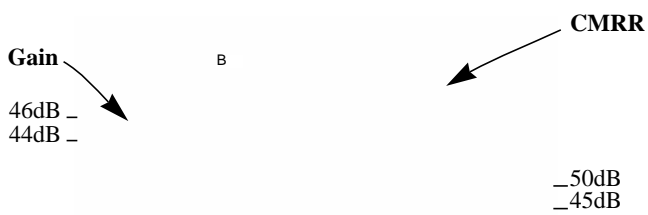


Figure 5 : Gain and CMRR frequency responses

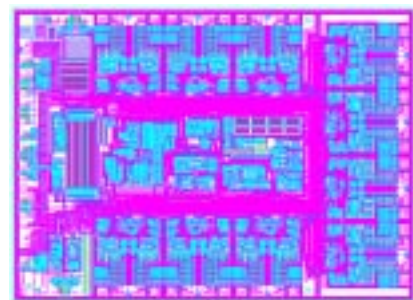


Figure 6 : Chip layout