

# High Speed Arithmetic Design Using CPL and DPL Logic

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## Abstract

PRML disk drive read channels have been developed delivering bit rates of 140-250Mbits/s in 0.6-0.35 $\mu$ m technologies. These require high speed low power digital arithmetic circuitry. Investigations have been carried out to find an optimum device level design style, which has the characteristics of high speed with minimum power. The CPL (Complementary Pass Logic) design style was used successfully in the read channel developments, but it is shown that DPL (Double Pass Logic) may be faster and, more significantly, is easier to map and optimise at device level than CPL. This is significant in improving optimisation and reducing design time.

## 1 Introduction

Current disk drive read channels are most commonly designed using a technique called Partial Response, Maximum Likelihood (PRML) [1]. This accommodates the partial overlap of the response from adjacent bits by synchronously sampling the waveform from the magnetic read head at the bit rate with an A-to-D converter and then applying one of a number of decoding algorithms to resolve the 1 and 0 bit values. This necessitates some digital signal processing of data with a word length of around 5-8 bits at the encoded read bit rate, currently in the range 150-300MHz. Clock speed is a primary design requirement with power consumption thereafter the most important performance metric. This paper reports on work on detailed circuit design techniques carried out to support a completed PRML read channel delivering 140Mbit/s decoded bit rate in a 0.6 $\mu$ m 5volt CMOS technology and a further 250Mbit/s development in 0.35 $\mu$ m 3.3volt technology.

One performance critical digital section in these PRML read channels is the adaptive equaliser which compensates the variation of pulse shape with position of the head on the radius of the disk. In this work, this is a 5-tap FIR with 6 bit data and 5 bit coefficients. In the 140Mb/s chan-

nel the filter is symmetric with the inner pair of taps adapting (Fig. 1); in the 250mb/s channel the filter is asymmetric with 4 taps adapting. System considerations also constrain the latency through the filter preventing free pipelining.

These requirements place great demands on the basic circuit level building blocks, of which the full adder is the key, with the XOR gate a key primitive gate used intensively in most arithmetic operations. Now it is well known that the most productive and thus most widely used design methodology is logic synthesis to a standard cell library. Some critical-path sample functionality was thus coded at Register Transfer Level (RTL) in Verilog HDL and synthesis attempted using a commercial cell library of an orthodox CMOS design style and the industry-leading logic synthesis tool. This failed to meet the required timing constraints by about 25%. The circuit was then designed by schematic entry at device level using Complementary Pass Logic (CPL) and the physical layout performed by hand. This resulted in meeting the target clock timing.

Due to the complexity of the FIR filter, most of the investigations to find the optimum design style were performed on the simpler representative element of a maximum speed adder. The balance of this paper reports those investigations.

**2 Complementary Pass Logic (CPL)**

It was found that an adder of the design style shown in Fig. 2 performed well for both speed and power relative to orthodox CMOS design styles. Cascading NMOS pass networks results in inherently low power, as the product of total gate capacitance and voltage swing is lower than the logically equivalent compound or cascaded CMOS gate(s). However, the positive-feedback signal regenerators must be judiciously placed and the pass devices correctly sized to meet the required propagation delay, and the circuit is thus time-consuming to optimise by design judgement and trial simulations. Thus although this design style met the immediate design objectives, the detailed device level implementation may not be fully optimised. Further academic research was thus carried out.

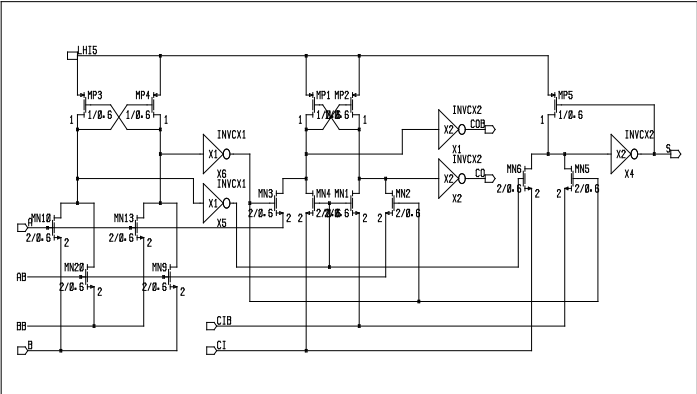
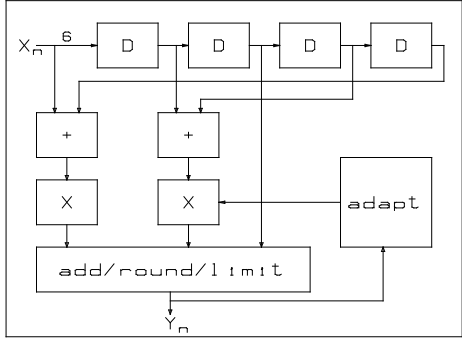


Figure 1. Adaptive Equaliser..... Figure 2. CPL adder bit

**3 Double Pass-Transistor Logic (DPL)**

DPL was introduced in [2] and like CPL [3,4] it uses complementary signals to drive the logic cells. As with CPL only a limited number of simple cells are needed to describe general logic functions (fig 3). DPL's main difference to CPL, is that it gives full swing signals for every logic state (either an n-mos tree for a logic zero or a p-mos tree for a logic 1 is active). This is very important when looking into reduced supply voltage designs. CPL's Vt voltage drop, because

of pure n-mos logic, is one of its biggest disadvantages and leads to performance degradation and severe design limitations. Buffers have to be inserted to drive the gates of logic cells in order to avoid even further speed degradation. Since DPL has full voltage swing output signals, buffers can be inserted wherever they offer better performance. The added transistor count is a disadvantage over CPL, but the overall advantages in speed can outweigh the increase in power dissipation and area. In fact power dissipation for DPL is not much worse than CPL, due to the sharper signal rise and fall and better synchronisation of the complementary signals.

Figure 3: DPL logic cells

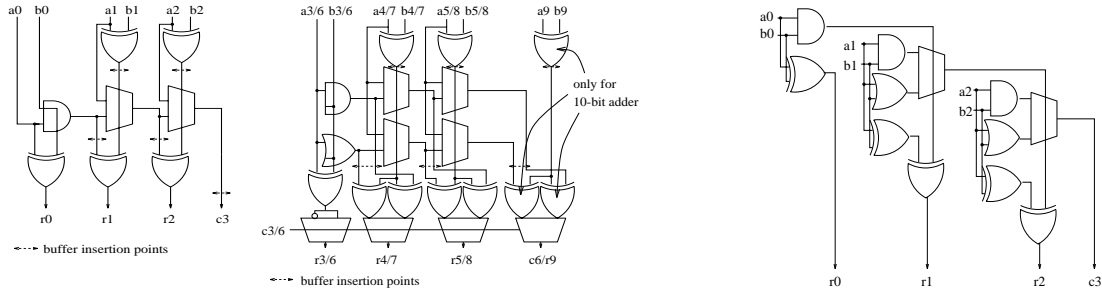
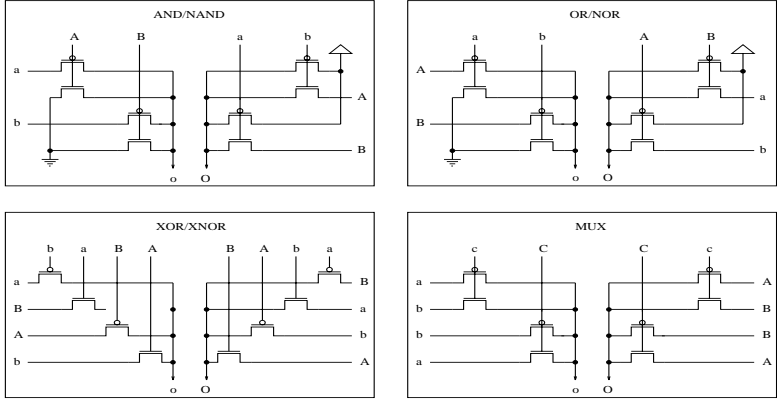


Figure 4: Carry Look-Ahead Adder Design...Figure 5: Conditional Carry Select Adder Scheme

**4 Design Improvements and Optimisation**

The basic design for the DPL implementation of the adder circuit is the same as for CPL. The CPL carry-look-ahead adder design already takes advantage of the complementary pass logic, using MUX carry-chains and XOR gates for carry generate and summation (fig 4). Each of these stages only need a single transistor in the input-output path to switch. One design improvement which works better for DPL is to use a scheme called conditional carry selection [2] (fig 5). This scheme reduces the maximum number of pass-transistor stages in series and therefore helps to speed up the signal. The cost for this scheme is a further AND and OR cell per adder stage.

Besides logic optimisation, transistor level optimisation using a simplified pass logic timing model can be carried out. Our model helps to find optimal transistor sizes for every logic element, buffer insertion points and handling of the critical path. The model consists of a design rule base and of a mathematical model.

**5 Layout Automation**

The first step towards layout automation was to create cell libraries for CPL and DPL design style, which can be used by place & route tools (in this study GDT's AutoCells from Mentor

Graphics). The cell design is very similar to normal standard cell designs. We used a two metal-layer process; the library cells were designed to use only metal1 thus freeing metal2 for over-cell routing.

## Results

The results comparing CPL and DPL for different 6- and 10-bit adders using automatic place & route can be seen in the following table 1. The data was generated using Lsim (Mentor Graphics) and should be within 10% of a SPICE simulation.

Table 1:Relative Number of Cells, Area and Speed for different adder designs

add6.cpl.....	65 / 0.0339 / 4.26ns
add6.dpl.....	60 / 0.0416 / 3.72ns
add6ccs.dpl.....	67 / 0.0462 / 3.68ns
add10.cpl.....	111 / 0.0696 / 6.01ns
add10.dpl.....	102 / 0.0718 / 5.69ns
add10ccs.dpl.....	112 / 0.0814 / 5.48ns

All the designs in this table include input and output buffers (which are of the same size) and buffers for speed optimisation (which can vary depending on the load they have to drive). The ccs designs use the above mentioned carry select scheme.

## 6 Conclusion

It has been found that pass transistor logic has advantages over orthodox CMOS standard cell design in the implementation of performance-critical arithmetic processing circuitry, used here in PRML disk drive read channels at 140-250Mbit/s bit rates. Comparative studies have further shown that DPL offers advantages over CPL in performance. As significantly, while CPL is difficult to map from logic to device level and then to optimise, DPL inherently lends itself better to rule-based mapping, modelling and optimisation, to speed the design process.

## References

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