

An ISM band Transceiver Chip for Digital Spread Spectrum Communication.

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Abstract

This paper discusses a transceiver chip operating in the Industrial, Scientific and Medical (ISM) band, 902MHz to 928MHz, developed for use in digital cordless telephones for the United States. The design has been fabricated on GPS' HGC process. Design objectives included low noise figure and distortion, low system cost and low current consumption from a 2.7V supply. Emphasised in this paper are the circuits which enabled the device to meet the required system specifications.

Introduction

The device consists of a pair of image-reject/single sideband (SSB) mixers. The receive mixers downconvert to an IF of 70MHz. The transmit mixers directly modulate the baseband IQ signal into the ISM band. An image-reject receive architecture eliminates the requirement for an image filter at RF^[1]. High accuracy quadrature generation coupled with an SSB mixer and LO spectral shaping means output spurs are reduced such that a transmit output SAW filter is not required. A block diagram of the device is shown in Figure 1. A comparison of specified, simulated and measured results is shown in Table 1.

UHF Oscillator and Quadrature Generation.

A balanced common collector colpits oscillator is used with an external printed stripline resonator. This drives a divide-by-two circuit consisting of two D-Types. The outputs from these are in approximate phase quadrature (prior to servo correction) and are used as I and Q local oscillator signals for both transmit and receive mixers. The outputs are also fed to a phase detector which is a doubly balanced multiplier. Any deviation from quadrature on the inputs causes a finite output current which is integrated to provide an error voltage. The phase detector output impedance is boosted to very high levels (typically in excess of 30K) by connecting a negative resistance

generator across the output. The error voltage is used to modify the mark-space ratio of the incoming VCO signal to compensate for errors in the VCO or the dividers (Figure 2). The accuracy of the resulting quadrature for the LO is therefore dependent only on the accuracy of the phase detector itself. A feature of this type of quadrature generation is that it requires a twice frequency oscillator. This is attractive in direct modulation systems as it helps to reduce VCO susceptibility to pulling by the transmit output signal.

Transmit Section

The I and Q LO signals have some spectral shaping applied to them prior to the mixers to reduce levels of higher order mixing products whilst still driving the mixer optimally. The current outputs from the long tail pair LO buffer amplifier approximate to a square wave which has a $1/x$ characteristic with frequency. The collector has an RC load which has been designed to have a $1/x^2$ characteristic at or above 1GHz. Harmonics at the output of this stage therefore follow a $1/x^2$ characteristic which means that the waveform is basically triangular in shape. The mixer LO ports have a transconductance which follows a tanh characteristic. By ensuring that the levels out of the LO buffer are triangular and of well controlled amplitude, it is possible to fully switch the LO ports to the mixer whilst ensuring that the higher order mixing products are substantially reduced. This feature removes the need for a high Q bandpass filter at the IQ mixer outputs.

The output of the mixer is fed into a preamplifier, then finally into the power amplifier driver. The balance of this amplifier is critical because any second harmonic of the TX output will be centered on the Tx VCO signal, and can cause modulation on the Tx LO and hence spreading in the Tx output spectrum. The output is open collector so the power derived is set by external resistors and matching components. A differential output is used to minimise noise coupling and to maintain balance thereby reducing the amount of signal energy flowing in the supplies.

Receive Section

The LNA (figure 3) is a cascoded common emitter configuration with inductive degeneration and tuned load. The input transistor is biased well below peak ft. With input frequencies above a few hundred MHz, the device is operating well above the beta-pole so that inductance in the emitter of the input transistor appears resistive looking into the base. A 1.5 nH inductor was used in the emitter of the input device, which provides about 10 Ohms of degeneration at 1 GHz and translates to a real input impedance of around 50 Ohms

The collector of the input device is cascoded to reduce miller feedback and to increase its output impedance. The LNA output is loaded with a LC tuned network. This increases the maximum achievable signal swing for the available headroom and has the added advantage of providing some rejection of image noise and noise at the third harmonic of the VCO which might otherwise be folded in-band, degrading the system noise figure. The input impedance of the mixer is seen in parallel with this load, and since this is fairly low the load has a Q of around 2 or 3 which gives it good tolerance to component variation.

An important consideration in the design of this type of LNA is the path that the RF signal current takes to the supplies. If the LNA supplies were only decoupled off-chip, all of the amplified RF signal current would be passing through a ground bondwire. This could add another 2nH of inductance to the emitter of the input device which would reduce its gain and affect its input impedance. The bondwire length would be expected to vary from device to device, depending on the positioning of the die in the package well, resulting in a highly variable error. An on chip

decoupling network was used to make sure that most of the amplified RF signal circulated on-chip to reduce the effects of package inductance. This decoupling was made broadband to de-Q any potential resonant effects with package and board parasitics.

The mixer gm stage (figure 2) is a common-base common-emitter configuration which provides a differential output to the balanced mixer and is also efficient in component usage, providing good noise and IIP3 performance without the overhead of large spiral inductors. The switching components are in a standard gilbert-cell configuration and have been optimised for noise using HP-Eesof.

The IF phase-shifters are differential dual first order all pass filters which provide a relatively broadband 90 degree phase shift between the I and Q outputs from the individual mixers. The capacitive and resistive elements provide a load impedance $Z(s)$ to the emitter followers (figure 4). An additional impedance of approximately $-Z(s)$ is added in parallel so that the emitter followers are loaded by a very high impedance across the whole frequency range of interest, thus high linearity can be achieved with a low bias current.

Conclusions

A transceiver chip suitable for use in spread-spectrum ISM band digital communication has been integrated in silicon using 6mm^2 of silicon area on GPS' HG technology. The chip meets all specifications and consumes only 90mW of power in receive mode from a 2.7V supply.

References

- 1) Louis Pandula, "Image Reject and Image Cancelling mixers", RF Design, April 1995
- 2) J. Fenk et al., "An RF Front-End for Digital Mobile Radio", IEEE 1990 Bipolar Circuits and Technology meeting 11.2.

	Specification	Simulated	Measured	Units
Receiver, $V_{cc}=2.7V$, $T=27C$				
Noise Figure	4	3.6	4	dB
IIP3	-13.5	-11.5	-11.5	dBm
Power Gain	12	18.5	17	dB
P1dB (input referred)	-27	OK	-24	dBm
Image Rejection	20	40	42	dB
IccMax ($V_{cc}=3.3V$, $T=80C$)	40	37.5	38	mA
IccNom($V_{cc}=2.7V$, $T=25C$)	NS	32	32.5	mA
Modulator & PA, $V_{cc}=2.7V$, $T=27C$				
LO rejection	20	NS	25	dBc
Image rejection	30	30	35	dB
PA output power	3	4.5	4	dBm
IccMax ($V_{cc}=3.3V$, $T=80C$)	60	60	55	mA

Table 1 - Comparison of Key Specified, Simulated and Measured Parameters.

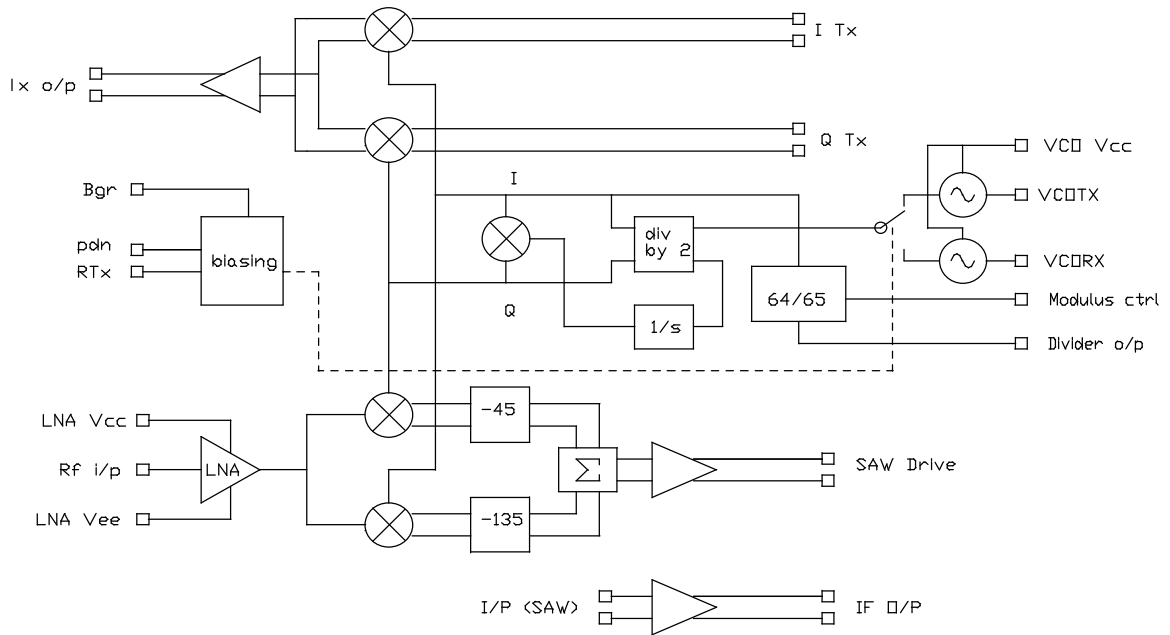


Figure 1 - Block Diagram of Transceiver Chip

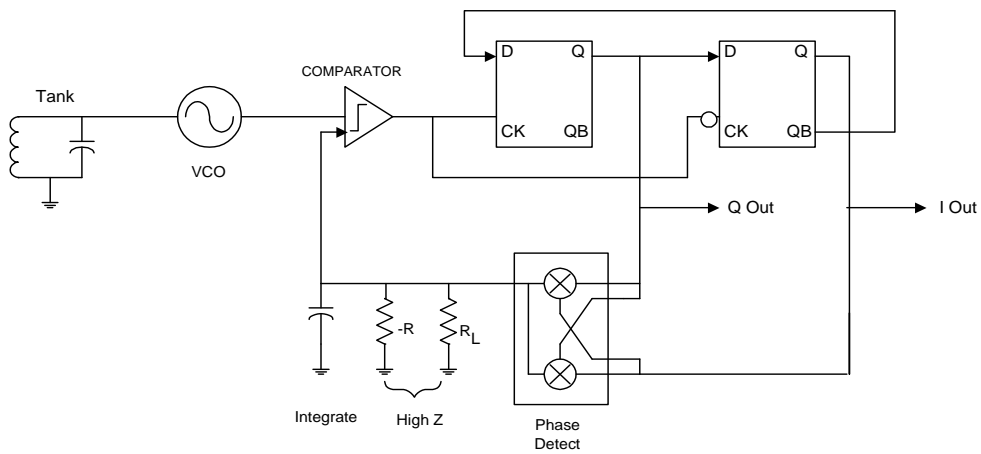


Figure 2 - Quadrature Generation

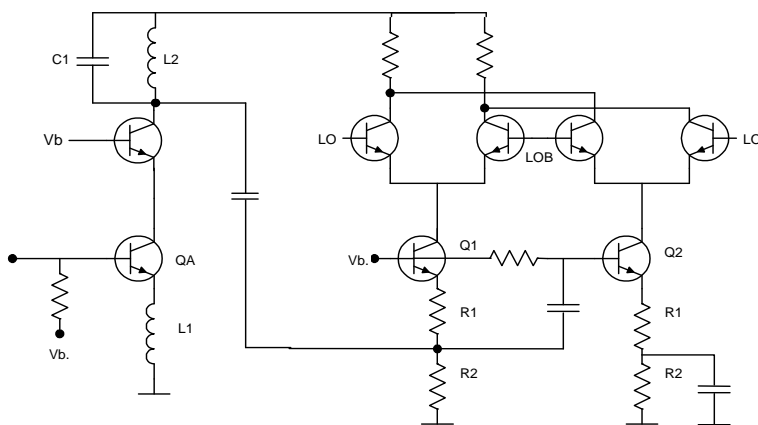


Figure 3 - LNA/Mixer Configuration

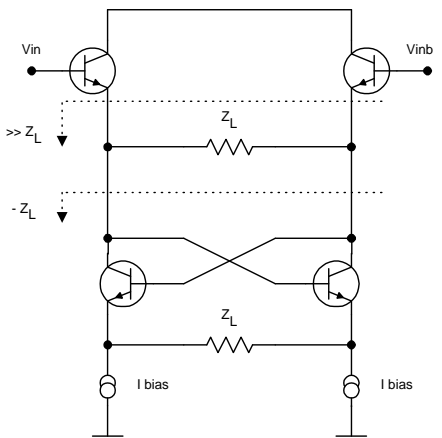


Figure 4 - Unity Gain Buffer