200 Megasample per second 6 bit A/D converter

Oskar Leuthold
GEC Plessey Semiconductors
Scotts Valley, USA

Abstract
A 200 Megasample per second flash A/D converter was built on a standard digital 5V 0.6u CMOS process in an area of 1.5 square millimeters.
The effects of metastability and bubbles were addressed to achieve a low error rate of 1e-9.

1. Introduction

A flash A/D converter consists of a bank of comparators and a decoder, as shown in figure 1. The code coming out of the comparators is called thermometer code, with the lower ranks producing all ones, and the higher ranks all zeroes. The location of the code transition is a digital representation of the input signal. The decoder converts the thermometer code to binary, suitable for arithmetic operations.
In the target application, a PRML chip for disk drive applications, the converter input is the last stage of a multiple pole continuous time filter with a bandwidth of 50MHz. This eliminates the need for a separate sample and hold circuit.

2. Overview of one slice

Figure 2 shows a simplified schematic of one slice of the converter. The input stage consists of two differential pairs, sending a differential current to a folded cascode. The outputs of the cascode transistors are connected to a first latch (Nlatch). Then two parallel latch structures process alternating samples. A multiplexer directs the samples to one of two pairs of storage capacitors. From there the samples are fed to a second latch (Platch), and a third latch

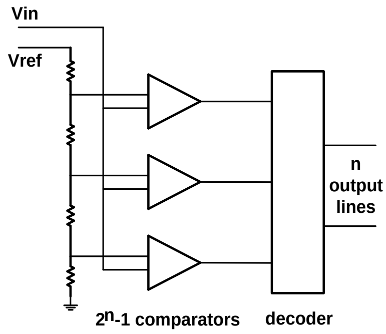


Figure 1: principle of flash A/D converter

(rslatch).Then the alternating samples are combined at the complementary output of the comparator. The decoder part of one slice contains the bubble gate, which compares samples from adjacent slices and if appropriate, produces a ROM address.

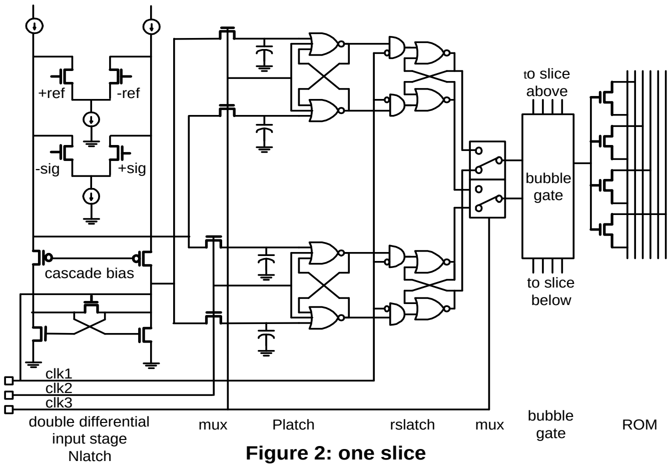


Figure 2: one slice

3. The comparator front end

Figure 3 shows the input stage in operating mode. The two differential pairs convert the signal and the reference voltage to current. When the input voltage differences are equal, then the sum of output current from the two stages is the same on both sides. A third differential pair produces current to compensate offsets. These currents are summed at the input of a folded cascode. The outputs of the cascode are tied to a group of NMOS devices, which can be configured differently for the various modes of operation: latch reset and evaluation, or autozero. In normal operating mode, the NMOS devices are cross coupled, and a switch defines the two phases, reset and evaluation.

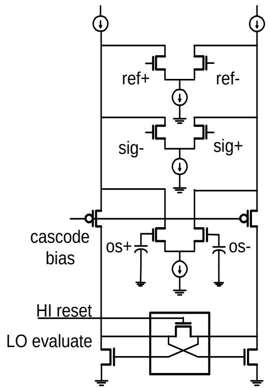


Figure 3: input stage operating mode

In order to achieve high speed, the transistors in the signal flow path need to be small, and their offset is likely too high for an LSB in the range of a few millivolts. Therefore the need for offset compensation on each comparator. The converter is switched to autozero mode between conversion bursts.

Figure 4 shows the autozero mode. The differential input stage, which normally accepts the signal, is tied to the reference. The sum of currents from the two differential stages should be equal on both sides. The gates of the NMOS devices are tied to the output of a common mode feedback circuit. The offset storage capacitors are charged by the latch output such that the offset pair injects the appropriate amount of offset current into the cascode summing nodes.

One problem with latches is kickback. For moderate input signals,the latch nodes go to the rail, in our case upsetting the summing node,and possibly disturbing the signal and reference input. To avoid this, clamps are connected across the Nlatch.

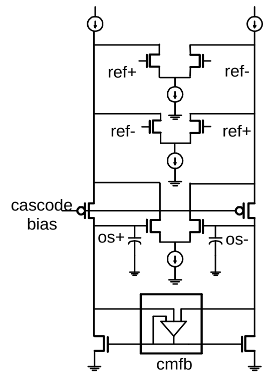
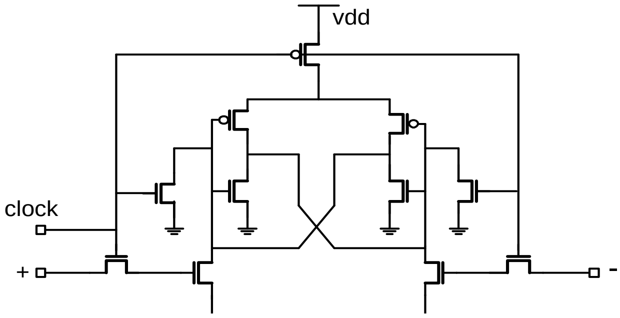


Figure 4: input stage autozero mode

4. The comparator back end

As shown in figure 2, two identical latch structures, each consisting of a Platch and an rsLatch, are working on alternating samples from the input stage. This design with the alternating Platches does not kick back to the Nlatch, allows for long evaluation time, and works with a simple clocking scheme.

Figure 5 shows the detailed Platch schematic with the multiplexing sample and hold input. For one complete cycle of the Nlatch, starting from the beginning of the reset phase to the end of the evaluation phase, the clock of one of the two Platches is high. The transfer switches are conducting, while the latch is reset, with both nodes held at ground. At the end of the evaluation phase, the final voltage of the Nlatch is stored on the gate capacitance of the coupling transistors. Then the clock goe low, the transfer transistors are switched off, and the latch is turned on. The PMOS devices charge the two nodes up rapidly; at some point the NMOS devices are also turning on, increasing the transconductance further, while the currents from the coupling transistors imbalance the latch.
Referring back to the simplified schematic of figure1, the Platch is followed by the rsLatch, which reads the data during the second half of the evaluation phase of the Platch. Finally a multiplexer sends one of the two complementary rsLatch signals to the comparator output.



5. Comparator gain and metastability

In order to achieve low error rate, the effects of metastability need to be addressed. For any comparator, there is a small range of input voltage, for which the output does not go all the way to the rail, it is metastable. Different gates, with different thresholds, interprete a metastable input level differently. Therefore, wherever the logic signal branches, the metastable states must have been resolved to a level which meets the error rate requirement of the application. In the present design, the target error rate is 1e-9. With an LSB size of 5mV, and a logic swing of 5V, a gain of 1e12 is required before the decoder. The voltages in latch structures grow and decay exponentially with time [1]. This property allows for high gain with simple means. Figure 6 shows simulation results for input stage and Nlatch with 1 uV input voltage. The initial voltage on the latch is 0.3 uV. After some time into the evaluation phase, the voltage builds up exponentially, at a rate of 0.8 decades per nanosecond. With an evaluation time of 2.5ns, 2 decades of gain result. Figure 7 shows the transient response of the Platch. The voltage grows exponentially, at 2.9 decades/ns. With 4ns evaluation time, 11.6 decades of gain result. Taking into account the gain of 0.3 from differential input to Nlatch, then the total gain to the Platch output is

0.3 * 10**2 * 10**11.6 = 1.2e13,

which compares favorably with the gain requirement of 1e12 mentioned before.

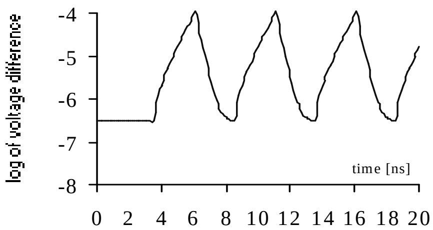


Figure 6: Nlatch Response

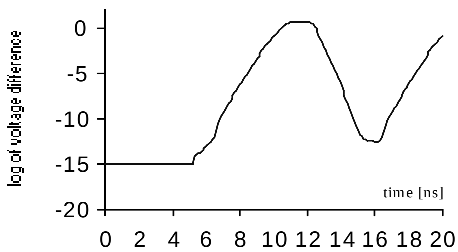


Figure 7: Platch Response

6. Decoder

The decoding section of a slice consists of a bubble suppression gate addressing one ROM byte location. From all the slices, exactly one address line needs to be activated. Under conditions like high noise level on the chip or high slew rate of the input signal, a comparator may make a wrong decision. The comparator bank output code resembles a bubble in the fluid of the thermometer. For certain decoder implementations, this condition activates several address lines in the ROM, which in turn produces then a substantial error in the binary output code.

In the present design, the decoder suppresses any single bit bubble, like 00100 or 11011 [1]. Each bubble gate looks at four successive comparator outputs and implements

Y=A AND (B EXOR C) AND NOT D,

with B being the output of the current slice, C one above, D two above, and A one below.

7. A/D top level

The VCO clock at 200MHz is split onto two clock lines, clkA and clkB in figure 8, which go through all comparator cells. A simple logic circuit then produces the required clock signals locally: a full frequency clock for Nlatch, rsLatch, ROM and output register, and a complementary clock at half frequency for the multiplexers and the Platches.

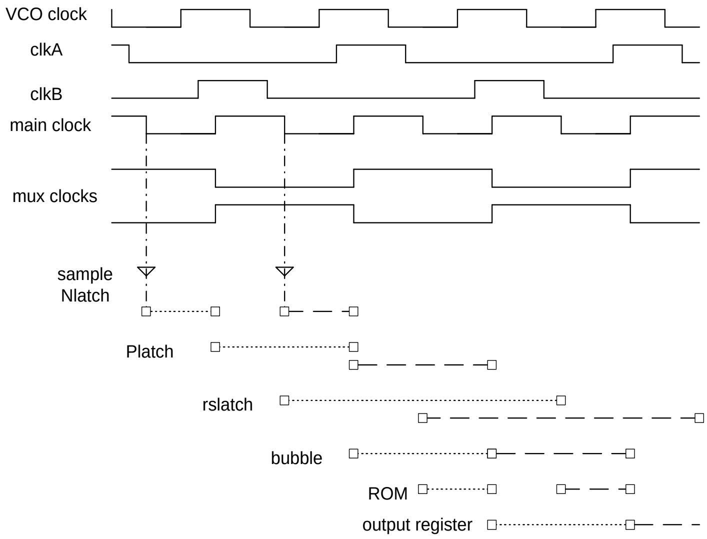


Figure 8: timing and latency

Figure 8 shows also how two subsequent samples are processed in the slice. Latency is 2.5 clock cycles. The size of the converter is 1.5 square millimeters. Power consumption is expected at 150mW. The integrated circuit containing this converter is in wafer processing at the time of this writing. Results from silicon will be presented at the conference.

Acknowledgement: The author would like to thank Florin Oprescu for the stimulating discussions, and Colleen Seiden for the extraordinary layout contribution.

References:

[1] C.Mangelsdorf: A 400 MHz Input Flash Converter with Error Correction, IEEE Journal of Solid State Circuits, Vol 25, No 1, 1990.