

A Low-Voltage Power and Area Efficient BiCMOS Log-Domain Filter

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ABSTRACT

A 3rd-order Chebyshev filter based on the log-domain principle and integrated in a 1 μm BiCMOS process is presented. It has a nominal cut-off frequency of 320 kHz corresponding to a bias current of 1 μA and can be frequency tuned over almost 3 decades up to about 10 MHz. It operates with a nominal supply voltage of 1.2 V maintaining a dynamic range (DR) at 1 % THD of 57 dB. For cut-off frequencies in the range of 10 kHz, the supply voltage can be reduced down to 0.9 V. The filter occupies an active area of 0.25 mm^2 and dissipates 23 μW , corresponding to a power consumption per pole and edge frequency of only 24 pJ. These results demonstrate the potential of log-domain filters for very low-voltage and low-power applications.

I. INTRODUCTION

In traditional linear transconductor-capacitor (g_m - C) filters, the transconductors have to be linearized in order to achieve the desired linear transfer function. This unavoidably increases the supply current required for implementing a given transconductance proportionally to the increase of the linear range, resulting in a poor current efficiency [1]. Moreover, this linearization also causes an increase of the minimum supply voltage in practical implementations. The recently introduced log-domain filter technique exploits the exponential characteristic of transistors for achieving an overall linear transfer function, it does not require any linearization and hence allow to avoid the related power consumption overhead [2], [3]. Moreover, it allows signal processing at supply voltages not so much higher than one junction voltage plus two saturation voltages of transistors at collector currents equal to the maximum signal current [4].

Therefore, the log-domain technique provides even at lowest supply voltages the most efficient use of the available current for implementing a given transconductance, which makes it very attractive for low-voltage and low-power integrated circuit design.

In contrast to class AB implementations, which allow ideally unlimited signal currents to be processed [5], the single-ended class A implementation presented in this paper consumes less power and is much less complex. Thanks to the good linearity of this circuit implementation, the theoretically maximum undistorted signal amplitude, equal to the bias current causes only a total harmonic distortion (THD) of 1 %. Therefore and because of its good noise performance, this filter achieves signal-to-noise ratios comparable or even superior to traditional filters needing higher supply voltages and dissipating much more power.

II. SIMPLE BICMOS LOG-DOMAIN INTEGRATOR

Fig. 1 shows the simplification of a BiCMOS implementation of a log-domain integrator [4]. It takes advantage of both, bipolar transistors and MOSFETs, available in a BiCMOS process. The accurate exponential characteristic of the bipolar transistors is needed to form the translinear loops, while MOSFETs were chosen everywhere else because they don't suffer from finite current gain, have lower saturation voltages, occupy less area, and P-channel MOSFETs offer a higher transit frequency than PNP bipolar transistors in the chosen process. On Fig. 1, two nested translinear loops can be identified. One of them is formed by the transistors Q2, Q4 - Q6, the other one by Q1, Q3, Q5 - Q6, they are implementing the equations:

$$i_{inp} \cdot I_b = i_{Cp} \cdot i_{out} , \quad i_{inn} \cdot I_b = i_{Cn} \cdot i_{out} \quad (1a, b)$$

Since Q5 is driven by a constant bias current, its base-emitter voltage is constant and the capacitor current i_C can be expressed in terms of v_{out} , and consequently also in terms of i_{out} .

$$i_C = i_{Cp} - i_{Cn} = -C \cdot \frac{dv_{out}}{dt} = -C \cdot \frac{dv_{out}}{di_{out}} \cdot \frac{di_{out}}{dt} = C \cdot V_T \cdot \frac{1}{i_{out}} \cdot \frac{di_{out}}{dt} \quad (2)$$

where $V_T = kT/q$ is the thermodynamic voltage.

Substituting (1a, b) in (2) results in a differential equation, describing a linear integrator:

$$\frac{di_{out}}{dt} = \frac{I_b}{C \cdot V_T} \cdot (i_{inp} - i_{inn}) , \quad i_{out} = \frac{I_b}{C \cdot V_T} \cdot \int (i_{inp} - i_{inn}) \cdot dt \quad (3a, b)$$

The unity gain frequency of this integrator is tuneable proportionally to the bias current I_b .

In contrast to the circuits of most other publications, here the distortion caused by the finite current gain of the bipolar transistors is effectively reduced, since the base currents of Q3, Q4 are merged to their collector currents and cause therefore only slight errors in the integrator's time constant. Only the base current of Q5 could affect the circuit's linearity, since it discharges the integration capacitor. Therefore, it is cancelled by another bias current I_b / β .

This implementation suffers from a slight mismatch between its non-inverting and its inverting input, since the base current of Q4 adds to its collector current, while the base and the collector current of Q3 are of opposite direction. Moreover, the current mirror M3-M4 introduces an additional delay time into the inverting path. These effects are causing a restricted attenuation in the transfer function of the filter.

III. LOG-DOMAIN FILTER IMPLEMENTATION

The schematic of the filter is shown in Fig. 3, it simulates a RLC ladder prototype structure of a 3rd-order Chebyshev low-pass filter with 1 dB pass-band ripple [4]. The capacitor values are $C1 = C3 = 22.5$ pF and $C2 = 11.5$ pF, respectively for a cut-off frequency of 320 kHz at a bias current of 1 μ A. It uses folded cascoded current mirrors for a reduced minimum supply voltage. These cascode MOSFETs require additional bias currents, which have to be cancelled to maintain lossless integrators, like for the second stage otherwise they act as a damping currents and make the integrator lossy, like for the first stage.

For compensating the 6 dB DC attenuation typical to the doubly terminated prototype structure, the size of the input transistor of the first integrator is doubled.

The 3rd-order Chebyshev filter was implemented in the 1 μ m B5CA BiCMOS process of Siemens. It is shown in Fig. 2. Including the bias block and the capacitors, it occupies a total area of about 0.25 mm². Without these blocks it measures less than 0.1 mm².

IV. MEASUREMENTS

Fig. 4 shows the frequency response of the single-ended filter, which can be tuned over about 3 decades with cut-off frequencies ranging from 10 kHz to 10 MHz at supply voltages comprised between 0.9 V and 1.8 V. For a 1.2 V supply, cut-off frequencies up to about 1 MHz can be achieved. The transfer functions of Fig. 4 have been measured setting the signal peak-to-peak input current equal to the bias current I_b . The supply voltage has then been adjusted to the minimum acceptable value for each individual curve. As shown in Fig. 4, this procedure introduces some dc gain errors which vanish when maintaining the same supply voltage for all the characteristics.

The THD measured at 1 kHz versus the input current peak-to-peak value is presented in Fig. 5 for two values of the bias current. Both measurements show that the filter can achieve good linearity (THD < 1 %) even for input current amplitudes close to the bias current. The output referred noise floor is 1.07 nA_{rms} for the 1 μ A bias current and 4.03 nA_{rms} for the 3 μ A bias current, resulting in a DR at 1 % THD of 57 dB and 52 dB, respectively. This shows, that the DR of log-domain filters is much less affected by the tuning than it is for linear filters. Ideally, it should even stay constant [6].

The filter linearity has also been checked in terms of intermodulation by measuring the fundamental and third-order intermodulation product at the filter output resulting from a duo tone input signal of equal amplitude with frequencies set at 99 kHz and 101 kHz, respectively. The extrapolated third-order input referred intercept point (IIP3) is equal to 8 μ A_{rms} (corresponding to 8 times the bias current). The noise floor has also been reported in Fig. 6 in order to evaluate the spurious-free dynamic range (SFDR) which is equal to 47 dB.

The quiescent power consumption is 23 μ W for a 1 μ A bias current and 59 μ W for a 3 μ A bias current. The performance of the filter are summarised in Tab. 1 together with the most important process characteristics.

V. CONCLUSION

A BiCMOS implementation of a 3rd-order Chebyshev low-pass filter was presented. Thanks to the log-domain filter principle, local linearization of the filter stages can be avoided. Therefore, this technique can lead to much more power efficient analog signal processing than conventional techniques even at supply voltages down to 1 V.

The presented results demonstrate the potential of log-domain filters for very low-voltage and low-power applications.

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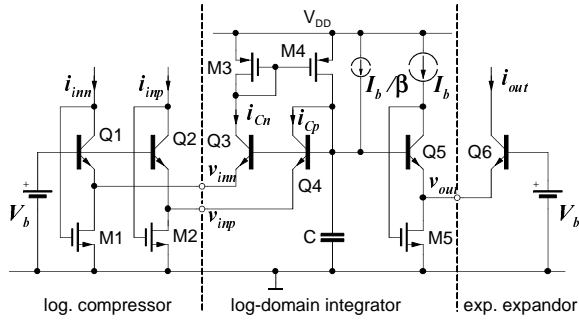


Fig. 1: Simplified log-domain integrator

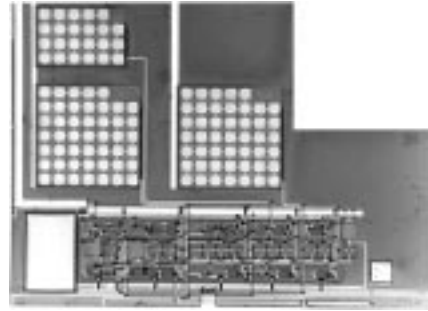


Fig. 2: Chip photograph

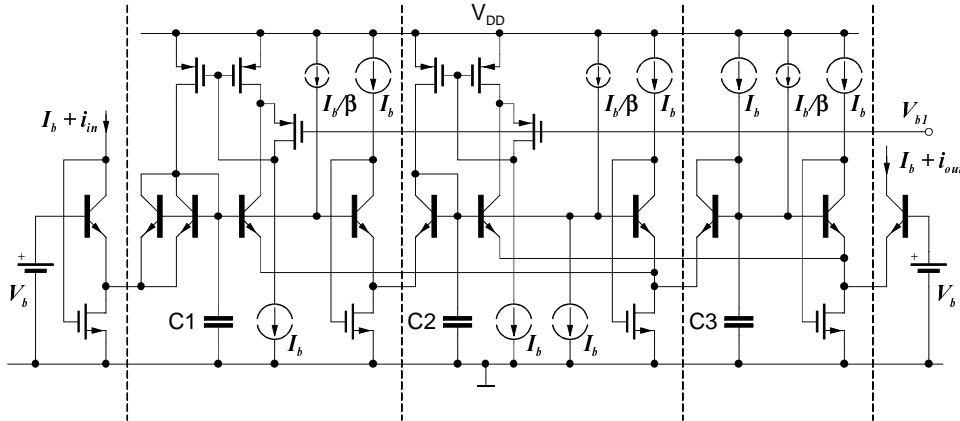


Fig. 3: 3rd-order Chebyshev log-domain filter

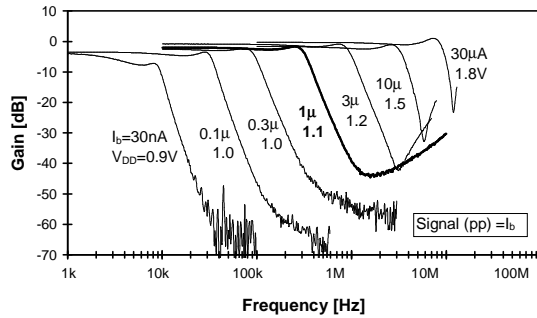


Fig. 4: Measured filter transfer functions

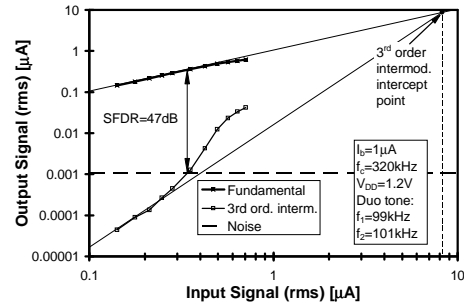


Fig. 6: Measured 3rd-order intermodulation

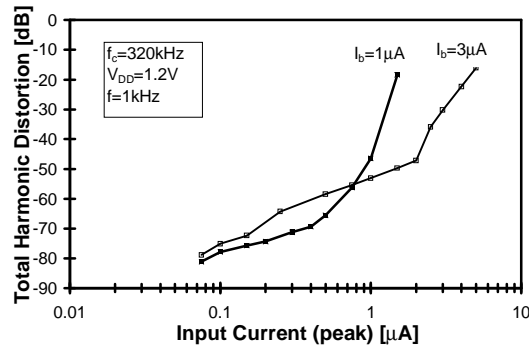


Fig. 5: Measured total harmonic distortion

Technology	1 μm BiCMOS	
BJT	$f_T = 6 \text{ GHz}$, $\beta = 80$	
MOSFETs	$V_{thN} = 0.7\text{V}$, $V_{thP} = -0.87\text{V}$	
Active area	0.25 mm^2	
Min. supply voltage	1.2 V (0.9 V - 1.8 V)	
Tuning range	3 dec : 10 kHz - 10 MHz	
Measurement conditions	$V_{DD} = 1.2\text{V}$, $I_b = 1 \mu\text{A}$	$V_{DD} = 1.2\text{V}$, $I_b = 3 \mu\text{A}$
Cut-off frequency (-3dB)	320 kHz	950 kHz
Noise current	1.07 nA_{rms}	4.03 nA_{rms}
Dynamic range (THD=1%)	57 dB	52 dB
Total power dissipation	23 μW	59 μW
Power dissipation per pole & cut-off frequency	24 pJ	20.5 pJ

Tab. 1: Table of performance