A 3.3 Volt, low distortion ISDN line driver with a novel quiescent current control circuit

H. Casier, dr. P. Wouters, B. Graindourze, D. Sallaerts

Alcatel Mietec
Raketstraat 62
B-1130 Brussels, Belgium
Tel.: +32 (2) 728 18 11 - Fax.: +32 (2) 726 42 15

Abstract - A single chip ISDN network terminator in an advanced 3.3 V, 0.5µ CMOS technology is presented. The circuit features a U-interface line driver with a THD better than -68 dB for an output swing of 5 V_{pp} on a 67 Ω load. A novel quiescent current control circuit is implemented which reduces the variation of the quiescent current and facilitates the driver's compensation.

1. Introduction

Narrowband ISDN (Integrated Services Digital Network) has been known for some years to be the next step in expanding the digital transmission capacity of the public telephone switching network. With its basic access, full duplex 144 kbit/s transmission rate (two B channels of 64 kbits/s and one D channel of 16 kbit/s), it offers the quadruple transmission rate of a sophisticated modem. The increased transmission capacity offers new types of services, e.g. facsimile transmission at 64 kbit/s, fast Internet access, or even transfer of low resolution video images such as video telephony.
It is expected that in the period '96 to '99 at least 5 million new lines will be installed worldwide every year. As a result, there is a real drive for highly integrated ISDN products, in particular for NT and LT equipment, to provide cost-effective solutions.

2. Basic system overview (figure 1)

At the subscriber premises a Network Termination (NT) box is installed, which links the subscriber's terminal (TE) to the Line Terminator (LT) at the exchange premises by means of the Uk0-interface (2B1Q or 4B3T encoding). This is the reference point identifying the 2-wire interface on the public level. Up to 8 digital terminals (phones, faxes, PC's) can be connected to the NT by means of a 4-wire S0-interface using AMI (Alternate Mark Inversion) coding. Each terminal can make independent connections to the exchange using one or both B channels and the D channel.

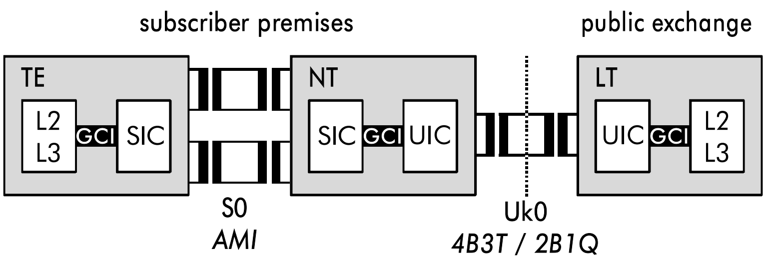

Figure 1 - Basic ISDN configuration

3. Description of the IC

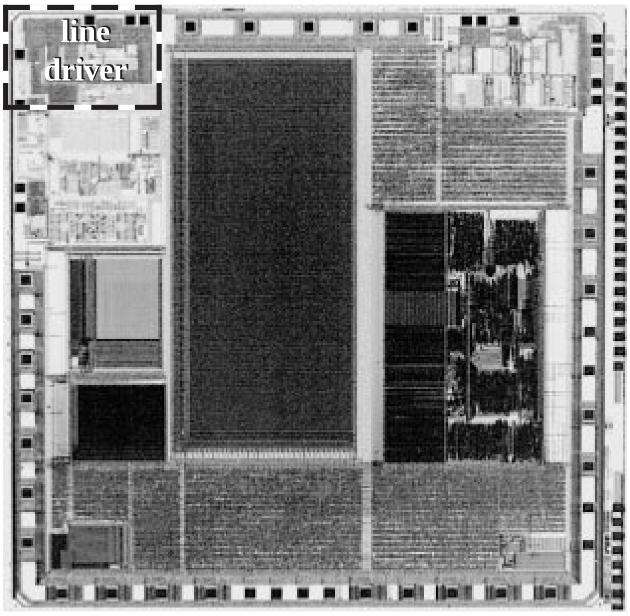

Figure 2 - Microphotograph of the chip

The U-interface driver described in this paper is part of a novel integrated circuit of which the microphotograph is shown in figure 2. This circuit integrates maximally all analog and digital functions of the U and S interface circuits for NT applications into a single mixed mode component. The IC is realized in an advanced 0.5 μm CMOS mixed analog-digital technology with double poly capacitors and three levels of metallization. It is operated from a single 3.3 V supply thus giving rise to low power consumption.

An embedded ARM7TDMI™ risc processor (*), running on a 31 MHz clock, takes care of the overall control. A dedicated coprocessor assists in arithmetic tasks such as echo cancellation, equalization and synchronization. The (de)scrambler, (de)coder, decimation filter, transmit shaping, digital GCI (General Circuit Interface) interface and the S-interface circuitry form dedicated blocks which are implemented in glue logic, under control of the ARM microcore. Both the U- and S-interface contain high performant, dedicated analog front ends for transmission and reception.

4. Transmit Path of the U-interface Analog Front End

The analog U transmit path consists of three major analog building blocks. The first block is a 1st order lowpass switched capacitor filter running on 7.68 MHz and having an accuracy of more than 12 bits in the band from 3 to 60 kHz. It is preceded by a digital pulse shaper, which generates the pdm signal by means of a 6th order sigma-delta modulator. Secondly, a 3rd order continuous time low pass Butterworth filter with a cutoff frequency of 138 kHz provides the input signal to the last block, namely the driver stage which is discussed in more detail in the next sections.

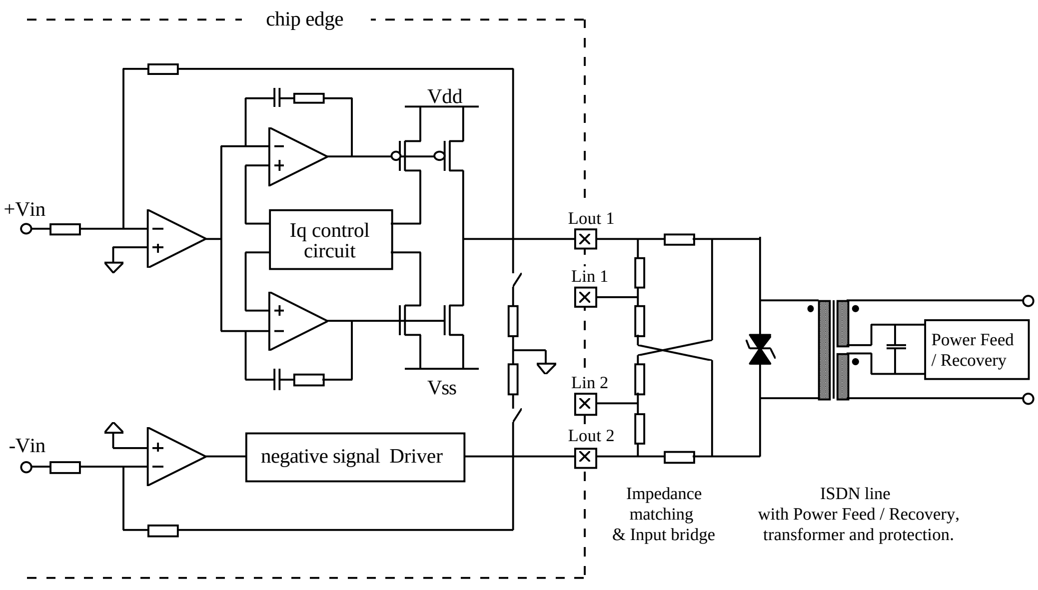

Figure 3 - ISDN Line Driver - Block Diagram

5. Driver circuit

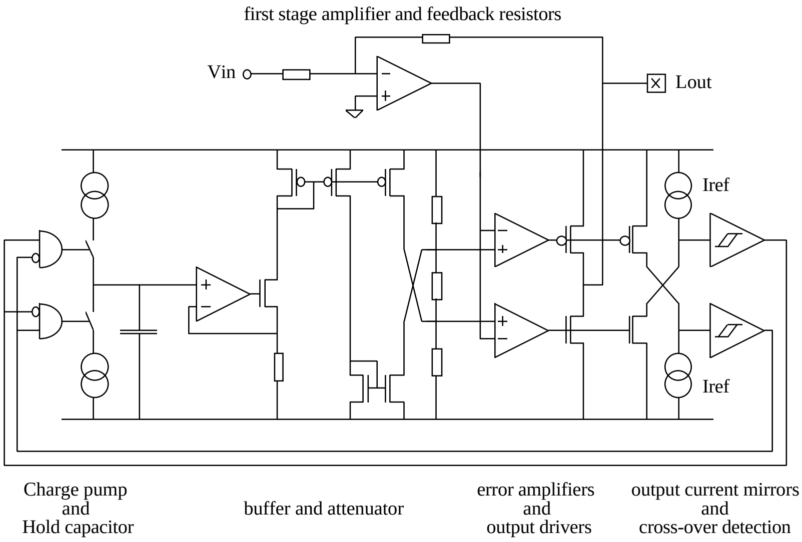

Figure 4 - Quiescent Current control circuit (**) : simplified schematic

The major challenge for the ISDN U-interface driver is to drive the worst case line load with low distortion from a supply voltage of 3.3 Volt ± 5%. With a line transformer ratio of 1:2, the 2B1Q signal requires a minimum output swing of 5 Volt ± 5% on a 67 Ω equivalent impedance.

The output driver is a standard pseudo-differential circuit with push-pull class A/B drivers [1,2-5]. Each driver is configured as an inverting amplifier with gain -1.42 with respect to the analog ground. A simplified block diagram of the output driver is shown in figure 3. In this figure, one of the driver stages is further detailed, showing the single ended, high gain first stage, followed by two lower gain error amplifiers, which drive the large PMOS and NMOS output transistors in the output stage. The output stage has an open loop gain variation of more than 20 dB with the output signal voltage and current and is the dominant distortion source. This distortion is reduced by the large gainbandwidth of the driver (≥ 10 Mhz).

The effect of the random offset voltage of the error amplifiers must be kept small since this could generate large quiescent current variations. This has previously been done by limiting the gain of the error amplifiers [2] or by adding a DC feedback loop [3,4] or current mirror technique [6, 7] for the quiescent current control or by combining a class B and class A/B output stage [5]. The novel quiescent current control (**) described below, compensates for the random offset variations of the error amplifiers and at the same time decouples the signal loop from the quiescent current control loop. The gain of the error amplifiers can now be increased to more than 40 dB with no common mode swing on their inputs. This results in a simple amplifier circuit and a straightforward pole splitting for the stabilisation of the whole driver (see figure 3).

A simplified schematic of the quiescent current control is shown in figure 4. The current through each of the output driver transistors is mirrored and compared to the given reference current I_{ref} in the cross-over detection circuit. Both digital comparator outputs are compared in a simple phase detector, which drives a charge pump to the hold capacitor C_{hold}. The timing diagram for the cross-over detection circuit and the phase detector is shown in figure 5. If the quiescent current is larger than the reference current, the capacitor is discharged, if it is lower, the capacitor is charged. Finally, a simple buffer with attenuator circuit transforms the hold capacitor voltage in the offset cancelling voltage for the error amplifiers.

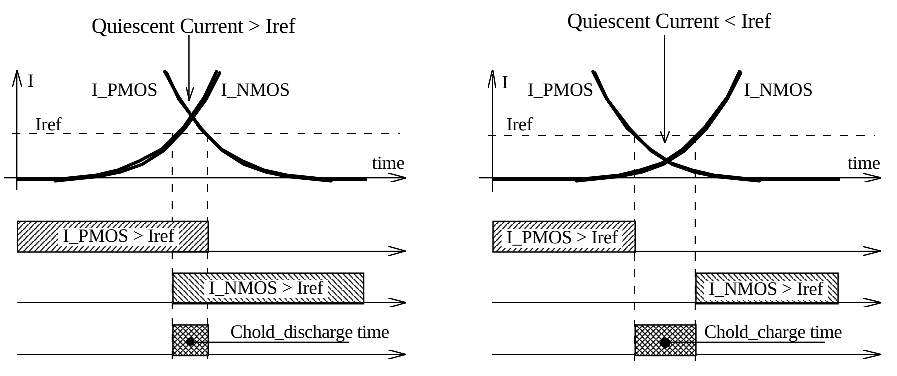

Figure 5 : Timing diagram for cross-over detection circuit and phase detector.

The described quiescent current control circuit only controls the amplitude of the quiescent current while the closed loop feedback resistors

of the line driver (figure 4) assure the symmetry between the PMOS and NMOS quiescent currents.
Several optimisations have been done during the layout of the driver. First, common centroid structures have been used where appropriate e.g. input stages. Next, the supply routing has been carefully layed out in order to limit the series resistances and the negative or positive signal feedback caused by them. Finally, both output driving transistors are connected to an output pad and are layed out according to the ESD/CDM rules for such transistors.

6. Measurement results

The measured performance of the U-interface driver is summarised in the following table:

power supply	3.135 ... 3.465 V
maximum output swing	5.25 V
power consumption (typical, 2B1Q, load excl.)	58 mW
THD for 3.3V, 27 °C, 3...60 kHz, 67 Ohm load, 5 V_{pp}	< -68 dB
output impedance	1 Ω in power up 5 Ω in power down
ESD performance	HBM > 2500 V CDM > 750 V

7. Conclusion

A 3.3 V, 0.5µ CMOS ISDN line driver is presented as part of a single chip solution for NT applications, containing both S- and U-interface circuits. A novel quiescent current control circuit is introduced. The THD is better than -68 dB for an output swing of 5 V_{pp} over a 67 Ω load.

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(*) ARM7TDMI is a registered trademark of Advanced RISC Machines Ltd, UK.
(**) A patent is pending for the quiescent current control circuit.