FET Mobility Degradation and Device Mismatch due to Packaging Induced Die Stress

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Abstract

CMOS FETs exhibit a stress sensitivity that is similar to classical piezoresistors in which mechanical stress induces changes in the FET transconductance through device mobility changes. Transconductance changes are a function of channel orientation, transistor location, and channel length. In plastic encapsulated die, it is demonstrated that NMOS transistors exhibit fairly uniform transconductance degradation, whereas PMOS devices can exhibit both degradation and enhancement. These changes can result in both degradation and increased spread of analog and digital circuit performance.

1. Introduction

CMOS integrated circuit design depends upon fabrication of well-matched field-effect transistors (FETs). Critical parameters to be matched include geometry, transconductance, and threshold voltage. This paper presents theoretical and experimental examples of FET transconductance degradation and mismatch due to mechanical stress in encapsulated die. Finite-element analyses, along with previously developed FET stress dependence equations are used to predict transconductance variation for both NMOS and PMOS devices across the surface of a die.

2. Transconductance Calculations

FETs on the (100) surface with channel lengths oriented along the [110] and $[\bar{1}10]$ directions respectively will have normalized transconductance variations with stress given approximately by

$$\left.\frac{\Delta g_m}{g_m}\right|_{[110]} = -\left[\frac{\Pi_S}{2}(\sigma'_{11}+\sigma'_{22}) + \frac{\Pi_{44}}{2}(\sigma'_{11}-\sigma'_{22}) + \Pi_{12}\sigma'_{33}\right] \qquad (1)$$

$$\left.\frac{\Delta g_m}{g_m}\right|_{[\bar{1}10]} = -\left[\frac{\Pi_S}{2}(\sigma'_{11}+\sigma'_{22}) - \frac{\Pi_{44}}{2}(\sigma'_{11}-\sigma'_{22}) + \Pi_{12}\sigma'_{33}\right] \qquad (2)$$

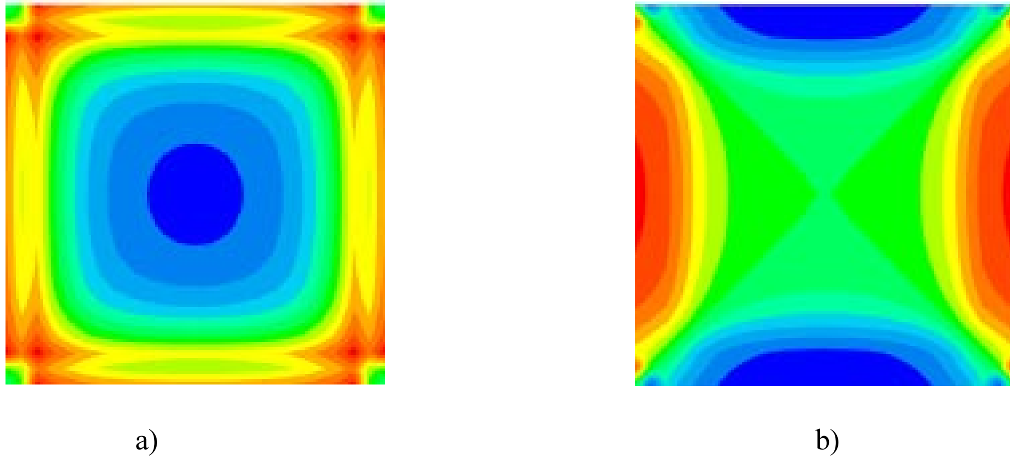
where the Π values denote the effective piezoresistive coefficients of the FETs, and σ'_{11}, σ'_{22}, and σ'_{33} are the three normal stresses at the die surface [1-3]. Table 1 presents the maximum values of piezoresistive coefficients for resistors, which generally place an upper bound on the FET piezoresistive coefficients in strong inversion. Previously reported results show FET values approaching 90% of those in Table 1 [1,2,4].

TABLE I
PIEZORESISTIVE COEFFICIENTS
FOR LIGHTLY DOPED SILICON

Piezoresistive Coefficient	N-Type Si (x 10^{-12} Pa^{-1})	P-Type Si (x 10^{-12} Pa^{-1})
Π_{11}	-1022	66
Π_{12}	534	-11
Π_{44}	-136	1381
$\Pi_S = \Pi_{11}+\Pi_{12}$	-488	55

4. Finite-Element Analysis

In order to predict transconductance variation due to stress using (1) and (2), one must first determine the stress components at the surface of the die. Finite-element simulation has been used to calculate both the sum and difference of the in-plane normal stresses for a 2.2 x 2.2 mm die encapsulated in plastic. Examples of the finite-element simulations are given in Fig. 1. A large compressive stress exists across the whole surface of the die as seen in Fig. 1 a), with maximum values of -120 MPa at the center, minimum values of -30 MPa near the corners. The normal stress difference reaches maximums of ±40 MPa along the die edges, and is approximately zero across most of the die. In larger die, considerably larger values of stress are predicted.



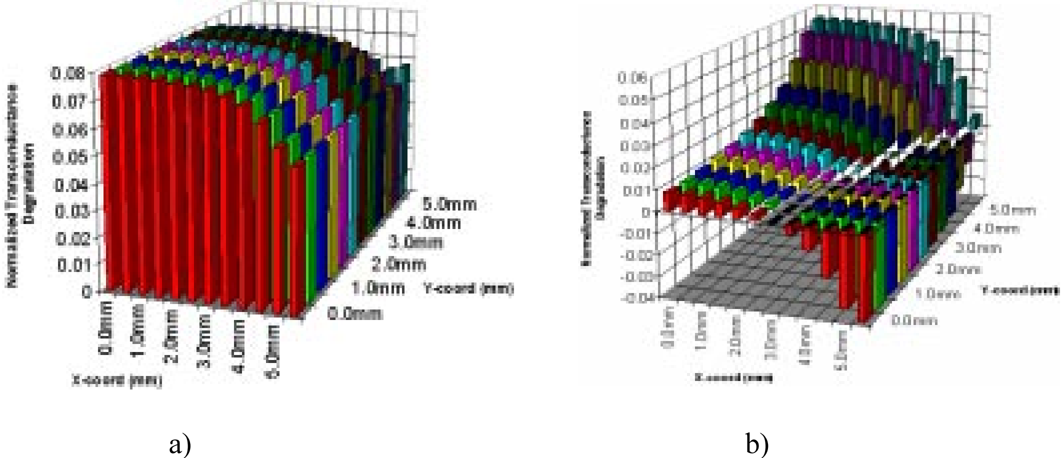
a) b)

Fig. 1. Finite-element calculations of a) $\sigma'_{11} + \sigma'_{22}$, and b) $\sigma'_{11} - \sigma'_{22}$ for a 2.2 mm x 2.2 mm die.

Based upon the predicted values of stress, and the piezoresistive coefficients in Table 1, the mobility and transconductance will vary significantly across the surface of the die. In the case of NMOS devices, the large Π_S term will tend to degrade the transconductance in a manner following $\sigma'_{11} + \sigma'_{22}$. The normalized transconductance degradation for one quarter of a 10 mm x 10 mm die is given as Fig. 2 a). The predicted degradation will be fairly uniform in the center of the die at nearly 8%, and becomes less pronounced near the edges (4%). We can expect degradation of many circuit performance parameters by this same factor.

In the case of a PMOS device, the large Π_{44} term will tend to change the transconductance in a manner following $\sigma'_{11} - \sigma'_{22}$ which changes sign in different quadrants of the die. The

PMOS transconductance degrades by up to 5% near the top edge of the die. The transconductance will increase however going from the center out to the right edge of the die. This indicates that the transconductance of two devices placed near opposite edges of the die could differ by as much as 10% as shown in Fig. 2 b). Also, note the opposite signs in the Π_{44} terms in (1) and (2). Even closely spaced orthogonal PMOS devices can experience a 10% spread in their characteristics [1,2].



a) b)

Fig. 2. Normalized transconductance variation over one quarter of a 10 x 10 mm die for a) NMOS devices, and b) PMOS devices.

5. Preliminary Encapsulation Results

A 2.2 x 2.2 mm MOSIS die containing both NMOS and PMOS orthogonal pairs was characterized and then subsequently encapsulated and re-characterized. Fig. 4 shows the change in normalized mobility due to encapsulation of the NMOS and PMOS orthogonal pairs.

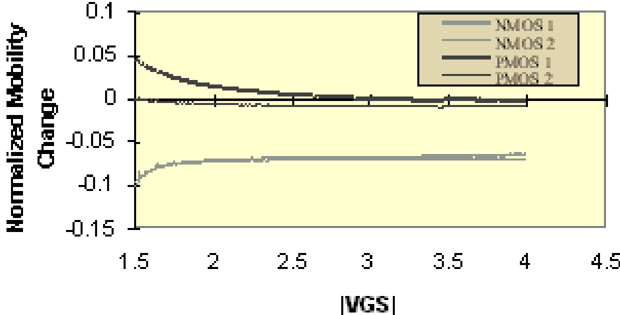


Fig. 4. Preliminary results of encapsulation of NMOS/PMOS pairs.

The NMOS devices were near the right edge of the die, and the PMOS devices were midway between the center and right edge. Notice that after encapsulation, the transconductance decreased by approximately 7% for both NMOS devices and 0-1% for the PMOS pair. The PMOS pair is in a region of much lower stress. However the spread of the characteristics due to transistor dependence on channel orientation is still observable [1].

6. Transistor Array

In an effort to corroborate the effects of encapsulation predicted by finite-element analysis, another MOSIS chip is being fabricated that contains an array of sensors. The design allows detailed characterization of both normal and shear stresses caused by die encapsulation [2]. The chip contains 49 sets of n- and p-channel FET pairs, 42 of which are equally spaced in one quadrant of the die. The remaining 7 sensor pairs are located along the edge of the die as shown in Fig. 5 and can be used to verify encapsulation stress symmetry.

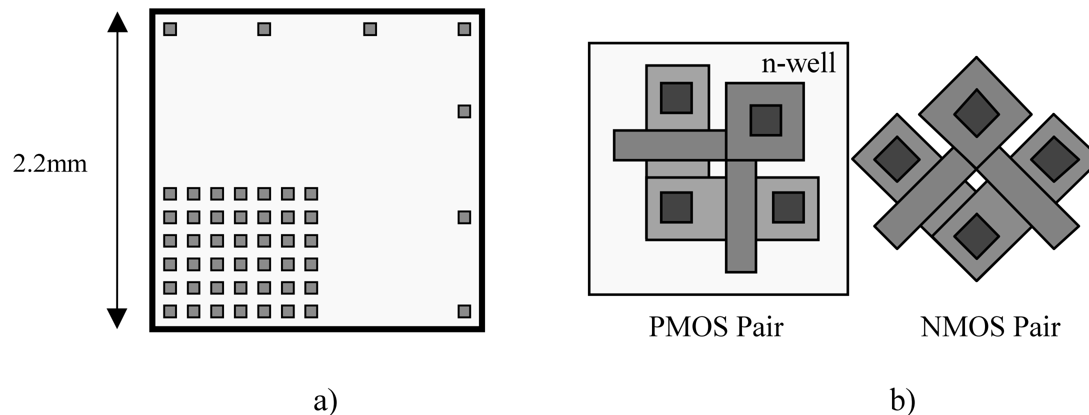


Fig. 5. a) Transistor array designed for encapsulation characterization,
b) individual stress sensors.

Conclusion

Theoretical calculations based upon finite-element analysis indicate that plastic encapsulation will cause mobility and transconductance to degrade in a fairly uniform manner for NMOS devices, whereas both enhancement and degradation can occur in PMOS devices. Initial encapsulation experiments are in general agreement with the finite-element predictions. Comprehensive measurement of device degradation and mismatch are in progress.[1]

References

(1) R.C. Jaeger, R. Ramani, and J. Suhling, “Effects of stress-induced mismatches on CMOS analog circuits,” *Proceedings of the 1995 International VLSI TSA Symposium*, Taipei, Taiwan, May 1995, pp. 354-360.

(2) R. C. Jaeger, R. Ramani, J. Suhling, and Y. Kang, “CMOS stress sensor circuits using piezoresistive field-effect transistors (PIFETs),” *1995 Symposium on VLSI Circuits Digest of Technical Papers*, June 1995, pp. 43-44.

(3) D.A. Bittle, et. al., “Piezoresistive stress sensors for structural analysis of electronic packages,” *Journal of Electronic Packaging*, vol. 113, 1991, pp. 203-215.

(4) Wang, J. Suski, and D. Collard, “Piezoresistive simulation in MOSFETs,” *Sensors and Actuators A*, vol. 37-38, pp. 357-364, 1993.

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