Single Bit Sigma-Delta Modulator with Nonlinear Quantization for µ-Law Coding

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Abstract

This paper presents a 1st order sigma-delta-modulator with µ-law coding for dynamic compression of audio signals. The nonlinearity is located in the feedback loop of the modulator and does not require an internal multibit A/D converter. The modulator requires just one opamp, one comparator, and a minimum of digital logic to generate a four bit feedback and to ensure a stable operation. The µ-law-function for µ=255 is approximated by a standardised piecewise linear 16 segment function which is commonly used in telecommunication. The chip has been designed and fabricated in a standard 1.5µm n-well CMOS process, occupies a die area of 2 mm^2, and has been successfully tested.

1. Introduction

Analog digital converters (ADC) based on the sigma-delta (ΣΔ) principle achieve a high signal to noise ratio (SNR) by combining oversampling, interpolation, and noise shaping while dispensing with the need of high precision anolog components. They rely on the noise spectrum of coarsely quantized input signal being shaped and shifted out of the signal band to higher frequencies to achieve fine quantization. Typically, the analog signal input of a 1st order ΣΔ-modulator is fed into a low resolution quantizer (often just 1 bit) via an integrator, while the quantized output is fed back and subtracted from the input. This feedback forces the average value of the coarsely quantized signal to track the analog input. The modulator is followed by a decimator which is a digital low pass filter combined with a subsampler. Its task is to reduce the shaped out-of-band quantization noise and to resample the digital output down to the Nyquist rate while restoring fine signal quantization.

If we wish to realize a fine nonlinear quantization based on ΣΔ-modulation two approaches can be adopted. Both use the interpolation characteristics of the modulator to approximate a nonlinear function with linear segments between two adjacent boundary nodes. The first idea is based on inserting a ROM, which contains the nonlinearity as a look-up table inside the decimation filter [1]. The nonlinearity is outside the modulator and has no influence on the signal/noise ratio SNR in this case.

The second principle based on multibit feedback that employs an internal nonlinear D/A converter (DAC) in the feedback loop. By assigning a logarithmic input-output characteristic to the internal DAC, it is possible to realize a ΣΔ-converter featuring dynamic compression [2]. The modified multibit feedback concept of our ΣΔ-μ-law coder is based on the second principle but avoids the use of a multibit ADC required otherwise. A detailed explanation follows in the next section.

2. The modified modulator concept

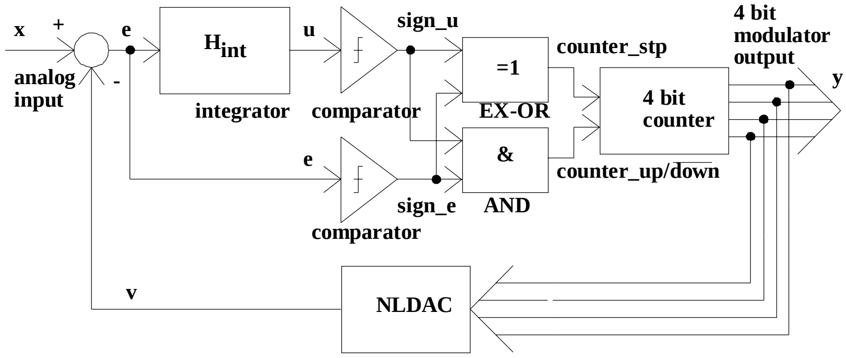

Fig. 1 The block diagram of the modified concept

Fig. 1 shows the signal flow in the ΣΔ-μ-law coder based on the multibit feedback principle. In order to obtain the desired nonlinear function y=F(x) between the input x and the output y, a feedback function is needed that corresponds to the inverse $F^{-1}(y)$ of the desired function F(x). Fig. 1 shows an example of a 1st order ΣΔ-modulator where the nonlinear function $F^{-1}(y)$ is realised by the nonlinear D/A converter (NLDAC) inserted into the feedback loop. The quantisation levels of the DAC correspond to the boundary nodes of the piecewise linear approximation of the inverse μ-law function. A 4 bit quantisation of the digital output y is necessary in order to obtain 16 boundary nodes required for the nonlinear function. The only conditions for realization of a nonlinear ΣΔ-modulator are the existence of the inverse function and the stability of the modulator with respect to the nonlinearity of the NLDAC, which in this case is the inverse μ-law function. That means that only strictly monotone functions can be realized.

To reduce hardware costs and eliminate possible nonidealities we have substituted the multibit ADC otherwise required by a comparator and a few logic gates. These additional components are necessary to generate the multibit feedback and digital output: the counter is used to generate a reduced delay between changes in the sign of the integrator output and the tracking of the digital feedback. In a way this could be compared to nonlinear filtering: the advantage when compared to linear filtering is, however, that this kind of nonlinear loop is inherently much more stable. The input signals to the logic are the sign of the input and output signal of the integrator (sign_e and sign_u). The four states of the signals were assigned to the counter operations in order to stabilize the feedback loop as follows:

1. sign_e $\neq$ sign_u:
   In this case the modulator forces the difference signal e at the integrator input towards zero without the need to change the current boundary node. Consequently, the counter state remains unchanged and the logic sets the counter_stp signal in order to freeze the output.

2. sign_e = sign_u:

   In this case the modulator cannot force the difference signal e towards zero without changing the output of the counter and so the logic has to make sure that the boundary node is increased or decreased. This causes a greater or smaller output signal y and in the next time steps the sign of the difference signal sign_e changes. If both signals sign_e and sign_u are positive the counter has to increase because in this case the output y growth up and consequently the difference signal e will change its sign. In the second case (sign_e<0 and sign_u<0) the counter has to decrease.

The counter control logic contains of only one AND-gate and one EXOR-gate as shown in Fig. 1. To reduce hardware costs the comparator that generates the sign_e signal uses the same opamp as the integrator in time-multiplex mode. In order to enable this, a 4 phase clock signal is internally generated from the external clock signal. So only one opamp is used for the operation of summation, integration, and comparison in the µ-law coder. For the generation of the signal sign_u an additional comparator is necessary which uses the phase ϕ_4. The nonlinear network in the feedback loop consists of a switched resistor and capacitor network for setting the boundary node in characteristics. The inverse µ-law function requires the electrical charge at the C-network to be divided by 256 and this is realized by combining voltage steps and switched arrays of sampling capacitors. **Fig. 2** shows the principle of the circuit realization. Although only a single signal path is shown, the actual circuit realization uses differential path technique.

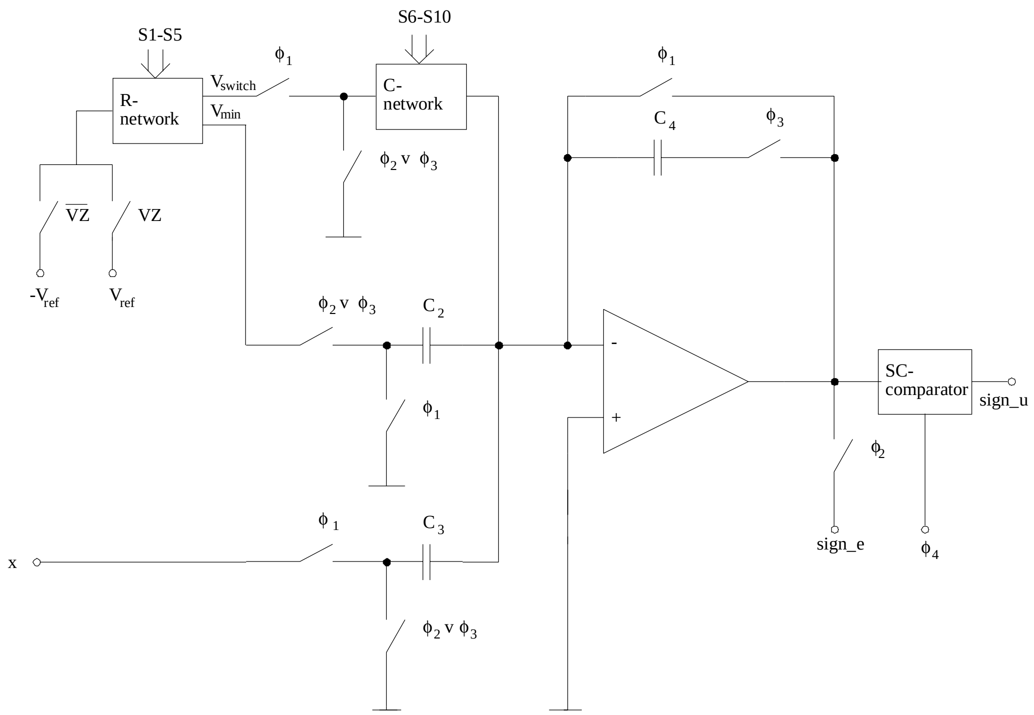

Fig. 2 The principle of the analog part of the µ-law coder

Thus in comparison to a standard 1st order ΣΔ-modulator the nonlinear coder requires an additional hardware amount consisting of one counter, two logic gates, and the nonlinearly quantized R- and SC-feedback networks with 8 levels and the sign.

3. Implementation and Results

The modulator has been designed and fabricated in a standard 1.5µm n-well CMOS process. The chip occupies an area of approximately 2 mm^2 without the pads. **Fig. 3** shows the simulation and measurement results of the µ-law function realized by the modulator for a DC-sweep from V_{in} = -1.5V up to V_{in} = +1.5V:

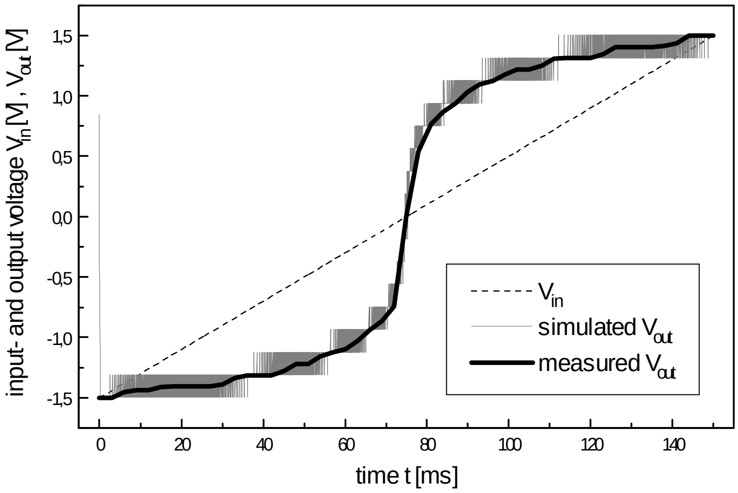

Fig. 3 Measured µ-law function of the coder

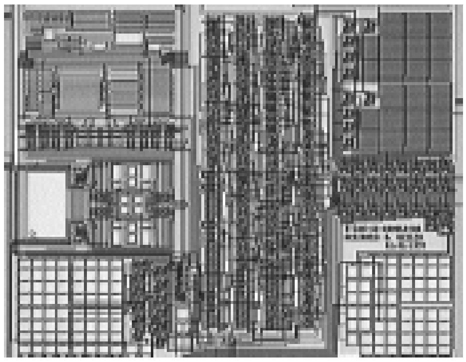

Fig. 4: Chip microphotograph

The plot shows the interpolating character of the modulator output. The measured modulator output is digitally filtered. The chip has been successfully tested and shows a good agreement between the simulated nonlinearity and the measured µ-law function.
The measured results are summarized in**Table 1**:

Power dissipation: 1.4mW	Sampling frequency: 250kHz	OSR: 64
SNR: 50dB betw. two boundary nodes	Technology: 1.5µm CMOS	Chip area: ca. 2mm^2

Table 1 Measured electrical parameters of the µ-law coder

4. Conclusions

A 1st order modified ΣΔ-modulator has been presented, which realizes a nonlinear µ-law coding with a minimum of hardware. The nonlinear network in the feedback loop reduces the quantization noise proportional to the quantization steps between the boundary nodes that are actually used to interpolate the output values. Thus the required sampling rate to acchieve accurate µ-law coding has been significantly reduced when compared to linear ΣΔ-conversion followed by digital µ-law coding .

5. References

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