

R, G, B acquisition interface with line locked clock generator, for LCD driver.

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ABSTRACT

This paper presents the analysis, design and experimental results of a triple 8 bits, 80 MSample/s Analogue-to-Digital acquisition channel with gain and clamp controls, together with a sample clock regenerator. While today's LCD driver systems require some 10 analogue integrated circuits, this single chip offers three 7.4 effective bits 300 MHz bandwidth acquisition channels, sampled by a 250 ps rms long-term jitter regenerated clock. This new level of integration and performances is reached through the implementation of a new clock regenerator architecture. The integrated circuit, available in a 100-pins plastic package, is realised in a 13 GHz, 1 μ m BiCMOS process and measures 25 mm². It dissipates 1 W from 5 V supplies.

1. Introduction

Today's LCD driver systems require analogue to digital conversion of the R, G, B video signals delivered by a PC or a workstation. They also require pixel clock regeneration from the horizontal video synchronisation signal. Fine delay control of the pixel clock allows optimum sampling when the video signals have settled. Figure 1 shows a simplified block diagram of the system, interfacing the PC and the display.

At present, graphic systems generally use fast video amplifier circuits, stand-alone ADCs and a programmable delay line circuit followed by a Phase Locked Loop circuit (for the pixel clock signal regeneration). All these integrated circuits require analogue or digital control signals, adding more complexity to the system. Because these applications use high rate digital clocks with sensitive analogue signals, attention should be paid for a careful board layout.

All these functions are now realised in one chip. This was possible due to highly integrated high speed ADCs and a new clock regenerator design.

2. Application

There are a number of constraints encountered in graphic application systems. Firstly, the video signals delivered by the RAMDAC (of the PC) have very steep edges and allow black to white transition within a small fraction of the pixel clock period. This means that these video signals do not have the band limitation of traditional TV signals. An analogue pre-processing bandwidth exceeding 250 MHz is necessary, in order to enable proper settling within one pixel clock period. However, the Signal-to-Noise Ratio (SNR) should be kept above 44 dB.

Secondly, LCD projection electronics is often close to a powerful light source, causing the IC temperature to change. In particular, the gain of the amplifiers should be independent of temperature. Moreover, accurate control of the clock delay enables sampling when the video signal has settled. Long-term clock jitter and reference breakthrough are key parameters for low noise acquisition. Finally, high pixel rate capability is a necessity for the most demanding graphic systems resolution.

3. Circuit design

3.1 Pixel clock regenerator

Phase control of the pixel clock is performed after frequency multiplication in contrast to the existing designs where a time delay is adjusted first (see Figure 2). An accurate phase delay is obtained through a weighted sum of VCO output signals, I and Q , which have a 90° phase difference. The phase diagram, in Figure 3, shows that these weighting factors can be accurately approximated by integer values ranging from 0 to 5. This produces phase delays in steps of 11.25° . The circuit realisation uses two transconductances, as shown in Figure 4. One transconductance processes the differential signals (I_p, I_n), and the other the signals (Q_p, Q_n). The digital signals (b_{ip}, b_{in}) switch currents through differential pairs. The signals (b_{1p}, b_{1n}), (b_{2p}, b_{2n}), and (b_{3p}, b_{3n}) select weights of 2, 2, and 1, respectively. The signal (b_{0p}, b_{0n}) controls inversion of the transconductance output. Thus, amplification by integer factors ranging from -5 to +5 provides phase control over a range of 360° .

Frequency multiplication is performed by a Charge Pump Phase Locked Loop (CPPLL) [1]. Its Phase Frequency Detector (PFD) avoids additional circuitry for capture. Setting the charge pump current and loop filter impedance also allows easy tuning of the PLL natural frequency (fn) and damping (ϵ). Performances can thus be optimised for each video format. Well-known equations are repeated here, in order to clarify the notations (fz is the zero frequency and fo is the unity gain frequency of the PLL open loop).

$$fn = \frac{1}{2\pi} \cdot \sqrt{\frac{Ip \cdot Ko}{C \cdot N}}, \quad \epsilon = \frac{fn}{2 \cdot fz} = \frac{fo}{2 \cdot fn}$$

Long-term time jitter originates mainly from the contribution of the VCO phase noise and the loop filter impedance thermal noise integrated over frequencies above the PLL bandwidth. Therefore, a wide-band PLL generates less jitter [2]. However a large PLL bandwidth means reduced reference breakthrough filtering. Hence, even a small leakage current (I_{leak}) at the loop filter capacitor node causes resynchronization pulses at each video line (at a frequency of f_{ref}). This generates VCO phase modulation. Simple derivation yields the pulses duration (Δt) and the peak-to-peak time modulation at the PLL output ($\Delta t_{o_{p-p}}$):

$$\Delta t = \frac{1}{f_{ref}} \cdot \frac{I_{leak}}{I_p}, \quad \Delta t_{o_{p-p}} = 2 \cdot \pi \cdot \frac{f_o}{f_{ref}} \cdot \Delta t$$

The loop bandwidth is optimised to avoid excessive jitter along with reference breakthrough. Large off-chip loop filter capacitors strongly reduce leakage current influence. They also avoid frequency drift when the PLL is in the coast mode (for certain video formats, line resynchronization pulses are missing during which the PLL charge-pump should be switched off).

3.2 Acquisition channels

The acquisition channel comprises a clamp, a voltage controlled gain amplifier (VGA), an ADC and a gain calibration circuit. The clamp is analogue allowing fast DC recovery. It uses the ADC reference voltages for easy black level adjustment. The number of VGA gain stages is reduced to two, to speed up settling and reduce noise. A Gilbert quad provides gain control. The ADC uses folding and interpolation techniques for area and power optimisation, while maintaining a high conversion rate. Finally, gain calibration of the overall acquisition channel versus an external reference voltage is possible. This feature offers excellent gain stability versus temperature and power supply.

4. Experimental results

This type of interface should deliver correct response to the so-called **Pixel On Pixel Off** test pattern. This means that the R, G, B signals toggle with the maximum amplitude at the highest repetition rate (half the pixel clock rate). Successful response requires fast acquisition settling, low long-term time-jitter and low reference breakthrough, (see Table 1, Figure 5 and Figure 6). The ADCs' can be clocked up to 80 MSample/s. Higher pixel clock rates can be achieved by two devices in a master-slave configuration. One device regenerates the clock and digitalises the even pixels. The other device digitalises the odd pixels.

5. Conclusions

A highly integrated R, G, B acquisition interface, based on a novel clock regenerator architecture, has been realised. Three high bandwidth frontends, driven by a regenerated clock with low jitter and reference breakthrough perform accurate digitalisation. This new level of integration and performances enables significant cost reduction of high end graphics systems.

6. Acknowledgements

The authors wish to thank all those at Philips Semiconductors Caen who contributes to the design, layout or measurement work.

7. References

- [1] Razavi, "Monolithic Phase-Locked Loops and clock recovery circuits", IEEE press, 1996.
- [2] W.P Robins, "Phase noise in signal sources", IEE telecommunications, 1991.

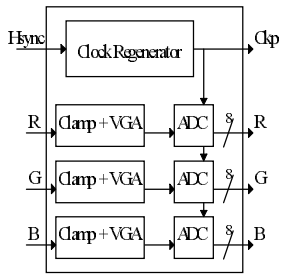


Figure 1 : R, G, B acquisition interface.

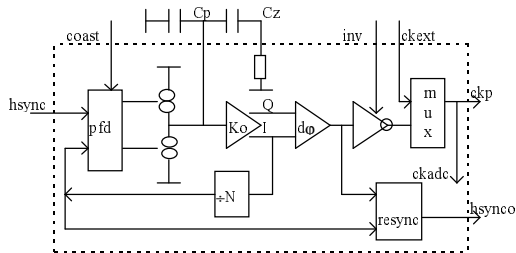


Figure 2 : Pixel clock regenerator.

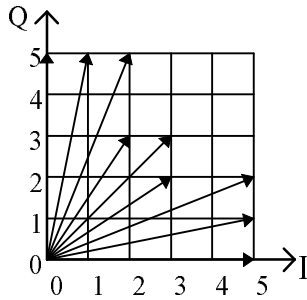


Figure 3 : Phaser diagram.

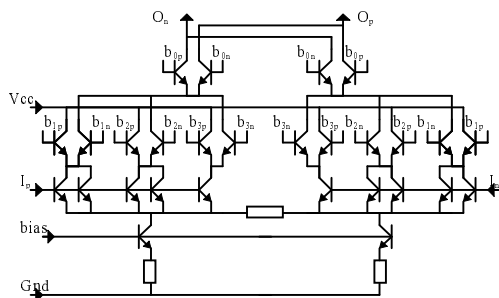


Figure 4 : Phase shifter transconductance.

Clock generator :

Frequency multiplication	16...4094
Phase control step	11.25°
Long-term jitter at 80 MHz	250 ps rms
Breakthrough at 80 MHz	400 ps p-p
Acquisition channels :	
Maximum conversion rate	80 MHz
1% settling	4 ns
SNR	46 dB
THD	55 dB

Table 1 : circuit performance summary.

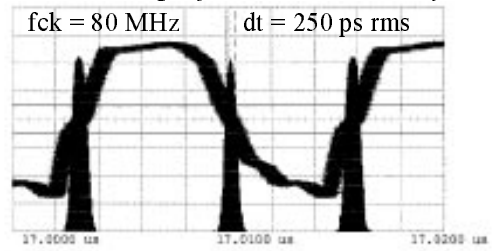


Figure 5 : Regenerated pixel clock signal and time jitter histogram, measured after one line period (17 μ s).

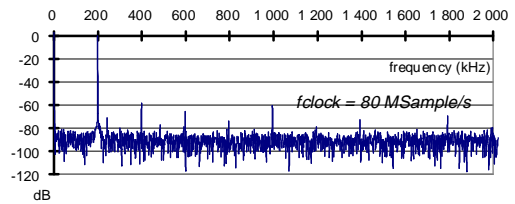


Figure 6 : FFT at acquisition channel output with 200 kHz sinewave input.

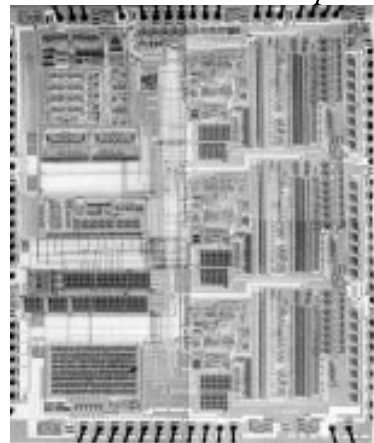


Figure 7 : Die photograph.

