DRAIN CURRENT MISMATCH IN SOI CMOS CURRENT MIRRORS AND D/A CONVERTERS DUE TO LOCALISED INTERNAL AND COUPLED HEATING

B M Tenbroek[1], M S L Lee[1], W Redman-White[1], C F Edwards[1],
M J Uren[2] and R J T Bunyan[2]

1 Department of Electronics and Computer Science, Southampton University, UK
2 DERA, Malvern, UK

ABSTRACT

Matching of transistor behaviour is critical to the functioning of many analogue circuits, and is usually controlled by device area and layout. This paper shows how highly localised heat generation and coupling can significantly alter the matching behaviour in circuits when fabricated in SOI CMOS.

Measurements and analyses are presented for simple current mirrors and a current output D/A converter fabricated in 0.7μm SOI CMOS which demonstrate the significance of these effects and how they can be accommodated in design.

INTRODUCTION

Transistor matching is an issue of great importance to the analogue designer, and it controls how well most of the common circuit configurations will operate. Many studies over the years (e.g. [1]) have shown that the degree to which two identically drawn devices behave alike can be described in terms of the gate areas and measured process related parameters. In traditional bulk VLSI CMOS it is an almost universal assumption that the circuits can be treated as isothermal, since the underlying substrate material has good thermal conductivity, and individual device power dissipations are relatively low.

These assumptions must be questioned in the context of VLSI CMOS on SOI. Although there are undoubted advantages over bulk for digital applications, in terms of device engineering, leakage current, packing density and of course, speed and power due to the reduced parasitic drain and source junction capacitances, there are drawbacks for analogue applications. In addition to the well known floating body effects when no body tie is used, the isolating buried oxide layer is of such low thermal conductivity (a factor of 100 worse than silicon) that even with the relatively moderate power levels encountered in typical signal path transistors, increases in the channel temperature of 10's of degrees due to self-heating can be observed. The heat generated can also have some influence on neighbouring transistors on the die, but the temperature gradients generated lead to non-isothermal conditions, and hence mismatch.

DEVICE LEVEL BEHAVIOUR

As power is dissipated in the channel of an SOI device, the temperature rises due to the poor thermal conductivity of the buried oxide. This oxide is often relatively thick. The localised temperature rise then affects the device's channel current through the mobility, threshold and velocity saturation mechanisms [2,3]. These effects can lead to a single device exhibiting very low or even negative output conductance due to this internal heat generation [4]. Figure 1 shows typical measured I-V characteristics for a 0.7µm MOSFET. The modelled curves are shown for comparison, both including self-heating and with self-heating removed by setting the thermal resistance to zero.

In addition to these static effects, the analogue designer must also be aware that the self-heating has a very marked frequency response. In effect, with very high frequency changes in a device operating conditions, the heat flow is effectively low-pass filtered, and eventually has no distinguishable frequency response, even though the local temperature may be quite elevated [2,5]. To investigate these issues several small analogue circuit cells have been fabricated in a 0.7µm process, and measured results and discussions of the mechanisms are now presented.

THERMAL GENERATED MISMATCH AND FEEDBACK IN CURRENT MIRRORS

The current mirror is one of the most frequently used circuit configurations, and it is of interest here because it relies for its operation solely on matching under isothermal conditions. To investigate the significance of self-heating and coupled heating, several simple mirrors were fabricated, each having the same device dimensions, but with different spacings in layout (figure 2). Conventional wisdom dictates that devices should be placed as closely as possible. In the SOI case, this also promotes thermal coupling between the reference and the output devices. The degree of thermal coupling can be derived from the change in gate voltage at the reference device as the drain voltage at the mirror output is varied [6]. Figure 3 shows that for the mirror with shared source layout, thermal feedback causes a shift of more than 50 mV in the effective threshold voltage of the reference device due to changing output device power dissipation. Even with 20µm spacing between devices, there is significant thermal coupling between output and reference. A thermal MOSFET model in SPICE [3] can be used to predict the channel temperatures, using measured thermal resistance parameters [2]. The change in reference device temperature due to output device power dissipation thus calculated is shown on the right hand side of figure 3.

Consider a typical application where a current mirror is used to provide several load current sources as illustrated in figure 4. In this circuit M1 and M2 are in close proximity while M3 is further removed. Suppose that M2 supplies current to a node where there is significant voltage excursion, while M3 supplies current to a node at a fixed voltage.

Considering only the electrical behaviour of the mirror, one would expect the current from M3 to be constant whatever the sink voltage of M2. However, the measurements in figure 5 show a significant change in the output current of M3 with changing sink level and hence power dissipation of M2. This demonstrates that a current source which should be completely fixed shows 1% variation due to thermal coupling between another output and the reference transistor. Time dependent coupling has also been observed.

THERMAL GENERATED MISMATCH IN D/A CONVERTER CIRCUITS

The ideality of current sources and the issue of mismatch is of central importance in the design of D/A converters, and the sizing of devices is normally undertaken with this as the key requirement. To investigate the impact of localised heating, a straightforward 7-bit current output D/A was designed and fabricated in a 0.7µm SOI CMOS process. The design specifically included an open drain output to allow the use of either a voltage source current sink at the output, or a simple resistor load to give a voltage output. The binary weighted current sources were made up of arrays of identical transistors each sharing the same gate reference as part of a large mirror structure (figure 6). Note that when any of the current source elements are not required at the output, they are connected to the VDD line in the usual way to minimise transients. The fabricated circuit is shown in figure 7.

When a voltage source sink is used at the output, there is no variation in the power dissipation between source elements, since the currents are essentially the same, and the drain-source voltages are fixed by the load. Hence, in the active state, each source will have the same local temperature unless there is an internal coupling mechanism along the mirror layout as discussed in the previous section.

The situation changes when one uses a resistor load (as is very common for video systems). Now the drain source voltage across any source that is selected is also a function of how many and which of the other sources are being selected. The power dissipation in an individual element and hence its current is therefore a function of the digital code applied. This can be seen best by using the thermal SPICE model to predict the channel temperature of one of the mirror elements as the input code is changed over a period time (16μs in this example, see figure 6). The device temperature (plotted as temperature increase with respect to ambient) is seen to start at a high value as the drain is connected to VDD in the "dump" condition. When the source in question is selected and current flows through the load, the drain voltage drops and so does the power dissipation. The channel temperature now drops with an exponential time constant, and its current output will thus increase slightly. At the next code the source is again connected to VDD, and the temperature starts to return to its original value. As more sources are selected, the output voltage drops still further, reducing individual current source dissipations and hence increasing their current contributions.

This thermal behaviour influences the linearity of the D/A converter, although it is not such a large effect, as it is in opposition to the familiar channel shortening behaviour. Figure 9 demonstrates this by showing the measured current step size at each code for the 7 bit D/A and simulations with and without self-heating. Without self-heating the step size would reduce with the output voltage level and hence with digital input. The self-heating opposes this channel shortening behaviour and the measured step size is seen to be approximately constant for all digital inputs as predicted by the SPICE simulation. For this particular example the influence of self-heating is noticeable but less significant than the random mismatch due to process variations.

CONCLUSIONS

Using measurements and special SOI MOSFET circuit level models, it has been demonstrated that self-heating and coupled heating can have a significant effect on commonly used circuit blocks when fabricated in SOI technology. Channel temperature rises of 10's of degrees are possible even at modest power dissipations, and the effects are dependent upon the layout as well as the circuit configuration. Circuit level simulations of these effects have been shown, and it is clear that such more advanced simulation tools are essential if designers are to accommodate these anomalies in successful VLSI analogue interfaces in SOI CMOS

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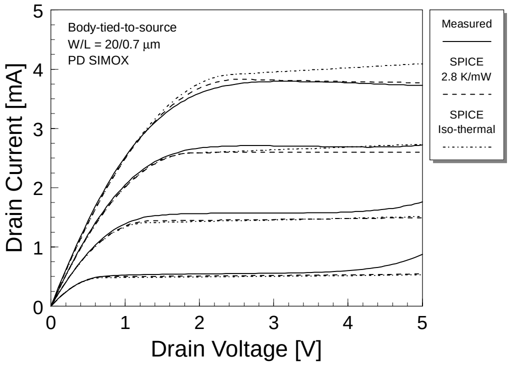

Figure 1: Measured I-V plot of a 0.7 µm MOSFET and SPICE simulations with and without self-heating.

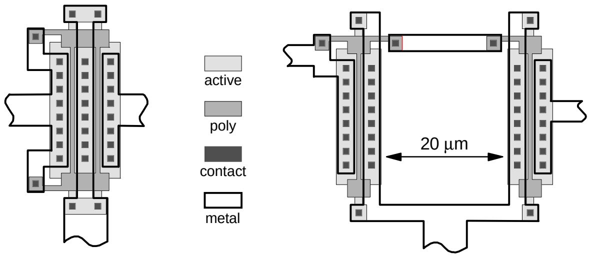

Figure 2: Shared source and separated mirror layouts.

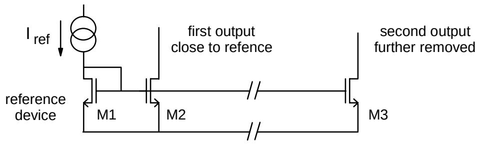

Figure 4: Schematic of current mirror with dual outputs.

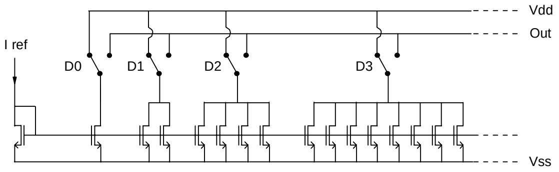

Figure 6: Schematic diagram of D/A architecture.

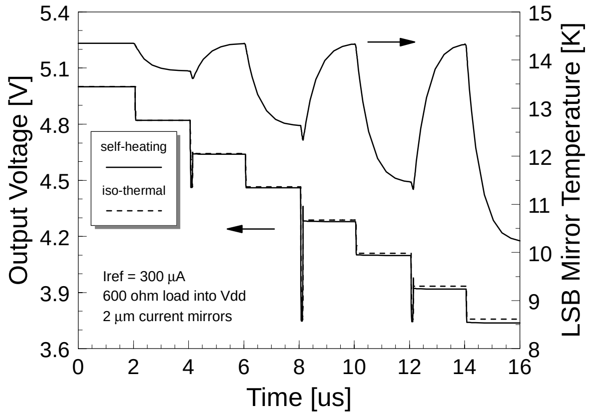

Figure 8: SPICE simulation of D/A output for first 8 codes and temperature increase of LSB mirror.

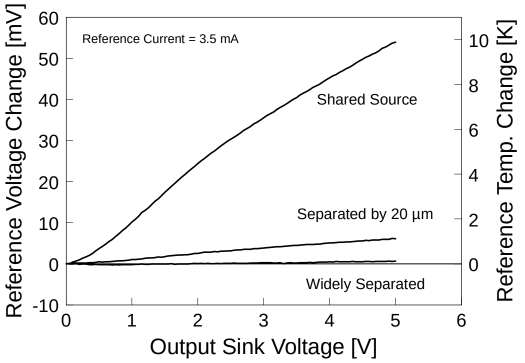

Figure 3: Thermal coupling in the mirrors of figure 2.

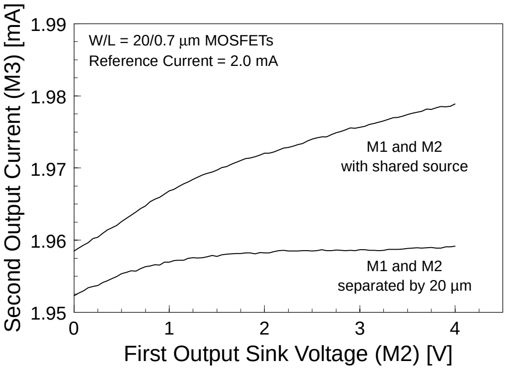

Figure 5: Thermal mismatch in dual output mirror.

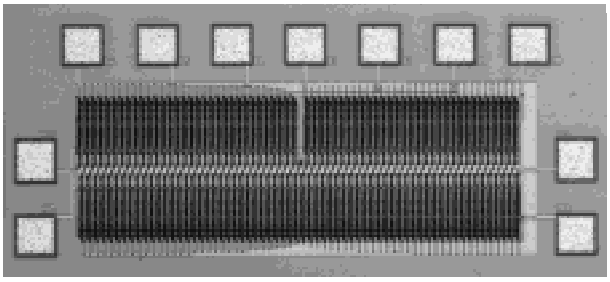

Figure 7: Chip photograph of the 7 bit current D/A.

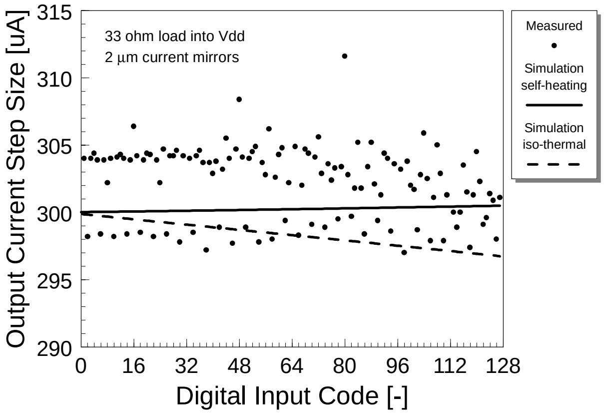

Figure 9: Measured and simulated output current step size versus digital input with and without self-heating.