

# A High Speed SRAM macro for 0.35 $\mu$ m Low Voltage SOI/CMOS Gate Arrays

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**Abstract-** A high-speed 2-port SRAM macro has been developed for 0.35 $\mu$ m SOI/CMOS gate arrays. The memory cell includes a new read buffer, which is composed of combinational gates, to reduce its area size and bit-line capacitances. The multiple read bit-line scheme was also adopted to reduce the access time in the SRAM macro. The test chips have been fabricated using both 0.35 $\mu$ m SOI/CMOS and bulk/CMOS processes. The access time of the 1.5K-bit (256word x 6bit) SOI SRAM was 2.6ns at 2.0V and 43% faster than that of the bulk counterpart. Even at the low supply voltage of 1.0V, the SOI SRAM operated at 6.4 ns.

## 1. Introduction

ASICs consist of several large macros such as RAMs and ROMs which often determine the speed performance and the power performance of chips. As the number of gates increases, the better performances: such as high-speed, low-power and low-voltage which are strongly demanded in large macros. The technique of reducing the access time and the power dissipation in multi-port SRAM macros has been reported for gate-isolated gate arrays [1]. This memory cell used a NAND-type read buffer enabling lower voltage operations. However, this read buffer configuration required additional transistors for isolation of the gates. Hence, it made a larger area size and the greater junction capacitance.

With reference to the device technology, SOI/CMOS devices are attractive candidates for high-speed and low-power ULSIs because of their smaller junction capacitances and reduced back-gate bias effects. A partially-depleted SOI/CMOS gate array has been recently reported [2]. This gate array used the field-shield isolation technique to allow the use of cell libraries and design methodologies compatible with bulk/CMOS gate arrays.

We propose in this paper a new memory cell circuit, where excess gates were eliminated by contriving the read buffer. Smaller bit-line capacitances can be accomplished which results in the reduced access time of the memory cell. The test chips were fabricated using 0.35 $\mu$ m SOI/CMOS process with field-shield isolation. The SOI SRAM showed superior speed performance even at the lower supply voltages.

The content of this paper is as follows. In section 2, we describe the proposed 2-port memory cell and the multiple bit-line scheme in detail. Section 3 shows the partially-depleted SOI/CMOS gate arrays using field-shield isolation. Finally, we demonstrate the experimental results.

## 2. SRAM Memory Cells

Figure 1 (a) and (b) show the proposed and the conventional [1] 2-port memory cells, respectively. These memory cells contain the read buffer to stabilize their stored data preventing memory loss. The read buffers drive the read-bit-line to its full-swing voltage to enable lower voltage operations.

In the proposed memory cell the read buffer has the AND-NOR combinational gate, which was modified from the conventional NAND-type gate to minimize the memory pattern layout. The inputs of the AND-NOR gate are connected to the storage nodes of the memory cell pairs (m0 and m1) and the read-word-lines (R1WL0 and R1WL1). The output of the AND-NOR gate is connected to the PMOS transistor p1 and the NMOS transistors, n2 and n4. The drains of the NMOS transistors, n1 and n3, are connected to the read-bit-line, while the gates of these transistors are tied to their read-word-lines.

In the read operation, only one of the read-word-lines of all rows among all of the rows goes to high-level. This read-word-line is specified by the address inputs. When the storage

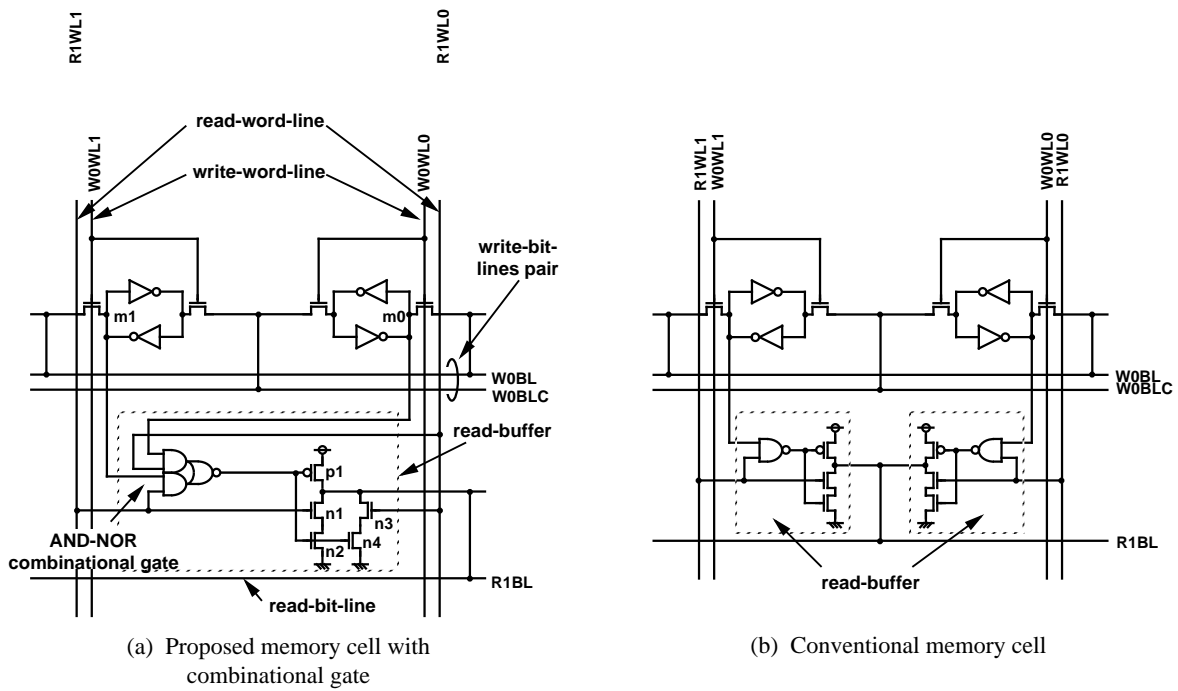


Fig.1 Memory cells for 2-port SRAM

data of the selected memory cell is high-level, the output of the AND-NOR gate goes to low-level. Then, transistor p1 drives the read-bit-line to high-level. On the other hand, when the storage data is low-level, the output of the AND-NOR gate goes to high-level. Therefore, the read-bit-line is discharged through two NMOS transistors, n1 and n2.

The memory cells were designed for 0.35 $\mu\text{m}$  gate arrays. Fig. 2 shows the physical layout of the 4 bits of the 2-port memory cells. The basic-cell (BC), which consists of a PMOS transistor and a NMOS transistor, is 1.6 $\mu\text{m}$  x 26.0 $\mu\text{m}$  in size. Each word-line is the vertical 2nd-metal, while each bit-line is the horizontal 1st-metal. The upper-row of the basic-cell arrays is apportioned to the write-port, while the lower-row is assigned to the read-port. By contriving the AND-NOR gate, there is no isolation gate for the NMOS transistors. The 1-bit memory cell in the proposed circuit configuration consists of 8 basic-cells. The memory cell area is 11% smaller than that of the conventional memory cell which requires 9 basic-cells including the isolation gate [1]. The memory cell size is 6.4 $\mu\text{m}$  wide by 52.0  $\mu\text{m}$  high having an area of 332.8 $\mu\text{m}^2$ . Adjacent transistors share all source/drain regions of the NMOS transistors. Therefore, the junction capacitance added to the read-bit-line in the proposed read buffer can be reduced to 75% compared with that of the conventional buffer [1].

As shown in Fig.1(a) and Fig.2, the source/drain regions of the NMOS transistors, n1 and n3, are connected to the read-bit-line

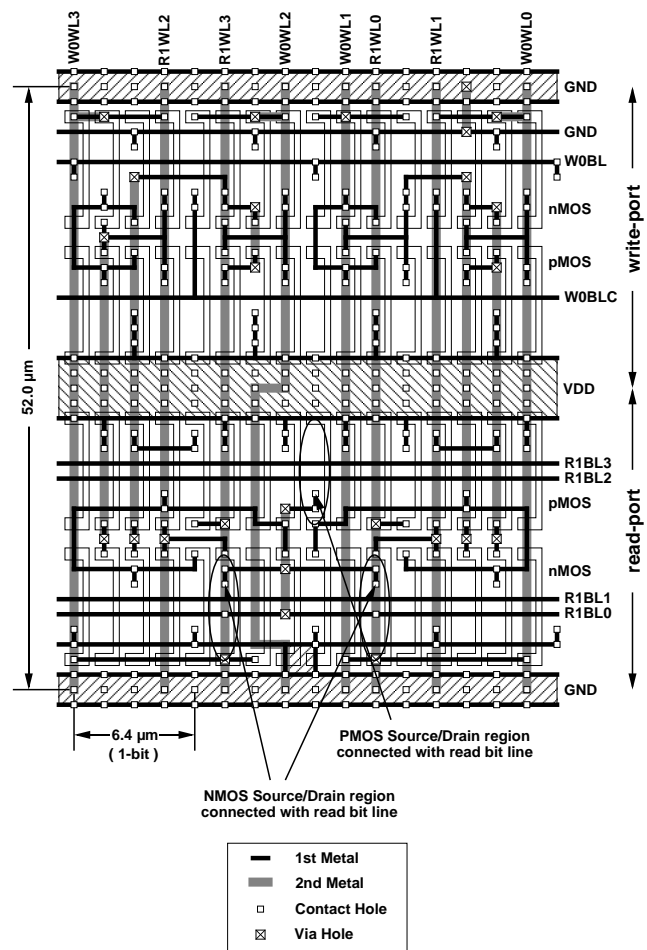


Fig.2 Layout of 4-bit memory cells with combinational gates

every other word. Otherwise, the source/drain regions of the PMOS transistor, p1 are connected to the read-bit-line every 4 words.

Figure 3(a) and (b) shows the multiple read-bit-line scheme. The n-bit lines ( $n \geq 1$ ) correspond to one column and are connected to the memory cells alternatively. Figure (a) and (b) show the column of memory cell arrays when  $n=1$  and  $n=4$ , respectively. As was mentioned in the report[1], the value of n equaled 4, giving it name "fourfold read bit line technique". The source/drain capacitance of the bit line at  $n=4$  equals one-fourth as much as at  $n=1$ . In this paper, we adopted both  $n=1$  and  $n=4$ , in order to verify the advantages of multi-bit-line scheme in SOI/CMOS gate arrays.

### 3. SOI/CMOS Gate Arrays

Figure 4 shows the basic cell structures of SOI/CMOS and bulk/CMOS gate arrays where the gate isolation technique is adopted. The SOI/CMOS basic cell utilizes the field-shield gates to isolate the PMOS and the NMOS transistors [2]. Field-shield isolation technique allows the use of cell libraries and design methodologies compatible with bulk/CMOS one without any area overhead. Therefore, we can use the same metalizations of the memory cell (Fig. 2) on the SOI/CMOS and bulk/CMOS gate arrays.

### 4. Experimental Results

In order to verify the performance of the SRAM macros, the test chips were designed and fabricated using both 0.35 $\mu\text{m}$  SOI/CMOS and bulk/CMOS processes. The device features are summarized in Table-1. Figure 5 shows the microphotograph of the test chip which includes 220K usable gates in the sea-of-gate array. The chip size is 7.2mm x 7.4mm.

The chip contains eight types of 2-port SRAMs. Half of the test chip contain 1.5K-bit 2-port SRAMs (A-D) with 6 bits by 256 words configuration, and the other half contain 0.78K-bit 2-port SRAMs (E-H) with 25 bits by 32 words configuration. All eight types of 2-port SRAMs combined total 9.2K-bit, and the total number of transistors is 186.4K which includes the I/O buffer blocks and the test circuits. The memory cell type, the read-bit-line structure, and the measured access time are summarized in Table-2.

When using the single read-bit-line ( $n=1$ ), the access time improved in the SOI/CMOS and in the bulk/CMOS SRAMs after adopting the new memory cell. Table-2 shows that the multiple read-bit-line scheme is greatly effective for the reduction of the access time.

Figure 6 shows the access time versus the supply voltage of the 1.5K-bit (6b x 256w) SRAM (D). The access time of the SOI SRAM which is 2.6ns at 2.0V. This is 43% faster than that of the bulk SRAM which is approximately equal to that of bulk/CMOS at 3.6V.

Figure 7 shows an example of the "shmoo plot" of 1.5K-bit SOI SRAM (D) for the access time versus the supply voltage. It was verified that the SOI RAM operates at supply voltages over 0.8V. Even at a low supply voltage of 1.0V, the SOI SRAM operated at 6.4 ns.

### 5. Conclusion

A high-speed and low-voltage 2-port SRAM macro has been successfully developed for SOI/CMOS gate arrays. The SRAM macro adopted a new read buffer composed of combinational gates which reduces the area size by 11% and reduces the junction capacitance of the read-bit-line by 25% compared with the conventional circuit. The multiple read bit-line scheme was also adopted to reduce the access times in the SRAM macro. The test chips were fabricated by both 0.35 $\mu\text{m}$  SOI/CMOS and bulk/CMOS processes. The access time of the 1.5K-bit (256word x 6bit) SOI SRAM was 2.6ns at 2.0V and 43% faster than that of the bulk counterpart. Even at a low supply voltage of 1.0V, the SOI SRAM operated at 6.4 ns.

### Acknowledgment

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### References

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- [2] K.Ueda, et. al., "A CAD-Compatible SOI/CMOS Gate Array having Body-Fixed Partially Depleted Transistors", IEEE 1997 ISSCC, 17:2.

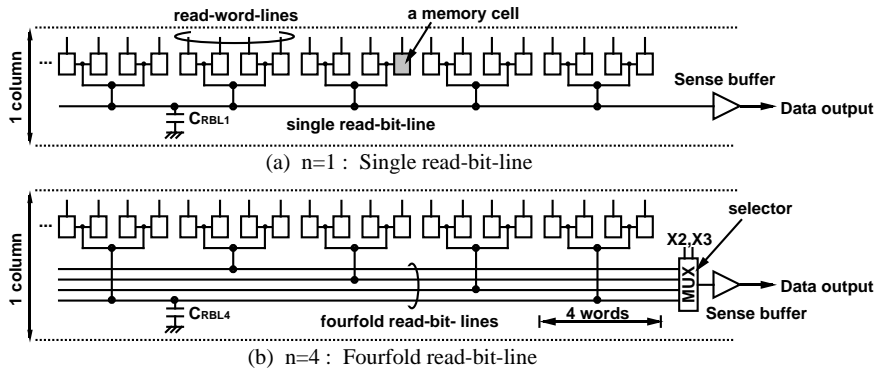


Fig.3 Multiple read-bit-line scheme

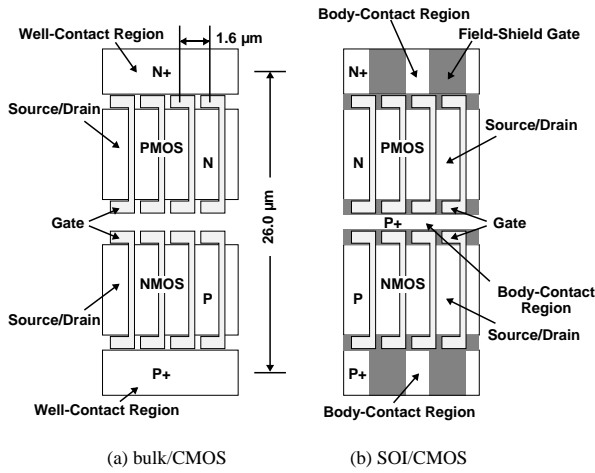


Fig. 4 Basic-cell Structures for 0.35µm Gate Arrays

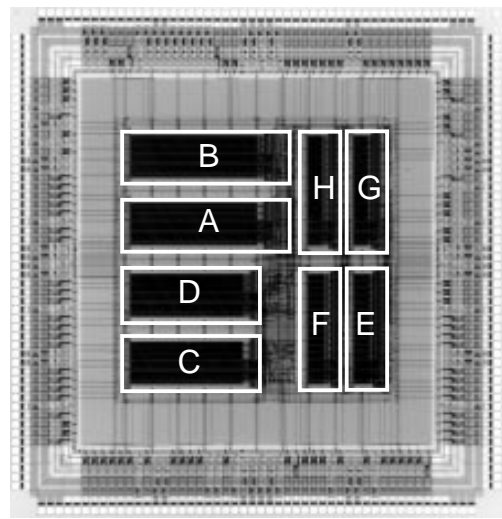


Fig.5 Microphotograph of the test chip

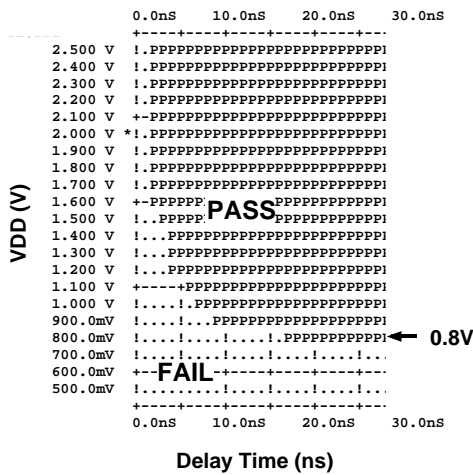


Fig.7 Shmoo plot of SOI/CMOS SRAM (RAM-D:1.5K-bit)

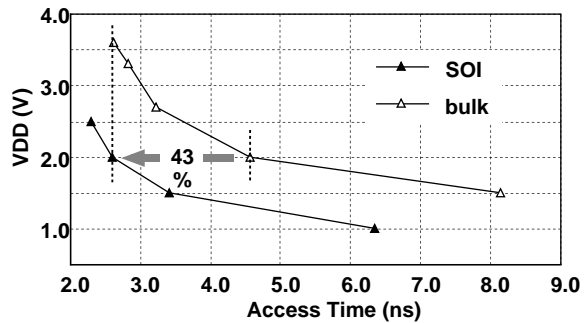


Fig.6 Access times of 1.5K-bit 2-port SRAMs

Table 1 Device features

	SOI	Bulk
Lp/Ln [µm]	0.40 / 0.35	0.40 / 0.35
Vtp [V]	0.43	0.70
Vtn [V]	0.22	0.50
Idp [mA]	1.1 @2.0V	2.9 @3.3V
Idn [mA]	3.9 @2.0V	5.7 @3.3V

Table 2 Configurations and Access times of the SRAMs

Configurations	RAMs	memory cell type	# of Read Bit Lines	Access Time [ns]		
				SOI@2.0V	Bulk@2.0V	Bulk@3.3V
6-bits x 256-words (1.5Kbit)	A	NAND	1	4.1	8.6	5.5
	B	AND-NOR	1	3.9	7.5	4.7
	C	NAND	4	2.6	4.8	3.0
	D	AND-NOR	4	2.6	4.6	2.8
25-bits x 32-words (0.78Kbit)	E	NAND	1	2.1	3.5	2.1
	F	AND-NOR	1	2.1	3.5	2.1
	G	NAND	4	2.0	3.3	1.9
	H	AND-NOR	4	2.0	3.3	1.9