

A Fully-Integrated CMOS AM Radio Receiver for Wrist-watch Calibration

F. Op 't Eynde, P. Cathelin, N. Krasnanski⁽¹⁾

Mixed Silicon Structures (MS2), 2, Blvd du Général Leclerc, Roubaix, France

⁽¹⁾ Info Réalité, Rue de la Forêt, Vendenheim, France

Abstract: *In this paper, a CMOS AM radio receiver ASIC is presented. The antenna and a 32-kHz oscillator crystal are the only required external components. The ASIC is dedicated to the 162-kHz « Allouis » radio transmitter. It allows to decode digital data, encoded as a phase modulation of the carrier frequency.*

I. Introduction

From a village called « Allouis », about 100 km South of Paris, a 1000-kW radio transmitter is broadcasting a standard AM radio music signal with a carrier frequency of 162 kHz. As an additional, particular feature, the transmitter is broadcasting a 40-bit/sec. digital data signal simultaneously with the audio information [1]. This data is encoded as a phase modulation of the carrier frequency. 15 bit/sec. are used to communicate the exact time once per minute. The remaining 25 bit/sec are available for various applications. In this way, the « Allouis » radio transmitter offers an alternative for the DCF77 transmitter.

Since the transmitter frequency is situated in the « Long-Waves » band, the radio signal is following the earth curvature over long distances. Field trials have shown that the phase modulation can be decoded at distances up to 3000 km. This radius covers most of Europe, including cities as Dublin, Oslo, Helsinki, Warsaw, Minsk, Ankara, Algiers, Casablanca, etc.

The presented ASIC is designed to receive this 162-kHz radio signal and to decode the digital information. Thanks to a low supply voltage, a low power consumption and a reduced number of external components, the circuit can be built in a wrist-watch.

II. The ASIC architecture

The digital data is transmitted as a tri-level phase modulation of the radio signal carrier [1]. The phase varies between +1 rad, -1 rad and zero, with an average equal to zero. The transmitter output signal spectrum is depicted in Fig. 1. The two side bands at $\pm[300 \text{ Hz}, 3.3 \text{ kHz}]$ contain the AM audio information while the digital phase-modulated information is situated in the central band. This band has a bandwidth of about 100 Hz.

The receiver block diagram is shown in Fig. 2. The 162-kHz antenna signal is applied to a Low-Noise input amplifier (LNA) with variable gain. The LNA output signal is mixed with two 163.84-kHz quadrature signals obtained from a synthesized Local-Oscillator (PLL1). The PLL frequency is derived from a crystal oscillator (XTAL). The two mixer output signals are applied to two lowpass filters (LPF) with variable-gain amplifier stages (VGA) and then mixed again with two quadrature signals at 2409 Hz. It can be verified that the two resulting output signals at 569 Hz are in-phase. They are applied to a summator circuit and

subsequently to a bandpass filter (BPF). This filter has a bandwidth of 150 Hz, centered around 569 Hz. With a comparator (COMP), the filter output signal is converted to a digital format, hereby eliminating all residual AM modulation. This double-conversion architecture offers the advantage of image rejection, without the need for the commonly-used 90° phase-shifter.

The variable gain stages are controlled by an on-chip AGC circuit. Thanks to this AGC, the comparator input amplitude is kept constant at 100mVp, independent of the input signal amplitude.

All filters are on-chip Continuous-Time filters, controlled by a tuning PLL (PLL2) [2].

In order to decode the phase-modulated information, a digital PLL (PLL3) with a slow time constant is implemented. Since the signal phase modulation is varying much faster than this PLL time constant, the PLL cannot track the phase variations [3]. It is therefore locking to the average input signal phase. Hence, an unmodulated replica of the PLL3 input signal is available at the output. The phase difference between the PLL3 input and output signals is identical to the original radio signal phase modulation. This phase difference can be easily measured by a digital counter.

In order to improve the ASIC noise immunity, the measured phase difference is averaged over five periods of the 569-Hz signal. Further noise improvement is obtained by an on-chip Viterbi decoder. System simulations have shown that this phase demodulator can operate with an SNR of 6 dB at the comparator input.

Since the ASIC is foreseen to function with a ferrite antenna, the overall receiver is strongly directive. In order to improve this, an optional second antenna input is foreseen. The second antenna is placed perpendicular to the first one. By introducing an on-chip 90° phase-shift to the second antenna signal, the sum of both antenna signals becomes independent of the antenna orientation.

The ASIC output signal is compatible with existing ASICs for the DCF77 signal.

III. The practical implementation and measurement results

The receiver circuit is realized in a 1.5 μ m CMOS technology. The technology features nMOS and pMOS transistors with a low threshold voltage, double-poly capacitors and high-ohmic resistors. A chip microphotograph is shown in Figure 3.

All circuits in the signal path are fully-differential. The LNA schematic is depicted in Figure 4. It contains two differential-pair gain stages, placed in parallel. Because of the degeneration resistor in the first pair, the gain of this stage is only about 0 dB, while the second gain stage offers a gain of about 25 dB. By means of a gain control voltage « V_c », the bias current can be gradually switched from the first pair to the second one. This allows to vary the gain from 0 dB to 25 dB. When the gain is maximum, only the non-degenerated pair is operating, hereby offering a minimum equivalent input noise voltage. On the other hand, when the gain is minimum, only the degenerated pair is operating, hereby offering a maximum linearity. The measured LNA gain is shown in Fig. 5. The gain variation range is 26 dB.

The LNA output spectrum for a 10- μ V input signal is depicted in Fig. 6. One can distinguish the required signal at 162 kHz, a spurious component at the Local-Oscillator frequency (163.84 kHz), and a noise floor. This noise is equivalent to a 50nV/ $\sqrt{\text{Hz}}$ input noise density.

The Continuous-Time filters are OTA-C filters, realized with transconductors as described in [2]. The bias current for each transconductor input transistor is 50 nA. The Variable Gain Amplifiers (VGA) are also realized with transconductors, as shown in Fig. 7. Each VGA

contains a cascade of four gain stages. By varying the bias currents of the input transconductors in each stage, the gain can be varied [4]. At the output of each gain stage, the signal DC-component is short-circuited by an inductor. This prevents the amplification of offset voltages. The inductors are synthesized as a gyrator and a capacitor. The resulting VGA gain variation is depicted in Fig. 8. This Figure shows a gain variation of 52 dB. Therefore, the total AGC dynamic range is 78 dB.

Figure 8. allows also to estimate the receiver selectivity: spurious signals due to other AM transmitters are at least 9 kHz separated from the 162-kHz input frequency. After mixing with the first local oscillator, the spurious-signal frequency is larger than 7.16 kHz. At this frequency, the lowpass-filter attenuation is better than 70 dB.

The bandpass filter (BPF) is a small Second-Order filter, mainly intended to limit the input noise bandwidth. Its characteristic is shown in Fig. 9. The -3dB-bandwidth is 150 Hz.

In Figure 10, the spectrum at the comparator input is shown for a 100 mVpp antenna signal. The noise floor in this Figure includes the noise generated by the Local-Oscillator PLL. Therefore, this Figure allows to estimate the spectral purity of the PLL1.

In order to evaluate the receiver linearity, the «Third Order Intermodulation Intercept Point (IP3)» is measured (see Fig. 11): Two input signals with amplitudes of 100mVpp each and frequencies equal to 161.995 kHz and 162.005 kHz respectively are applied to the antenna input. As can be seen in Fig. 11, the intermodulation products are 50 dB below the fundamental signals. This implies that the IP3 equals 630 mVrms.

Most of the digital circuits are implemented as a datapath with a full-custom layout.

The radio receiver characteristics are summarized in Table 1.

IV. Acknowledgments

Mr. X. Saboret (MISIL Design, Rungis, F) is acknowledged for the Vitterbi decoder design. Mr. M. Miodini, Mr. R. Moughabghab and Mr. O. Declerck are acknowledged for the filter designs and for the SPICE simulations. We thank Mr. J-C Delefosse for the careful layout.

V. References

- [1] European Norm « NF C 90-002 », August 1988
- [2] F. Krummenacher, N. Joehl: « A 4-MHz CMOS Continuous-Time Filter with On-Chip automatic Tuning », IEEE J. Solid-State Circuits, June 1988
- [3] R. Best, « Phase-Locked Loops », McGraw Hill
- [4] European Patent Nr. 94 2856, MS2, France

Supply Voltage	2.2 ... 4.5 Volt
Supply Current in Stand-by	< 1 μ A
Power-Up Supply Current	< 150 μ A
Antenna input impedance	> 1 M Ω
Sensitivity	10 μ V ... 100mV
IF Bandwidth	150 Hz
Blocking Immunity (1)	> 50 dB
IP3	630 mV
Startup Time	< 20 sec.

(1) $\Delta f > 9$ kHz

Table 1: The major ASIC Characteristics

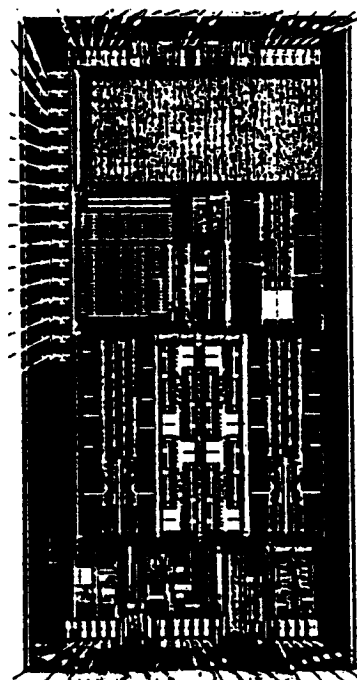


Fig. 3. A chip microphotograph

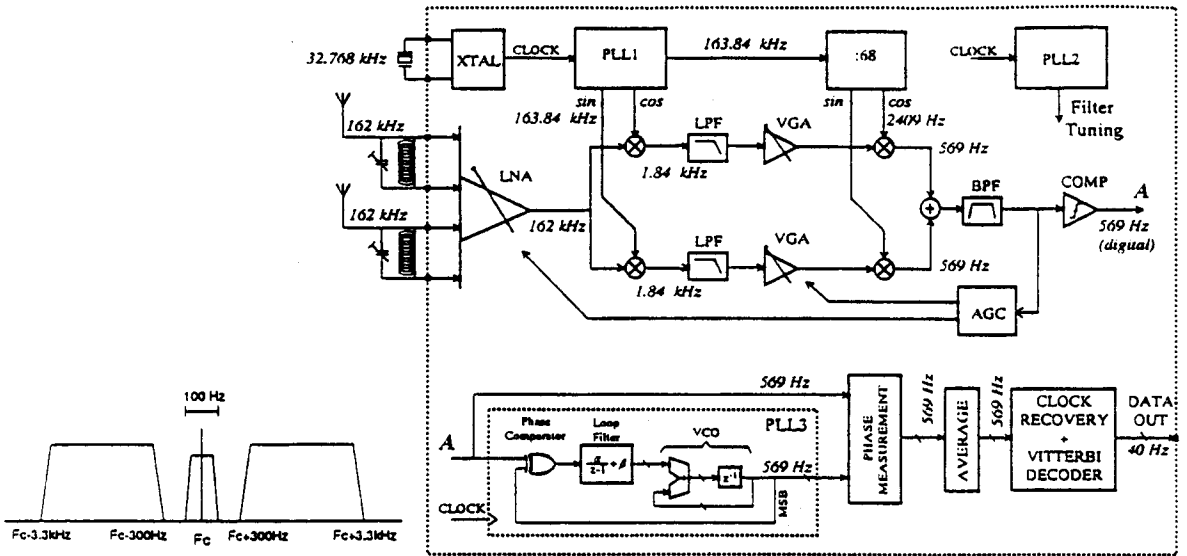


Fig. 1: The transmitter signal Spectrum

Fig. 2: The ASIC block schematic

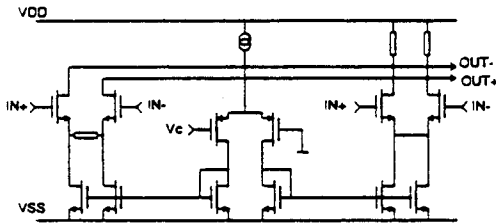


Fig. 4: The LNA schematic

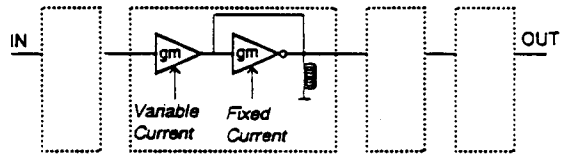


Fig. 7: The VGA Principle schematic

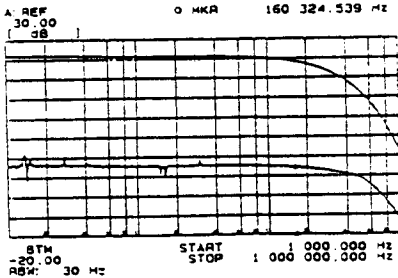
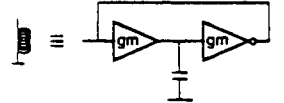


Fig. 5: The LNA Gain

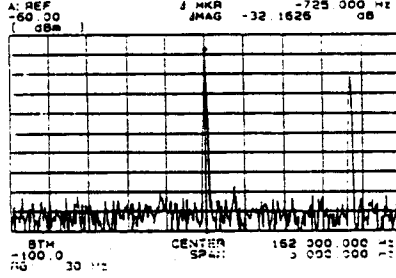


Fig. 6: The LNA Output Spectrum

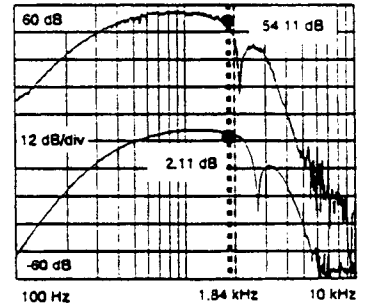


Fig. 8: The LPF+VGA Gain

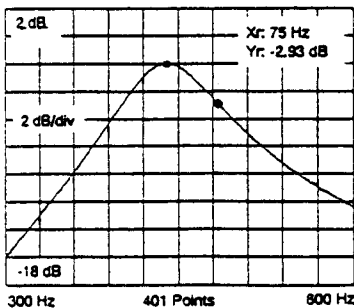


Fig. 9: The Bandpass Filter Characteristic

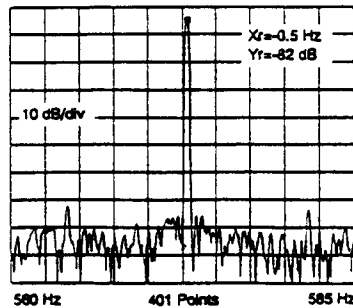


Fig. 10: The Comparator Input Spectrum

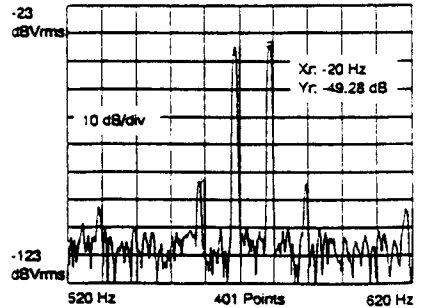


Fig. 11: The IP3 Measurement Both input signals 100mVpp