

A Generic CAD Model for Arbitrarily Shaped and Multi-Layer Integrated Inductors on Silicon Substrates

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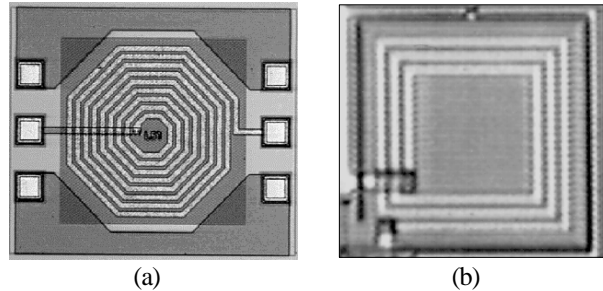
Abstract

A generic and process-independent lumped element model for simulating the performance of arbitrarily shaped and multi-layer inductors on silicon substrates is presented. Integrated inductors are modeled using an equivalent two-port network for each segment of the spiral. An algorithm that extracts the complete circuit is presented in detail. Element value calculation is based on microstrip line properties, considering magnetic and capacitive coupling, substrate losses, conductor skin effect and image current on the ground plane. Octagonal, square and two-layer integrated spiral inductors were designed and fabricated using three different processes. Measurement results confirm the accuracy of the model.

1. Introduction

Modern wireless communication systems increasingly demand low power and low cost circuits along with a high level of integration. The extensive use of on-chip inductors can be advantageous with respect to noise performance and contribute to a higher level of integration in silicon RF IC design. Towards this target, attempts have been made to evaluate the performance of inductors on silicon substrates and lumped element models have been presented. Recently [2], the results of a critical work on square-shaped spiral inductor modeling were reported and compared to measurement results. Also, in [3] an effective lumped element model for integrated spiral inductors is presented. However, no algorithm for creating a generic circuit model that describes the behavior of integrated inductors over a wide frequency range has been reported yet. Moreover, most efforts have been concentrated on planar and square-shaped spirals. In this paper, we present step by step an efficient algorithm that implements a precise lumped element model for monolithic inductors on silicon substrates. The model is generic in terms of geometry and technology; arbitrarily shaped polygonal inductors on one, or more, metal layers implemented in CMOS, bipolar or BiCMOS technologies can be accurately simulated. Furthermore, the model is valid from a few megahertz up to several gigahertz, usually beyond self-resonance frequency. Detailed analysis and equations chosen after thorough evaluation of the bibliography are presented.

Based on our algorithm, a compact computer program along with its graphical user interface has been developed as a CAD tool for RF IC design. The designer can enter any polygonal inductor shape, and the program generates the SPICE circuit model, extracts the values for its parameters and presents the simulation results. It can also model the coupling between two or more adjacent inductors and create a subcircuit for the equivalent n -port network. The accuracy of our program is established through comparisons between measurement and simulation results for various inductor structures fabricated in three different Si technologies. For both octagonal and square spiral inductors, our modeling technique exhibits a better than 5% accuracy in the prediction of the inductance and quality factor. A comparison between square and octagonal inductors occupying the same silicon area is also performed in this paper. Moreover, two-layer square spiral inductors have been designed and the simulation results of the model demonstrate area downsizing and inductance multiplication by a factor of five.



(a) 8.5-turn octagonal (b) 3-turn square
Fig. 1. Inductor microphotographs:

2. Inductor Model Lumped Element Approach

Each segment of the inductor is modeled with a two-port network consisting of lumped elements, as shown in Fig. 2(a). Two coupled microstrips in a typical silicon process are drawn in Fig. 2(b). The geometry characteristics of interest are the track width w of the spiral, the distance between two adjacent parallel tracks s and the height of the metal track t . The height of the Si substrate and the SiO₂ insulator are h_{Si} and h_{SiO_2} respectively. The main elements of the two-port are the series inductance L , the resistance R of the segment and the capacitors C_p formed by the insulating SiO₂ between the inductor and the Si substrate. All equations referred to hereinafter are listed in Table 1. L is calculated by (1), while R is given by (2); R_{sh} is the sheet resistance of the metal track. All lengths are in cm , while inductance is given in nH . C_p is given by (3).

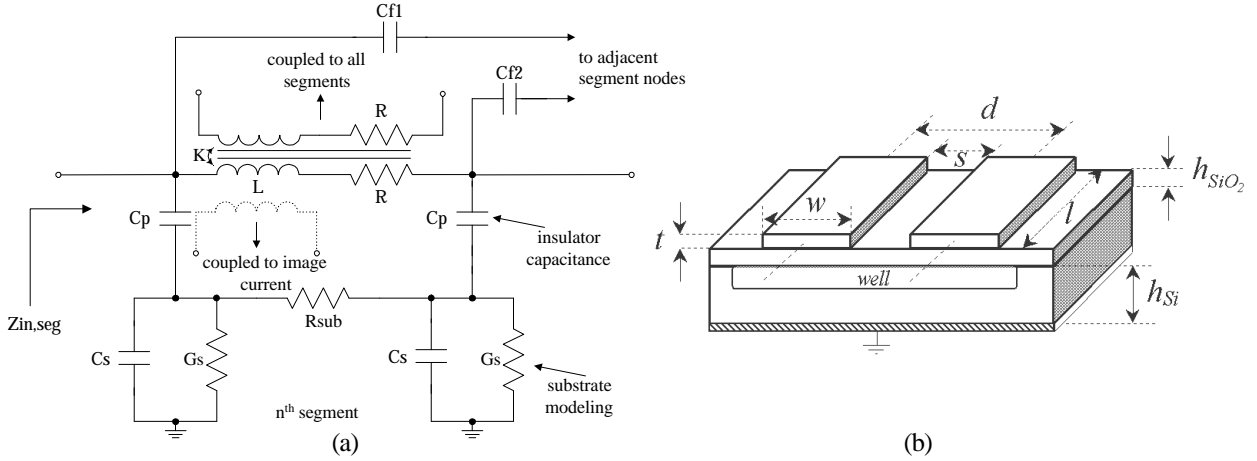


Fig. 2. (a) Equivalent two-port for one segment of the spiral inductor.
(b) Parallel coupled spiral segments over Si substrate

The mutual inductance among the segments of the spiral plays an important role to the computation of the total inductance. The mutual inductance M between two segments of the inductor is modeled with a transformer. The complete circuit of the spiral inductor contains a transformer for every possible couple of segments. The magnetic coupling coefficient K of these transformers is given by (5), where L_1 and L_2 are the inductance values of the two segments that form the transformer.

Table 1. Equations of the proposed generic model

	Equation	Reference
$L = 2l \{ \ln[2l / (w+t)] + 0.50049 + (w+t) / 3l \}$	(1)	[1]
$R = R_{sh} l / w$	(2)	
$C_p = \epsilon_0 \epsilon_r w / h$	(3)	
$M = 2IU$	(4)	[1]
$K_m = M_{1,2} / \sqrt{L_1 L_2}$	(5)	
$2M = (M_{l+m \pm d} + M_d) - (M_{l \pm d} + M_{m \pm d})$	(6)	[1]
$2M = (M_{m+p} + M_{m+q}) - (M_p + M_q)$	(7)	[1]
$M_{lm} = 2 \cos f \left[l \tanh^{-1} \left(\frac{m}{l+y} \right) + m \tanh^{-1} \left(\frac{l}{m+y} \right) \right]$	(8)	[1]
$M_{lm} = 2 \cos f \left[(M_{m+l/n+m} + M_{mn}) - (M_{m+l/n} + M_{n+m,m}) - W d_z / \sin f \right]$	(9)	[1]
$W = \frac{p}{2} + \tan^{-1} \left[\frac{d_z^2 \cos f + lm \sin^2 f}{d_z R_l \sin f} \right] - \tan^{-1} \left(\frac{d_z \cos f}{l \sin f} \right) - \tan^{-1} \left(\frac{d_z \cos f}{m \sin f} \right)$	(10)	[1]
$R_{sub} = r_{Si} l / (wh_{Si})$	(11)	
$C_s = \frac{(w+Dw')}{h} \epsilon_0 \epsilon_{r,Si}$, $Dw' = \left(I + \frac{l}{\epsilon_{r,Si}} \right) \frac{Dw}{2}$, $Dw = \frac{t}{p} \ln \left[4e / \sqrt{\left(\frac{t}{h} \right)^2 + \left(\frac{l/p}{w/t+1.1} \right)^2} \right]$	(12)	[5]
$G_s = s \frac{w}{h}$, $s = s \left(\frac{l}{2} + \frac{l}{2\sqrt{1+10h/w}} \right)$, $h = \frac{w}{2p} \log \left(\frac{8h}{w} + \frac{4w}{h} \right)$	(13)	[6]

During this step, the algorithm examines the relative position of every pair of segments and calculates K . Considering segments as simple filaments, the possible configurations in space are illustrated in Fig. 3. Two different cases are distinguished here: i) the segments are parallel (Figs. 3(a) and 3(b)) and ii) the segments are at an angle of j radians (Figs. 3(c)-(f)). The mutual inductance of two parallel segments of equal length l , forming an orthogonal rectangle, is given by (4). All other configurations of parallel segments are based on this equation. Attention should be paid to the U factor in (4). U is calculated using closed-form expressions provided by Grover in [1], and concerns the various cases of the geometric mean distance (GMD) between two conductors of width w and height t , separated by d cm. If the segments are parallel, two distinct cases may appear. The first is shown in Fig. 3(a) and the mutual inductance is calculated by (6), where d is positive for non-overlapping segments and negative for overlapping ones. In the second (Fig. 3(b)) the mutual inductance M_{lm} between the two conductors with lengths l and m is calculated by (7).

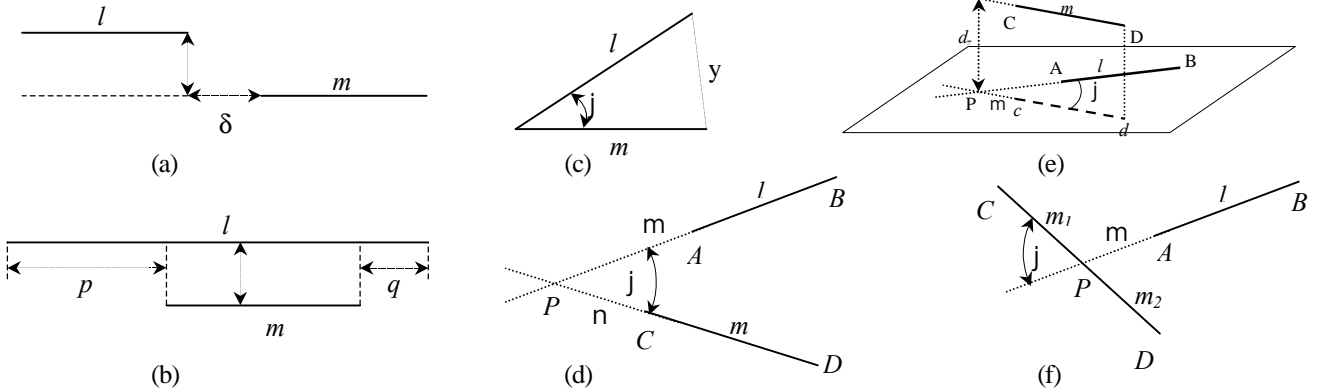


Fig. 3. Magnetically coupled segments in special configurations

If the two segments are at an angle (Fig. 3(c)), their mutual inductance is calculated by (8). This general form is employed in the calculation of M in Figs. 3(d)-3(f). In Fig. 3(d) the intersection point P is lying outside the two filaments and M is computed by (9). W applies only in the case of non-planar segments (Fig. 3(e)) and is given by (10). The most complex case is the one depicted in Fig. 3(f) where the intersection point P lies upon one segment. This case is examined by partition as follows: Segment CD is divided in CP and PD . Total M is calculated as the sum of M_1 and M_2 . M_1 is the mutual inductance of segments CP and AB while M_2 is that of PD and AB . Both M_1 and M_2 are calculated as for Fig. 3(d). Mutual inductance computation between inductor segments and image currents on the ground plane under the semiconductor is also incorporated in a similar manner.

The coupling capacitances between parallel adjacent segments are calculated as proposed in [4] with closed-form expressions. The computation of the two elements modeling the substrate layers under the insulator is based on (12) for C_s , and on (13) for G_s . A comprehensive study presented in [6] addresses the calculation of the conductivity per unit length G_s and leads to (13), where S is the conductivity of the substrate that behaves as a lossy semiconducting material. If a layer exists under the inductor, i.e. n-well in a CMOS process, it is modeled with an extra C_s , G_s branch computed also by (12), (13) and connected in series with the C_s , G_s branch. Finally, the substrate resistance R_{sub} is computed by (11). The skin effect formulation for both L and R employed in our algorithm is based on the closed-form expressions presented in [4].

3. Experimental Results

a) Fabricated Integrated Inductor Structures

Inductor structures in three different silicon processes have been fabricated and measured. Specifically, SIEMENS' B6HF bipolar process was used for the design and fabrication of square spirals, SGS-THOMSON's HSB bipolar process for octagonal spirals, and ATMEL-ES2's ECAT05 CMOS process for two-layer structures. A two-layer inductor is formed by two planar inductors one exactly over the other as illustrated in Fig. 4.

A comparison between measurement and simulation results for a square and an octagonal spiral is shown in Fig. 5. The presentation is organized as follows: for each inductor, the $L = \text{Im}(1/Y_{11})/2\pi f$ and $Q = \text{Im}(1/Y_{11})/\text{Re}(1/Y_{11})$ values are shown versus frequency. Each plot contains the simulation and measurement curves for both Q and L . The simulation model

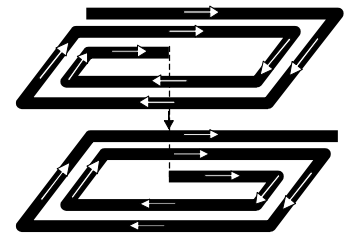


Fig. 4. Two-metal layer inductor structure

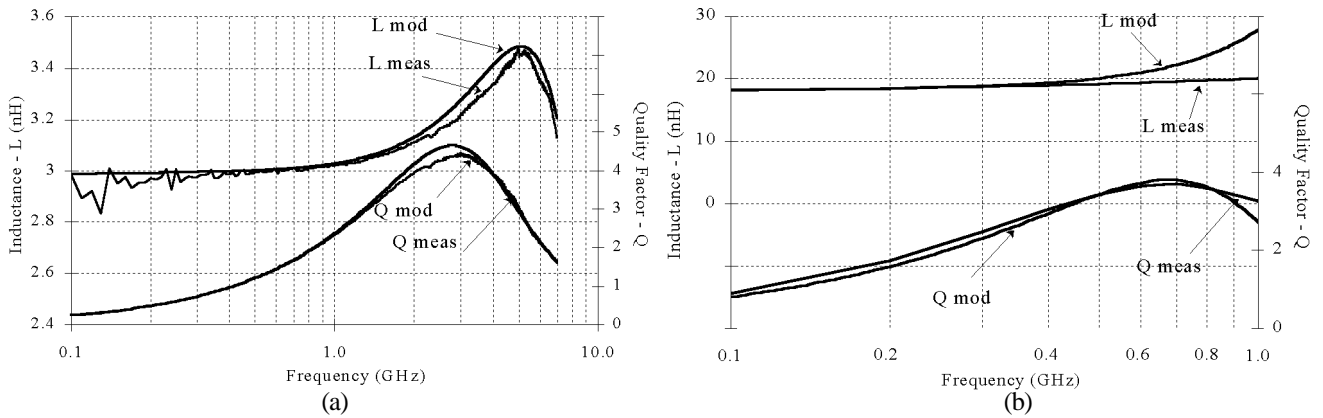


Fig. 5. Experimental results of (a) 3-turn square spiral inductor and (b) 8.5-turn octagonal spiral inductor

is extracted from typical technology parameters; “fast” and “slow” simulation results were derived from a worst case combination of technology parameters’ deviation (not shown in Fig. 5). The discrepancy between measurement and simulation results is between 1-5% in the bandwidth of interest. The L and Q of a 3-turn square (Fig. 1(b)) spiral with an outer dimension of $245.5 \mu\text{m}$, $w=12.5 \mu\text{m}$ and $s=5 \mu\text{m}$ are plotted in Fig. 5(a). In Fig. 5(b) the results of an 8.5-turn octagonal spiral (Fig. 1(a)) with radius $r=250 \mu\text{m}$, $w=16 \mu\text{m}$ and $s=8 \mu\text{m}$ are shown.

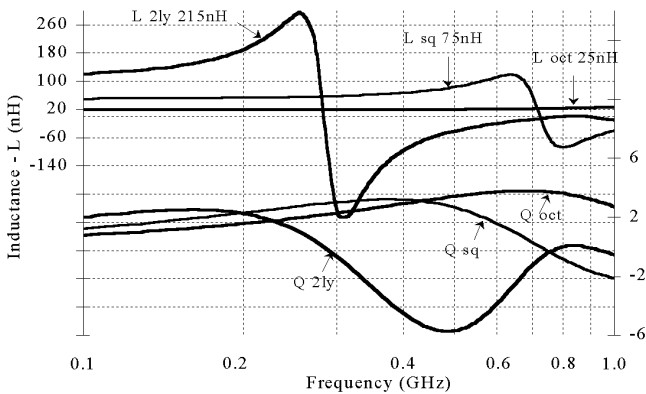


Fig. 6. Comparison between octagonal, square and two-layer inductors occupying the same silicon area

b) Comparison between different structures

Thanks to its flexibility and accuracy, our algorithm is especially useful for comparing alternatives during design optimization. As an example, Fig. 6 shows a comparison between square, octagonal and two-layer spirals of 8.5 turns, occupying the same silicon area, with $w=16 \mu\text{m}$, and $s=3 \mu\text{m}$. As before, results are presented in terms of L and Q . This comparison reveals that, for the parameters

chosen, there is a real advantage in choosing an octagonal geometry whenever a significant Q value over a wider frequency range is required, and the two-layer geometry when high inductance value is the target.

4. Conclusions

A generic and process-independent algorithm for the evaluation of any integrated inductor structure over silicon substrates was presented in detail. Comparison between simulated and experimental results from different silicon processes proved the accuracy and efficiency of the proposed technique within 5%. A two-metal layer inductor structure was also presented and modeled, exhibiting high inductance values at low frequencies.

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5. References

- [1] F. W. Grover, “Inductance Calculations”, *Van Nostrand, Princeton N.J.*, 1946, *Dover Publications*, 1962.
- [2] J. R. Long, M. A. Copeland, “The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC’s”, *IEEE JSSC*, vol. 32, pp. 357-369, Mar. 1997.
- [3] J. Crols, P. Kinget, J. Craninckx, M. Steyaert, “An Analytical Model of Planar Inductors on Lowly Doped Silicon Substrates for High Frequency Analog Design up to 3GHz,” *Proc. VLSI Circuits Symposium*, June 1996.
- [4] E. Pettepaul, et al., “CAD Models of Lumped Elements on GaAs up to 18 GHz”, *IEEE Trans. on MTT*, vol. 36, pp. 294-304, Feb. 1988.
- [5] H. A. Wheeler, “Transmission-Line Properties of a Strip on a Dielectric Sheet on a Plane”, *IEEE Trans. on MTT*, vol. 25, pp. 631-647, Aug. 1977.
- [6] H. Hasegawa, M. Furukawa, H. Yanai, “Properties of Microstrip Line on Si-SiO₂ System”, *IEEE Trans. on MTT*, vol. 19, pp. 869-881, Nov. 1971.
- [7] R. Garg, I. J. Bahl, “Characteristics of Coupled Microstriplines”, *IEEE Trans. on MTT*, vol. 27, pp. 700-705, July 1979.