

An IF-Strip with Integrated 2nd IF Filter for a Triple Conversion GPS Receiver.

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Abstract: An IF-strip for a low power, triple conversion GPS receiver has been designed in a 1.0 μm BiCMOS technology. The IC comprises a 179 MHz 1st IF amplifier and mixer, a 4.7 MHz 2nd IF with on chip RC active filter and some base-band support circuitry. A total gain of 84.7 dB and a noise figure of 8.8 dB have been achieved, with a current consumption of about 1.8 mA.

1 Introduction

The GPS is a radio navigation system using 24 satellites, which are located at height of 20200 km. Each satellite sends the UTC and its own position on two frequencies (L1 and L2) using a spread spectrum CDMA technique. A receiver can calculate its own position and speed using the data coming from any 4 satellites and the delays required in the correlators to correlate the signals of these satellites. The two frequencies are derived from a 10.23 MHz atomic clock. The frequency of L1, for civilian use, is 1575.42 MHz (154 times the atomic clock) and that of L2, for military use, is 1227.6 MHz (120 times the atomic clock) [1].

During the last few years, there is growing interest in the GPS system, not only among professional and military users, but also in the consumer area. Potential applications in the latter field may range from positioning and navigation for cars and boats to mountaineers, leisure hiking, and precise world-wide time reference for watches. In order to fulfill the requirements of the consumer market, low power, low cost integrated GPS receivers are highly desirable.

Although complete single-chip GPS receivers have become widely available [2], these receivers are usually targeted towards high performance and relatively big hand-held or fixed (e.g. on a car or ship) applications, where the power consumption and the number and size of external components are less a problem. We have developed a highly integrated GPS receiver for the civilian L1 band, targeting towards miniaturized, cost sensitive consumer applications. The receiver's RF front-end was reported recently [3]. In this paper we report the IF-strip.

2 Receiver Architecture

The underlying idea of the triple conversion architecture, shown in fig. 1, is to minimize the number of components working at the highest frequency, thus minimizing power. A highly integrated IF strip plays an important role in keeping the number of external components down.

The 1.57 GHz GPS signal is received from an active patch antenna and filtered with a SAW filter to remove signals at the image frequency and other strong out-of-band signals which may

overload the RF front-end. This front-end comprises an LNA, an LC oscillator, a single balanced mixer and a prescaler.

The 1st IF signal is then routed to an off-chip 179 MHz SAW filter where channel filtering occurs. This signal is then amplified and down-converted to the 4.7 MHz 2nd IF with a double balanced mixer. Since the required performance of the 2nd IF filter is quite modest, the latter can be fully integrated on chip. The biggest advantage of integrating the 2nd IF filter is the reduction of the complexity of the receiver to a level comparable to a single superhet one, thus saving an external filter. After amplification and amplitude limiting, the 2nd IF signal is converted to digital with a 1 bit ADC. Sampling at 3.6 MHz, the ADC also down converts the 2nd IF signal to the 3rd IF of 1.05 MHz. Detection and decoding of the GPS signal is then performed by a CMOS chip, which contains all the digital processing parts of the receiver and which is not part of this work.

3 The IF-Strip

The IF-strip reported here includes the parts to the right of the dashed line in fig. 1. The schematic diagram of the 1st IF mixer, preceded by a preamplifier, is shown in fig 3. The required gain of the amplifier was 12 dB, which can be easily obtained with a single transistor. A single-stage common base amplifier has thus been chosen. This transistor also generates the bias voltage for the mixer. The mixer is a double balanced Gilbert-cell type, that is required here to achieve a high local oscillator rejection, to avoid overloading the active 2nd IF filter. The output of this mixer is connected to a transimpedance active load which also implements the real pole of the 2nd IF filter. The current consumption of the amplifier and the mixer is $80 \mu\text{A}$ each.

The 2nd IF filter is a 5th order low-pass Butterworth active RC filter, with a cut-off frequency of 6.6 MHz. Its schematic diagram appears in fig. 2. AC interstage coupling has been used to remove offset and low frequency signals, resulting in the filter's characteristic being bandpass. A fully differential structure has been used to minimize the pick-up of substrate noise and the potential instability due to parasitic feedback. Figure 4 shows the schematic diagram of the opamp used in this filter. It is a single stage differential amplifier with emitter-follower output buffers. This simple structure fits best the requirements of wide bandwidth, low output impedance and low power consumption. Indeed the simulated gain-bandwidth product is 350 MHz with a current consumption of $140 \mu\text{A}$. The 2nd IF strip is completed with 3 differential limiting amplifiers, to obtain an overall gain (1st IF input to 2nd IF output) of 85 dB. The signal is then converted to digital with a latched comparator.

A frequency synthesizer, consisting of a chain of dividers, a phase comparator and an amplitude-regulated crystal oscillator, completes the chip. The divider-by-8 is implemented with differential current mode CMOS logic (ESCL) while the rest uses standard CMOS logic.

4 Measured Performance

The measurements have been performed on unpackaged chips, bonded to a small PCB, which contains all the necessary external components. The die photo is shown in fig. 5. The supply voltage has been set to 3 V.

The overall voltage gain of the IF-strip is 84.7 dB, which agrees very well with the calculated 85 dB. Fig. 6 shows the measured frequency response of the 2nd IF filter (dashed), together with the simulated one (solid). Again a very good agreement has been observed. The noise figure is 8.8 dB referred to 500Ω , and the limiting voltage is +6 dBm. The amplitude of the

crystal oscillator is $1.1 V_{pp}$ at the nominal supply of 3 V. This corresponds to a driving power of 25 - 50 μW , depending on crystal characteristics. When the supply voltage is varied from 2 V to 5 V, the oscillation amplitude only varies from $1.045 V_{pp}$ to $1.122 V_{pp}$. The minimum operating voltage of the chip is 2.0 V. Table 1 summarizes the key performances of the chip.

5 Conclusions

A low power IF-strip for a triple conversion GPS receiver targeted towards low power, low cost consumer applications has been designed. The key parameters were very low power and reduced complexity rather than high performance, to allow the construction of miniaturized GPS receivers that will fit in a watch. The number of external components has been minimized, especially by the integration of the 2nd IF filter, while the use of a relatively high 1st IF allows the use of a small size SAW filter. The current consumption is kept as low as 1.8 mA, while the complete GPS receiver, using the chip in [3] as RF front-end, will consume only about 12 mA. Despite the low power consumption, a performance comparable to that of typical commercial chips [2] has been obtained.

References

- [1] E. D. Kaplan, *Understanding GPS, Principles and Applications*, Artech House Publishers, Boston, London, 1996;
- [2] Datasheets from GEC Plessey (*GP1010, GP2010*), Sony (*CXA1951Q*), NEC (*UPB1004GS*), Philips (*SA1570*) and Rockwell.
- [3] F. Piazza, Q. Huang, *A 12 mA Triple-Conversion Receiver for GPS*, ISSCC Digest of Technical Papers, pp. 286-287, Feb. 1996, San Francisco, USA;

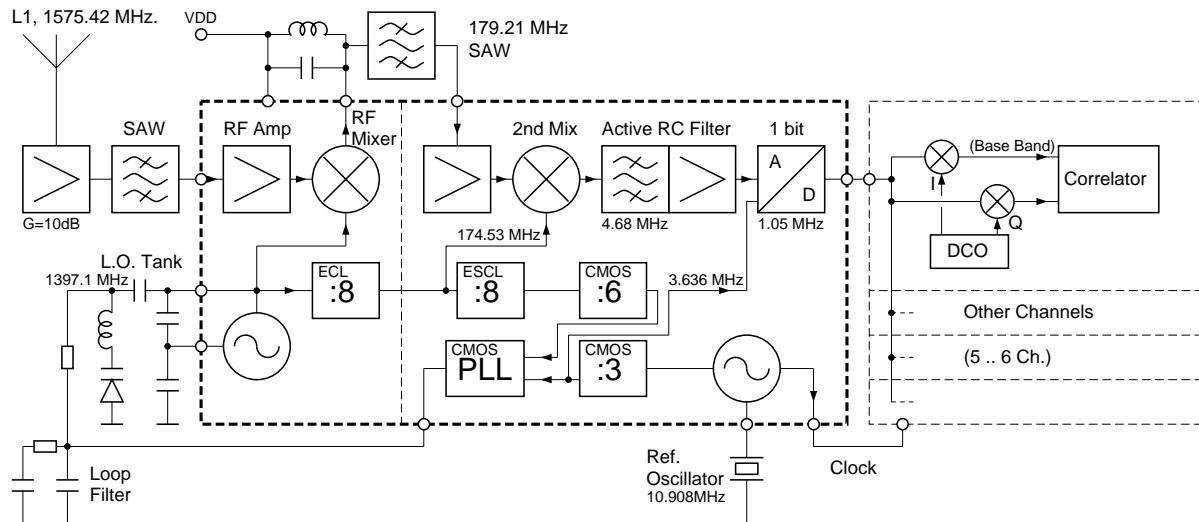


Figure 1: Block diagram of the complete GPS receiver.

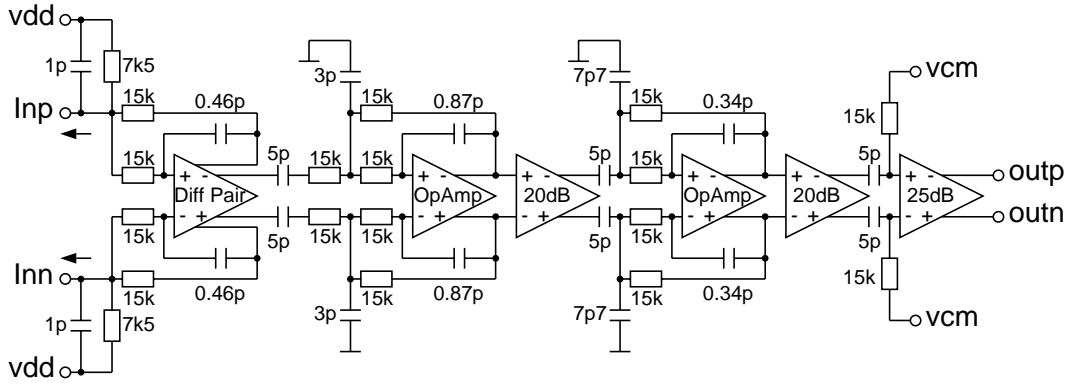


Figure 2: Schematic diagram of the 2nd IF filter.

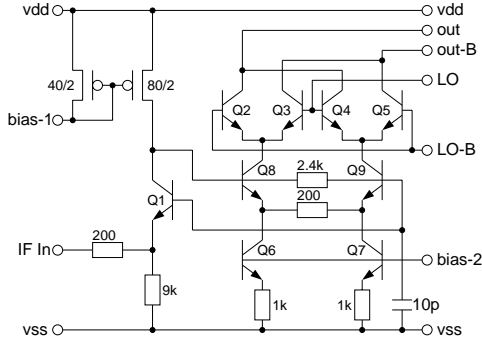


Figure 3: 1st IF mixer with preamp.

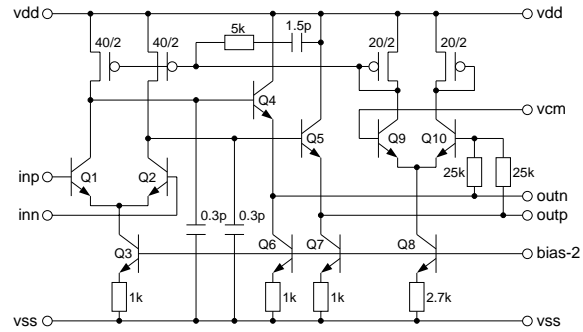


Figure 4: Opamp for the active IF filter.

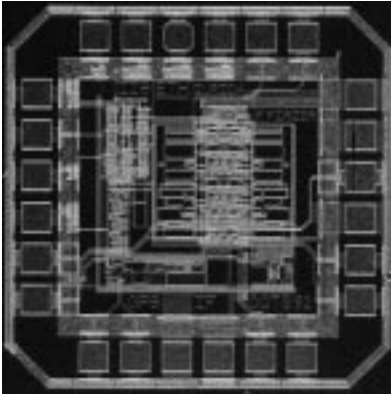


Figure 5: Chip photograph.

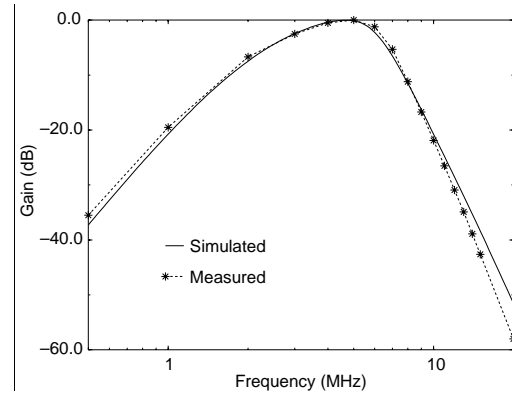


Figure 6: Frequency response of the filter.

Process	1.0 μm BiCMOS
Chip size	1404 μm x 1404 μm
Overall gain	84.7 dB
Limiting level	6 dBm
filter characteristic	B5, -3 dB at 6.6 MHz
Input impedance	500 Ω
Noise figure (500 Ω)	8.8 dB
Xtal osc. amplitude	1.1 V _{pp}
Supply voltage	2.0 - 5.0 V
Supply current	1.81 mA at 3 V

Table 1: Measured IF-strip characteristics.