

# **A novel driver architecture capable of driving high capacitive loads for sub-half micron technologies**

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## ***Abstract***

*The purpose of this paper is to present a new CMOS compatible driver which overcomes certain limitations of the conventional CMOS circuits. The proposed driver has very low fan-in (about 50% reduction) and, as it will be demonstrated, is very efficient for high capacitive loads. These benefits are obtained without any excess of power dissipation compared to the standard CMOS solution. It will also be shown that this basic architecture is applicable to BiCMOS technology. The operation of the proposed drivers is attributed to a Deep Depletion Condition phenomenon, present in sub-half micron CMOS/BiCMOS technologies, for input pulses with fast rise times.*

## **1. Introduction**

The challenge in sub-half micron technologies is to design fast drivers capable of driving large capacitive loads (e.g. clock drivers, bus drivers, etc.), while maintaining Si area and power consumption as small as possible. The experience which has been gained over several technology generations suggests that for high capacitive loads CMOS drivers exhibit lower performance than BiCMOS and NMOS drivers [1,2]. Indeed, the BiCMOS drivers preserve the low power characteristics of a CMOS architecture, while taking advantage of the high current driving capability of BJTs. The disadvantage of the BiCMOS solution is the additional fabrication cost and the lack of rail-to-rail swing at the output node. Likewise, the NMOS solution suffers from static power dissipation and the high output voltage has a  $V_{th}$  drop from  $V_{dd}$ . These drawbacks of NMOS circuits cannot be compensated by their beneficially high speed with respect to CMOS structures.

The above discussion points the necessity of a new CMOS driver architecture, which should exhibit the following advantages compared to the conventional designs: a) higher efficiency for high output capacitive loads (i.e. reduced delay, rise and fall time), b) lower fan-in and c) similar power dissipation. The purpose of this paper is to present new CMOS/BiCMOS driver architectures which fulfill the previous requirements. This is achieved by taking advantage of a Deep Depletion Condition phenomenon in the source of an n-channel MOSFET, present in sub-half micron CMOS/BiCMOS technologies for very fast pulses. The simulated results presented hereinafter have been obtained with ST-SPICE for well defined 0.5 $\mu$ m CMOS and BiCMOS processes, developed by SGS-Thomson Micr. Similar results have been obtained for the 0.35 $\mu$ m CMOS/BiCMOS technology.

## 2. Driver Architectures, Operation and Simulation Results

Fig. 1.a shows the new driver along with the conventional one (Fig. 1.b)[3]. For comparison purposes, the geometry of the output devices is identical in both cases. Fig. 1 shows that the pull-down is the same for both circuits, while this is not the case for the pull-up. Indeed, the new driver has an n-channel MOSFET as a pull-up device (M5; Fig. 1.a), which is driven by M3 (Fig. 1.a), which in turn is controlled by an inverter (M1 and M2; Fig. 1.a). It has to be underlined that the substrates of M3 and M5 are floating. Let us now consider the case where the previous input signal was high (i.e. the voltage at the load capacitance is 0V as well as at the node V2) and that the new input signal is low. In such a situation the devices M4 and M6 are off and the voltage at V1 becomes Vdd. One should expect that the voltage at V2 will be Vdd-Vth. This is not the case as indicated in Fig. 2, where the voltage at V2 attains the value Vdd+1.1V.

This paradoxical operation is not only related to a boot-strapping mechanism. Provided that nowadays technologies make use of shallow junctions and retrograde wells (i.e. abrupt doping profiles), 2D device hydrodynamic simulations have shown that this behavior is due to a Deep Depletion Condition (DDC). More precisely, if a very fast pulse is applied at the gate of M3, the charge which suddenly arrives at the source of M3 forces the underlying diodes in DDC [4]. In this case and in order to conserve the injected charge, the overall capacitance at the source of M3 decreases and as a result the voltage at V2 increases above Vdd (see Fig. 2). This behavior can be observed in advanced processes (due to the above mentioned technological issues) and only for pulses with fast rise times. Indeed, the DDC is related to the timing of the input pulses and the doping profile at the source and drain regions. This is further demonstrated in Fig. 3 where the rise time of the output pulses is plotted versus the slope of the input pulses. The dependence of V2 on the slope of the input pulses is also reported in the insert. Consistently with the physics of semiconductor devices [4], these data suggest that this phenomenon occurs only for fast input slopes. Obviously, the voltage value at V2 influences substantially the overall performance of the driver (see Fig. 3).

At this point several issues have to be clarified. The substrate of M3 (see Fig. 1.a) is floating in order to allow the voltage of the substrate to follow the voltage applied at the gate of M3. The substrate of M5 is also floating in order to minimize the capacitance seen by the gate of M5 when it is operated in strong inversion regime. For charge sharing purposes the capacitance at the source of M3 should be much less than the gate capacitance of M5, while at the same time M3 should be sufficiently large to drive M5. Obviously, such a requirement makes the design critical and for our technology, parametric simulations have shown that the optimum performance is obtained if M5 is about three times larger than M3. Finally, the maximum voltage value at V2 has to be properly adjusted in order to avoid reliability hazards (i.e. hot hole injection, trapping, etc.).

The CMOS compatible version of the new and the conventional drivers are being compared in terms of performance in Fig. 4. Consistently with the previous discussion the proposed circuit introduces significant improvement for high capacitive loads without excess of power dissipation (see Fig. 5). Obviously, these characteristics make the new driver architecture very attractive for several applications.

In Fig. 6 a similar full-swing BiCMOS driver is presented and compared to the full-swing BFBiCMOS driver presented by Bellaouar et al. [5] (by keeping the same fan-in). The results of the comparison in terms of delay time and power dissipation are illustrated in Fig. 7.

## 3. Conclusion

In conclusion, a new CMOS compatible driver has been presented which overcomes certain limitations of the conventional CMOS circuits. The proposed driver has very low fan-in (about 50% reduction) and, as it has been demonstrated is very efficient for high capacitive loads. These benefits are obtained without any excess of power dissipation compared to the standard CMOS

solution. It has also been shown that this basic architecture is applicable to BiCMOS technology. The operation of the proposed drivers has been attributed to a Deep Depletion Condition phenomenon, present in sub-half micron CMOS/BiCMOS technologies for input pulses with fast rise times.

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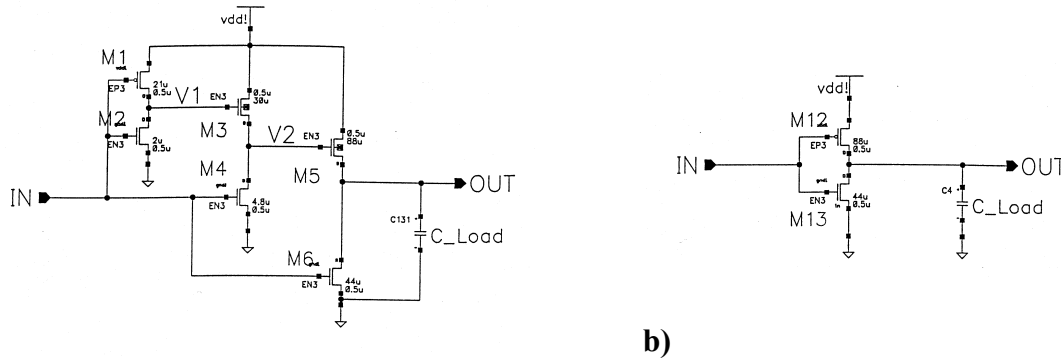


Fig 1. a) The proposed CMOS compatible driver. b) The conventional CMOS driver.

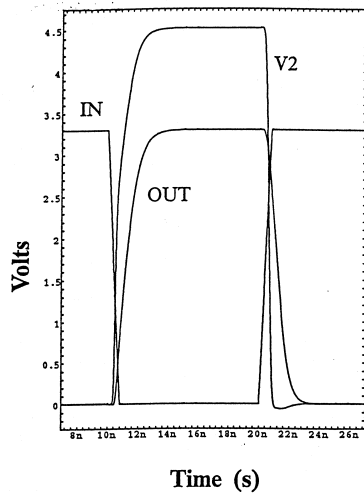


Figure 2. ST-SPICE voltage waveforms of the input voltage (IN), the output voltage (OUT) and the voltage at the gate of M5 (V2) for the driver of Fig. 1.a. (VDD=3.3V, Input slope=0.8ns and C\_Load=6pF.)

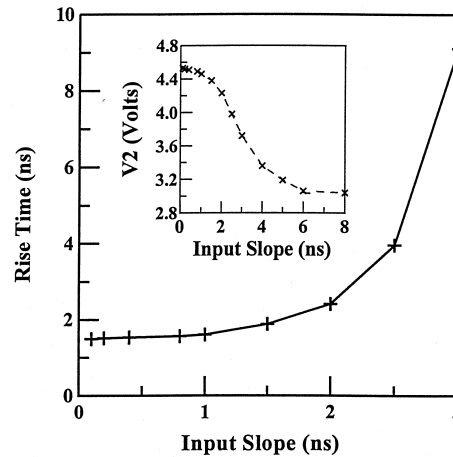
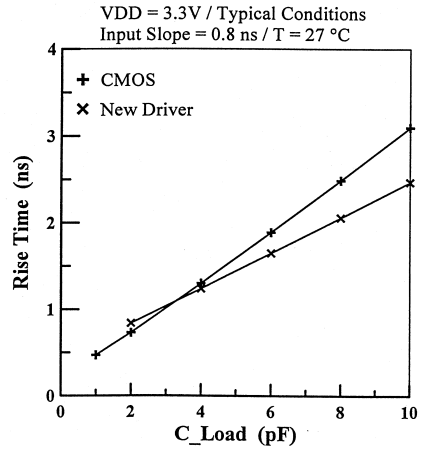
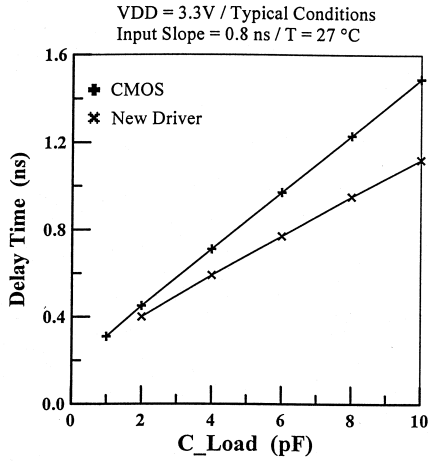
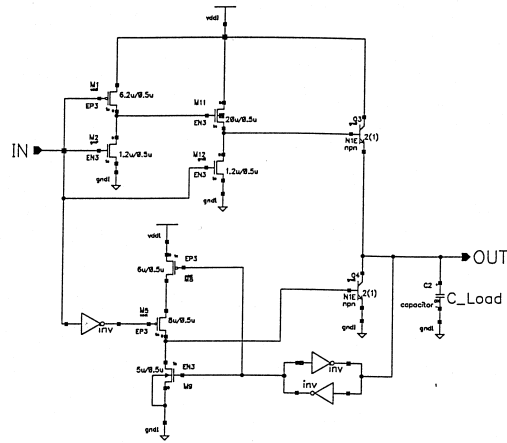
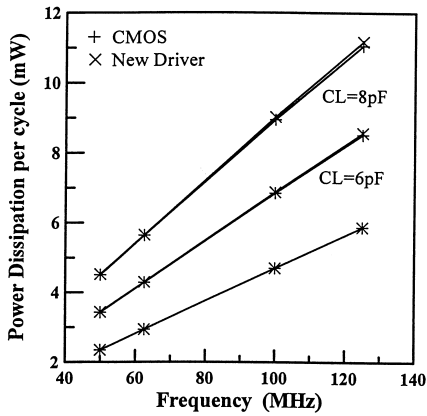


Figure 3. Rise time of the output pulses vs. the slope of the input pulses, for the driver of Fig. 1.a. In the insert, V2 vs. the slope of the input pulses. (VDD=3.3V, C\_Load=6pF.)

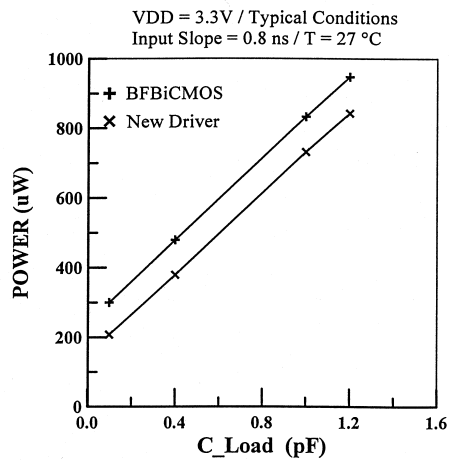
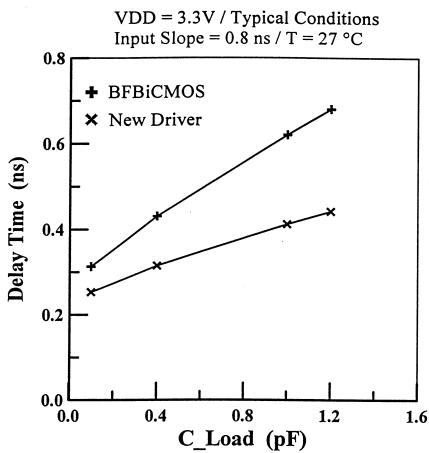


**Figure 4.** a) Output Delay time of the conventional CMOS driver and the new driver of Fig. 1.a vs. capacitive load. b) Output Rise time of the conventional CMOS driver and new driver of Fig. 1.a vs. capacitive load.



**Figure 5.** Power dissipation per cycle for the conventional CMOS driver and the new driver of Fig. 1.a vs. frequency, for different capacitive loads.

**Figure 6.** The proposed full-swing BiCMOS driver.



**Figure 7.** a) Output Delay time and b) Power dissipation per cycle for the BF-BiCMOS driver and the new BiCMOS driver of Fig. 6 vs. capacitive load. (Frequency = 50 MHz)