A 1V CMOS fully-differential switched-opamp bandpass ΣΔ modulator

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Abstract

A 2nd order bandpass ΣΔ modulator operating with a single 1V supply voltage has been realized within a standard (V_{THn}=0.65V, V_{THp}=0.7V) 0.5µm CMOS technology. In order to avoid the use of on-chip voltage multiplication, the circuit has been designed using the Switched-opamp technique. The use of proposed fully-differential structures has been exploited to increase dynamic range which is about 45dB in a 20kHz bandwidth

I. Introduction

The possibility of using bandpass ΣΔ modulator in the receiver demodulator channel has been demonstrated to be an efficiently alternative to standard solutions. On the other hand the demand of low-voltage low-power circuits for portable systems forces to develop solution for the bandpass ΣΔ modulators capable of operating at reduced supply voltage. In this paper the application of the improved version [3] of the switched-opamp technique [1] to ΣΔ modulator is given. This allows with respect to previous switched-opamp realization [2], to increase the sampling frequency and to increase internal integrators voltage swing (i.e. dynamic range).

In this work the basic building blocks necessary to realize a low-voltage bandpass ΣΔ modulator are proposed. The validity of the given structures is demonstrated by their application within a standard 2nd order bandpass ΣΔ modulator [4] able to operate at 1V supply with sampling frequency of 1.8MHz. Notice that, since it is based on the lowpass-to-bandpass transformation of a 1st order structure, it is expected to suffer with tonal behaviour just as the 1st order lowpass one does. Therefore the intention of this work is limited to present the potentiality of the switched-opamp technique without realizing a final commercial product.

II. Switched-opamp building blocks

In this section low-voltage circuit solutions for the blocks necessary to build ΣΔ modulators are given. They are: SC integrator, fully-differential opamps, comparator. They are based on the switched-opamp technique. It consists in eliminating the critical switches (which see the full signal swing) and in replacing their function by proper turning on and off the driving force of the opamps.

Fig. 1 shows the single-ended version of the switched-opamp SC integrator structure [3]. The opamp input common mode is set to ground. All switches in Fig. 1 are connected either to ground (if NMOS) or V_{DD} (if PMOS) and they can properly operate from a single supply equal to $V_{DD}=V_{TH}+V_{ov}$. In order to achieve rail-to-rail output swing, the output quiescent common-mode voltage is set to $V_{DD}/2$. This is obtained using a SC level shift between input and output common mode voltages through the use of C_{DC} which is set to be equal to $C_{DC}=C_{IN}/2$. In the realization a fully-differential topology is used to double the output swing. This gives also, at no extra cost, a sign change which is needed to build closed-loop structures without any additional inverting stage.

Fig. 2 shows the used fully-differential two-stage opamp [3]. Since the input common mode is set to ground, PMOS input stage is used . The second stage is an inverter-like stage whose output common-mode voltage is set to $V_{DD}/2$ to maximize output swing.

The opamp can operate with a minimum supply voltage equal to $V_{DDmin}=V_{TH}+2\cdot V_{ov}$, which sets the minimum supply voltage for all the system. To speed up the turn-on time of the opamp, only the second stage is turned-off, while the first stage is always kept active. In addition the Miller compensation capacitance is connected to the source of the NMOS folding device of the first stage through the series switch MS. Since this node is kept at a voltage only one V_{ov} higher than ground, the switch can be properly driven with a clock amplitude equal to V_{DDmin}. When the output stage is turned-off, MS disconnects the compensation capacitance which remains charged.

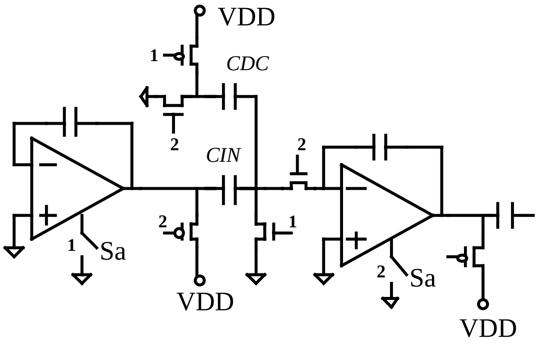
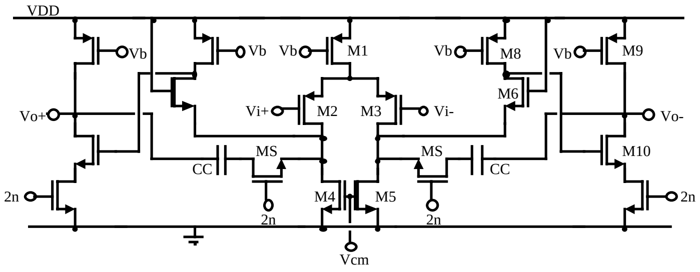


Fig. 1 - Switched-opamp integrator

Fig. 3 shows the proposed dynamic CMFB circuit able to operate at V_{DDmin} with a large differential opamp output swing. The CMFB opamp is a single-ended structure with PMOS input stage and input common mode voltage equal to ground. The CMFB steady state occurs when the charge injected in the integration capacitance (given by $C_P\cdot(V_{DD}-V_{out+})+C_M\cdot(V_{DD}-V_{out-})+C_{CM}\cdot(0-V_{DD})$) is zero. With $C_{CM}=C_P=C_M$ the output opamp common mode is set to $V_{DD}/2$. Also in this structure all the switches are connected to ground or to V_{DD}. For stability reason continuous-time feed-forward capacitors C_{FF} are included in the loop to create a zero. They are disconnected during reset phase and remains charged. During the on-phase the opamp requires 80µW power for a V_{DD}=1V, performs a gain larger than 75dB with an unity gain bandwidth of 30MHz for a 1pF load capacitor.



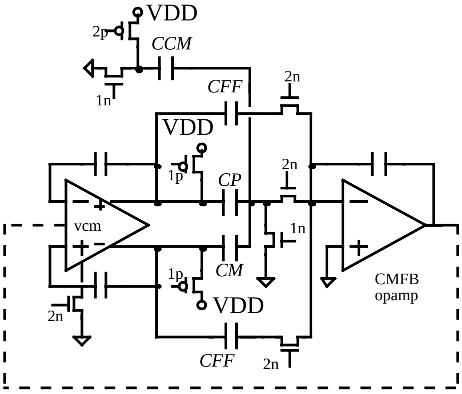


Fig. 2 - Low-voltage opamp structure *Fig. 3 - Switched-opamp CMFB circuit*

The quantizer must be able to sense a differential input signal centered at $V_{DD}/2$ (0.5V). Therefore the basic problem to read a differential voltage around $V_{DD}/2$ is again to be solved. The proposed solution for the low-voltage quantizer is shown in Fig.4. It is composed by a fully-differential switched-opamp preamplifier which is followed by a chain of digital inverters.

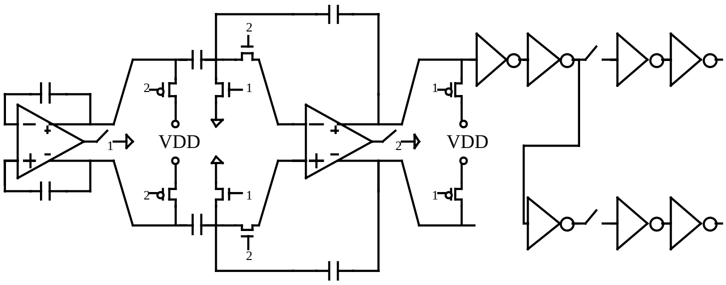


Fig. 4 - Low-voltage differential quantizer

The preamplifier is designed in order to implement a gain in the order of 5; in this way it make the differential signal to be sufficiently high to be properly read with a single ended block in one of the two output node. Following this preamplifier, the actual quantizer is realized with a single digital inverter applied to one of the two output nodes, while the other polarity is obtained by a sign inversion in the digital domain. Using this solution the threshold voltage is not externally fixed and it is set by the threshold of the inverter chain. This solution is possible since in a single-bit modulator the threshold value imprecision is not critical. After the digitalization of the sample, the latch is made-up of a series complementary-MOS switches which are capable to operate at low-voltage since their input signal is always equal to VDD or ground. The rails are used as reference voltages for the feedback. Therefore also in the feedback path, NMOS-only (for ground connection) or PMOS-only (for the VDD connection) switches are used.

III. Experimental results

The above building blocks have been used to realize a 2nd order bandpass ΣΔ modulator. Its architecture [4] is shown in Fig. 5. Notice that the required bandpass response allows to avoid a dc-connection with the input signal, which is one critical point for lowpass implementation [2]. As reference voltage for the feedback the supplies (1V and ground) have been used.

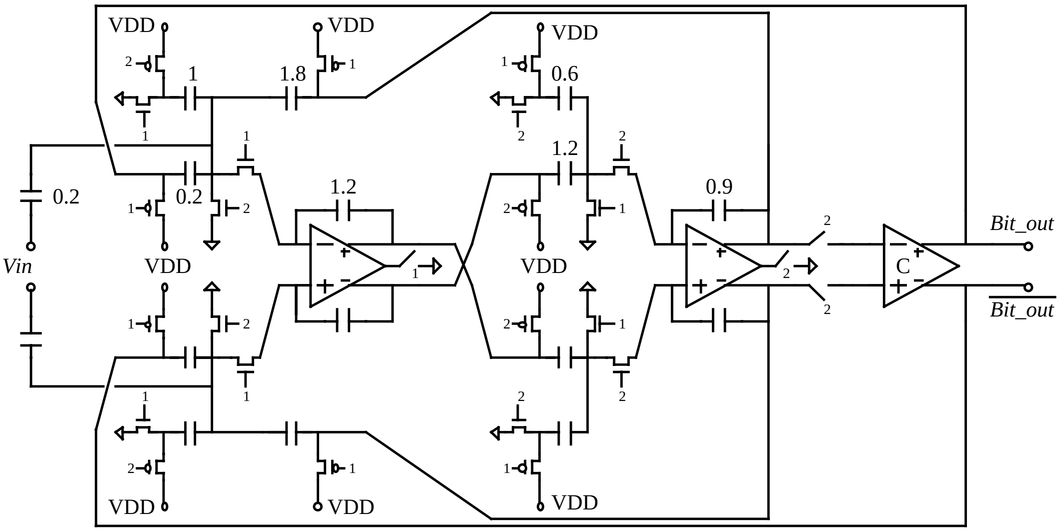


Fig. 5 - Low-voltage bandpass ΣΔ modulator architecture

Since the circuit is fully-differential, this corresponds to a full-scale of 2Vpp. The circuit has been realized in standard 0.5μm CMOS technology (V_{THn}=0.65V, V_{THp}=0.7V). The chip photograph is shown in Fig. 6. The chip area is about 1.5mm^2. The used capacitor values are indicated in the Fig. 5, in pF units. Using a 1.8MHz sampling frequency, for a 0.8Vpp input differential signal (-8dB), a 32768-bit digital output sequence is postprocessed by FFT after having applied a Hanning window. Fig. 8 shows the resulting Power Spectral Density for the frequency range from 0 to Nyquist frequency. The expected bandpass noise shaping is obtained. A zoom of this plot around the center frequency is given in Fig. 9.

The SNR vs. signal amplitude is reported in Fig. 10, for a signal bandwidth of 20kHz (the 0dB full-scale corresponds to 2Vpp signal amplitude). A 42dB SNR peak is achieved. In this plot the ideal slope of the SNR is also reported (i.e. for 46dB dynamic range). A good agreement between ideal and experimental behaviour for signal higher than -12dB can be observed. The structure is therefore limited by the quantization noise and it performs an extrapolated dynamic range equal to about 45dB. For signals lower that -12dB amplitude the SNR experimental data are lower than theoretical ones. This difference is due to the fact that the realized 2nd order bandpass modulator (equivalent to the 1st order lowpass structure) intrinsically suffers from tone generation [5, 6]. Table I summarizes the modulator performance.

IV. Conclusions

A 1V bandpass ΣΔ modulator has been realized within a standard 0.5µm CMOS technology. The aim of this work is to demonstrates the validity of the proposed building blocks, moving the optimization of the modulator performance to other works. However the 45dB dynamic range achieved with the prototype modulator demontrates the feasibility of the proposal.

Technology	0.5µmCMOS
VTHn	0.65V
VTHp	0.7V
Sampling frequency	1.8MHz
Center frequency	400kHz
Signal bandwidth	20kHz
Dynamic range (extr.)	45dB
SNR peak	42dB
Full-scale	2Vpp
VDD	1V
Power consumption	240µW
Chip area	1.5mm^2

Table I - 1V bandpass ΣΔ modulator performance

References

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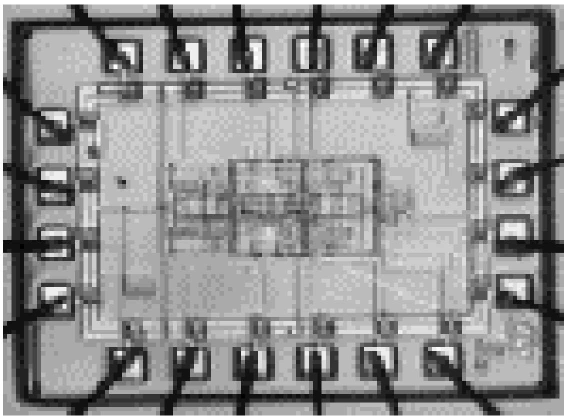

Fig. 6 - Chip photograph

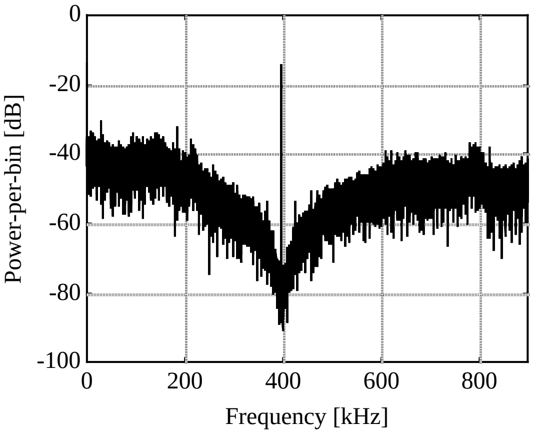

Fig. 7 - Modulator PSD

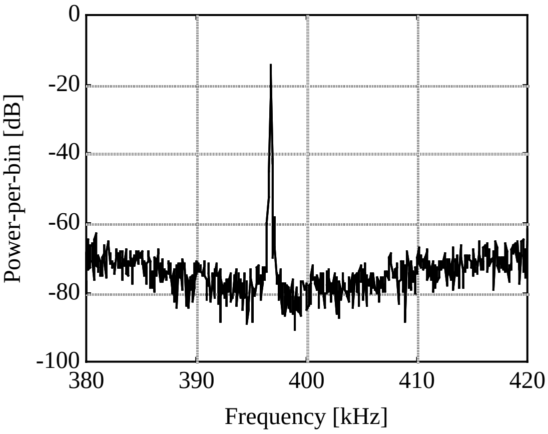

Fig. 8 - In-band PSD

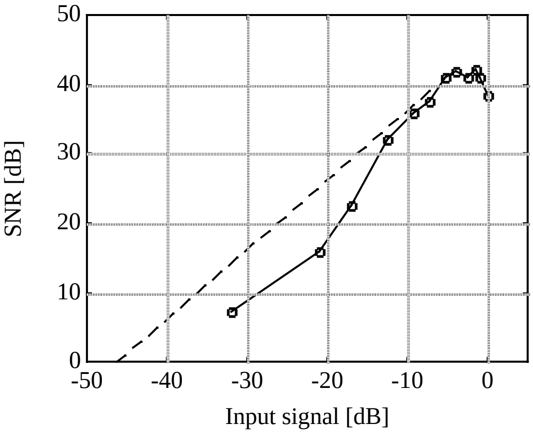

Fig. 9 - SNR vs. signal amplitude