Novel Level-Identifying Circuit for Flash Multi-Level Memories

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This paper presents a high-speed, small-area circuit specifically designe levels in the read out operation of a Flash Multi-Level Memory. The analog computation of the Euclidean Distance between the current rea cell and the reference currents that represent the different logic version of the circuit has been integrated in a standard double-meta with a die area of only 140 x 100 μm^2. Operating under a 5V power identifies the read-out current of a memory cell and associates it w level in 9 nsec.

1. Introduction

In order for Flash technology to access the profitable market portable applications, the cost per bit must be reduced. Device expected to take the bit cost down to $1/Mbyte by the year 2000 [extensive additional circuitry is required to write and read multiple Charge Storage (MLCS) could further reduce this cost by at least a f technology generation.

Reading multiple charge levels does not only mean that the cell in the binary case), but also that it is compared with reference cu which of the different logical levels it represents. This latter ope dedicated circuit which consumes silicon area, enlarges the periphe consequently, decreases the area reduction produced by using MLC introduces a delay which increases the access time of the memory. uttermost importance that the design of this ‘level identifying’ circ area and propagation time.

The architecture’s presented so far in the literature, show between area on one side and propagation time on the other. In fact architecture’s obtain high speeds through a single comparison step, independent from the cell content but they need n-1 comparators (n = to be implemented on silicon; sequential architecture’s [2] are much time depends on the cell content, but only one comparator is need architecture's utilise a single comparator, but extra logic circuitr state machine [3] and the propagation delay is larger than in the par

This paper presents a new fully parallel 'level identifying' c utilise comparators and is designed specifically to minimise die area

2. Working Principle

The circuit working principle and block diagram are shown i respectively. In order to realise the multi-level signal compariso between the read-out current and each of the reference currents (L1. four 'Distance Measuring' sub circuits of Fig. 2. Each of these sub c voltage that is proportional to the similarity of the measured curr signal (MS). The better the match, the higher the MS voltage becomes. to the second stage of the circuit of Fig. 2, the Winner-Take-All decides which of the four MS's is the highest and brings the correspo digital state, while the other three outputs remain low. Only one ou any given cell current value.

3. Circuit Implementation

This block receives two input signals (I$_{dc}$ and I$_{dx}$) and deliv (V$_{MS}$) that is proportional to the similarity between the two input cu the Euclidean distance between the currents, the higher is V$_{MS}$. Tl Euclidean Distance can be expressed as:

$$Dist = \sqrt{(R-L)^2} \qquad (1)$$

where R and L are two generic monodimensional vectors. V$_{MS}$ must be a monotonicall decreasing function of Dist. To implement expression (1) on silicon, of a long channel MOSFET in saturation is exploited:

$$I_{DS} \cong K\left(V_G - V_S - V_T\right)^2 \qquad (2)$$

Applying a voltage signal (R) to the gate of a MOSFET is straightforw to apply a voltage (L) to its source, a second MOSFET in the source must be connected to the source of the driving n-MOS device. In this L)^2 is implemented. The so obtained I$_{DS}$ is then fed to a p-MOS device in th configuration which implements the square root function.

The considerations mentioned above lead to the DM block circui which includes two driving n-MOS device (M2, M3) with the respectiv (M4, M1), a diode connected p-MOS device (M5) and two current-to-vo MOS device (D1, D2). The dimensions of the transistors are reported i have an aspect ratio which is ten times that of M2 and M3 since the transistors utilised to bias the source of the driving transistors. T with respect to the driving transistor, the more accurately the s Simulations show that a factor of 10 is a good compromise between

consumption. D1 and D2 convert I_{dx} and I_{cell} into V_C and V_D respectively. If I_{cell} i
than I_{dx}, then M2 is cut off since the voltage at its source, V_C, is h
at its gate. However, M3 is on and the larger the difference between its
drain current and the smaller is V_{MS}. On the contrary, if I_{cell} is sm
cut off and M2 is on.

Fig. 4 shows the proposed WTA, which consists of 4 current
(MS0...MS3) and 4 current comparators. The WTA receives the four V_M
blocks as input signals at the gates of the current conveyors and de
signals. The current conveyors have the source node (X) in common a
same biasing current. When the V_{MS}'s are applied to the gates of th
follows the largest input voltage, turning off the other three conv
will flow only through the conveyor with the largest V_{MS}. Only the co
V_{MS} will drive current and result in a high output voltage.

4. Experimental Results

An experimental version of the circuit has been integrated in a
double-metal 0.7-µm process with a silicon area of only 140 x 100 μm^2, as shown in the
picture of Fig. 5, and has been extensively evaluated.

Fig. 6 shows the experimentally evaluated V_{MS} as a function of a sweeping
current in the case of a reference current of 25 µA. As expected, the
the higher the V_{MS}. Fig. 7 shows the experimental output voltages o
circuit as a function of a sweeping cell current in the case of refer
and 160 µA. Only one output voltage is high for any given cell curren

5. Conclusions

The sensing and the correct identification of multi-level sign
issue in the design of MLCS memories. An adequate fully parallel arch
employs a system of four analog computational blocks and a winner-tal
propagation delay and the die area.

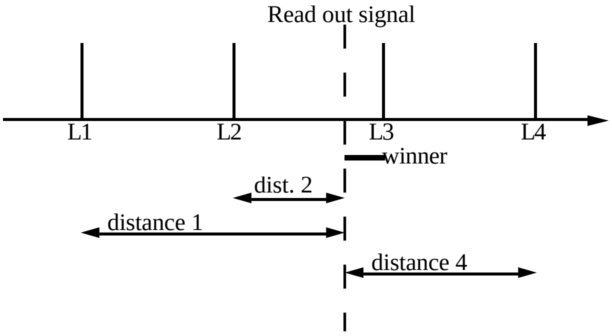
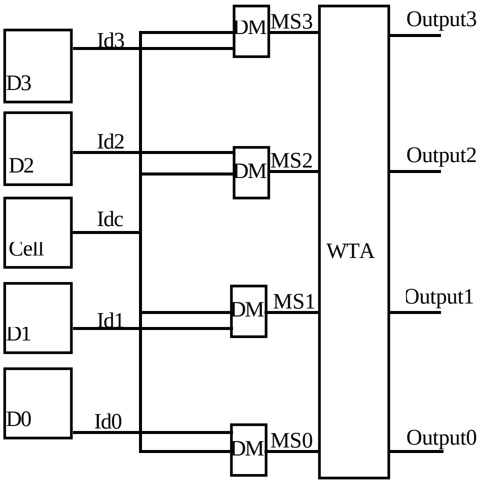


Fig.1: Level Identifying circuit: working principle.

	W (µm)	L (µm)
M1	70	0.7
M2	7	0.7
M3	7	0.7
M4	70	0.7
M5	1.5	0.7
MS0	70	0.7
MS1	70	0.7
MS2	70	0.7
MS3	70	0.7

Table 1: Transistor dimensions.



D0, D1, D2, D3: Dummy cells.
Cell: Memory cell.
Idx: Read-out current.

DM: Distance Measuring Block.
WTA: Winner-take-all.

Fig. 2: Block diagram of the level identifying circuit.

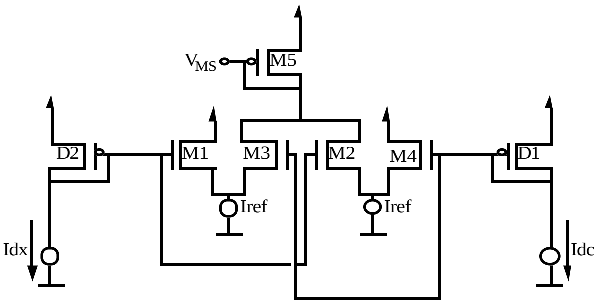


Fig. 3: Distance Measuring Block.

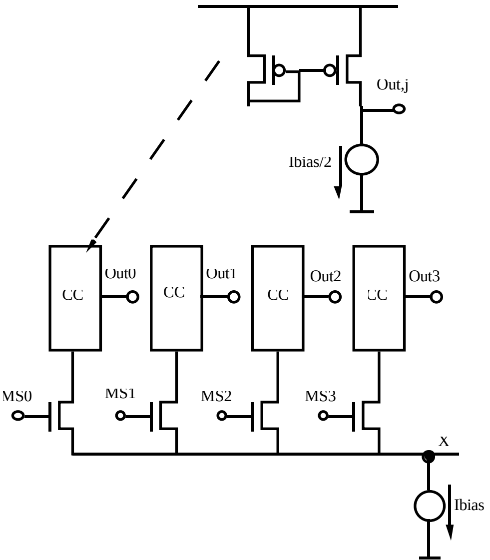


Fig. 4: Winner-Take-All

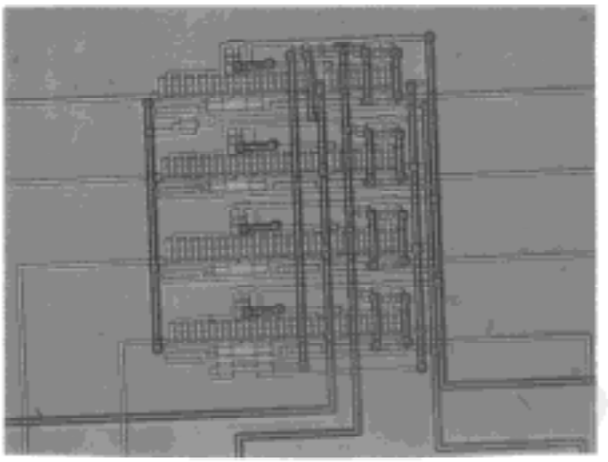


Fig. 6: Micrograph of the level identifying circuit.

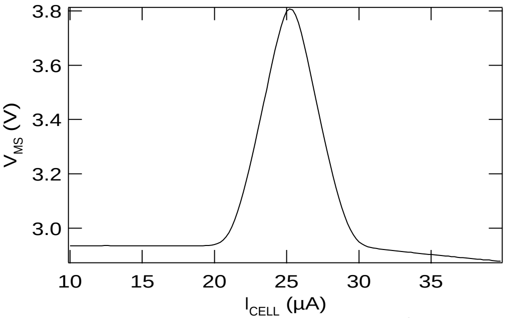


Fig. 6: ‘Distance Measuring’ transfer characteristic.

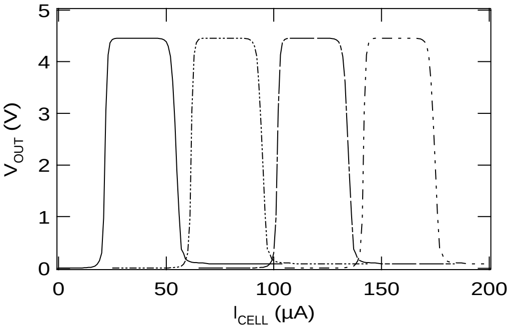


Fig. 7: ‘Level Identifying’ transfer characteristic.

References

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[4] Patent pending.