

A Wide Range dB-linear Variable Gain CMOS Amplifier

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Abstract — A 10 MHz 6-stage CMOS amplifier with variable gain from 0 dB up to 80 dB is presented. Differential inputs and outputs provide a high PSRR. The gain is controlled by a dB-linear differential voltage. At a single power supply voltage of 5 V the maximum linear input and output swing is 600 mV. The amplifier has been fabricated in a $1.6\mu\text{m}$ CMOS process and covers a chip area of 0.72 mm^2 . Measurements of a fully integrated automatic gain control are presented.

1 Introduction

Processing optical transmitted signals often means to provide a wide range automatic gain control (AGC) due to the square law dependency between distance and intensity of such signals. The purpose of the presented IC is to amplify an optically received pulse position coded signal with an amplitude range of more than 70 dB. Within $5\mu\text{s}$ the amplification has to be adjusted. The pulse position recognition of 50 ns pulses requires a 3 dB-bandwidth of at least 10 MHz. Since the minimum input signal level is supposed to be $100\mu\text{V}$ a high power supply rejection ratio (PSRR) and low thermal noise ($15\text{ nV}/\sqrt{\text{Hz}}$) are required. The AGC has been implemented in a standard CMOS process and — in contrast to [1], [2], and [3] — without any precise ohmic or bipolar components.

2 Circuit Description

The principal part of the AGC is the variable gain amplifier (VGA). It has been designed as a 6-stage amplifier with a gain between 1 and 5 per stage and a DC-decoupling after each stage. To provide a sufficient PSRR all stages have differential inputs and outputs. The gain is also controlled by a differential input.

2.1 Stage Design

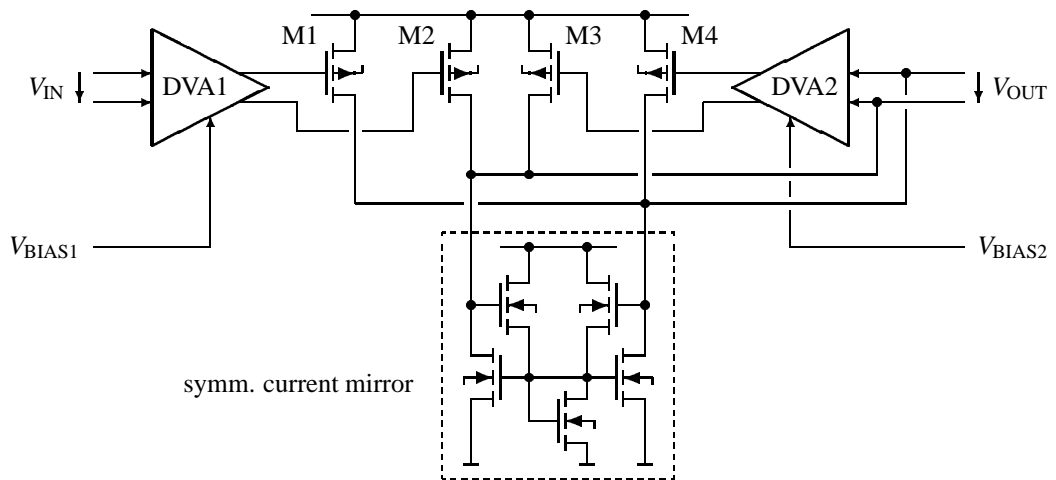


Figure 1: Circuit diagram of one VGA stage

Figure 1 illustrates the schematic of one stage of the VGA. A fully symmetrical highly linear differential voltage amplifier (DVA1) shifts the differential input signal to the common mode voltage given by V_{BIAS1} (i.e. $V_{BIAS1} \pm V_{IN}/2$). The output voltages of DVA1 control the drain-currents of M1 and M2. A fully symmetrical current mirror generates the difference between both currents which is linear dependent from the input voltage V_{IN} . V_{BIAS1} determines this highly linear transconductance G_1 . In the same manner a second transconductance G_2 — controlled by V_{BIAS2} — transforms the output voltage V_{OUT} into a second current that is adjusted by feedback to be equal to the first current. This results in a stage gain of

$$\frac{V_{OUT}}{V_{IN}} = \frac{G_1}{G_2}$$

To achieve a positive gain of $\sqrt{5}$ for $V_{BIAS1} = V_{BIAS2}$ the width of M1 and M2 is $\sqrt{5}$ times larger than the width of M3 and M4. The symmetrical current mirror shown in Figure 1 provides a common mode voltage level of the output signal of about 3 V. Figure 3(a) depicts the input-output transfer function of one stage.

2.2 The Entire VGA

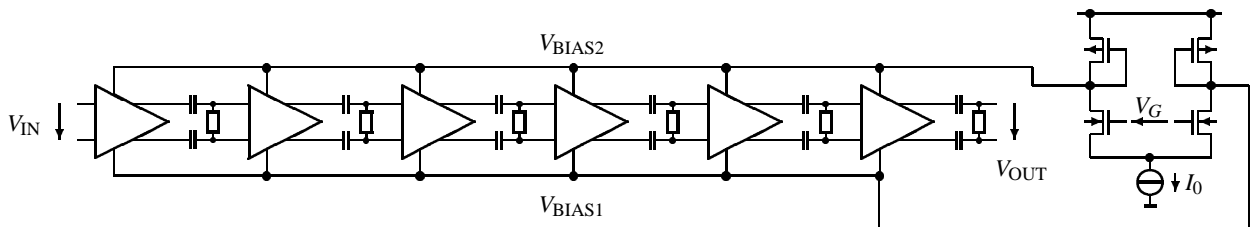


Figure 2: Block diagram of the 6-stage VGA

Figure 2 shows the entire VGA which consists of 6 stages of that kind described above, all controlled by the same voltages V_{BIAS1} and V_{BIAS2} . V_{BIAS1} and V_{BIAS2} are generated by a double-ended differential stage with PMOS load. This leads to a dB-linear voltage controlled gain. The transistor channel widths and the quiescent currents of the first three stages are graded to reach an optimum concerning input noise (at maximum gain) and power consumption.

A high-pass filter after each stage (represented by RC combinations in Figure 2) provides a DC-decoupling to suppress an offset voltage caused by mismatch effects (simulated with the computer program “GAME – General Analysis of Mismatch Effects”¹). Figure 3(b) shows the simulated gain of the entire 6-stage VGA for a gain control voltage V_G of $-0.6 \dots 0.6$ V (step size 0.2 V). There is a (nearly) linear increase in gain of about 60 dB/V. The entire power dissipation is about 37 mW. A “stand-by” mode allows to limit the power consumption to 1 mW within a few μ s.

2.3 Automatic Gain Control

The task was to adjust the gain within a very short time. This has been realized by a differential voltage comparator and a PI-Controller with different attack and release times. The output voltage of the VGA is adjusted to 400 mV (peak) by this AGC feedback. The AGC release time (from 0 dB up to 80 dB) is about 500 μ s but a RESET input allows to reach the maximum gain within 5 μ s.

3 Measurement Results

A 3-stage VGA test structure and the AGC including the 6-stage VGA (Figure 5) have been fabricated in a standard (single metal, single poly) CMOS process. Figure 4(a) illustrates the input (lower curve) and the output signal of the VGA test structure using a 1 MHz PPM coded signal.

The transient response of the AGC is depicted in Figure 4(b). At the beginning of this measurement there was no input signal and therefore the AGC had reached maximum gain when the amplified input noise became 400 mV (peak). The gain control voltage (upper curve) was at the higher limit. After 10 μ s the input signal was turned on and the AGC decreased the gain by ≈ 40 dB until the output signal reached the demanded level after additional 5 μ s.

4 Conclusions

A dB-linear 6-stage voltage controlled amplifier with a wide range of 80 dB has been presented. It provides a large input and output swing of up to 600 mV at a power supply voltage of 5 V. The presented experimental results show that the amplifier is very well suited for an integrated automatic gain control.

Since the implementation in a 1.6 μ m standard CMOS process allows a bandwidth of more than 10 MHz a corresponding higher speed would be possible in a modern 0.8 μ m CMOS process.

References

- [1] T. Pan and A. A. Abidi, “A 50-dB Variable Gain Amplifier Using Parasitic Bipolar Transistors in CMOS,” IEEE Journal of Solid State Circuits, vol. 24, pp. 951–961, Aug. 1989
- [2] J. J. F. Rijns, “CMOS Low-Distortion High-Frequency Variable-Gain Amplifier,” Proceedings of ESS-CIRC’95, pp. 46-49, Sept. 1995
- [3] E. A. M. Klumperink, C. T. Klein, B. Rüggeberg, A. J. M. van Tuijl, “AM Suppression with Small AM-PM Conversion by Means of Variable Gain,” Proceedings of ESSCIRC’95, pp. 214-217, Sept. 1995

¹available from <http://luzi.e-technik.uni-dortmund.de/~grueneba>

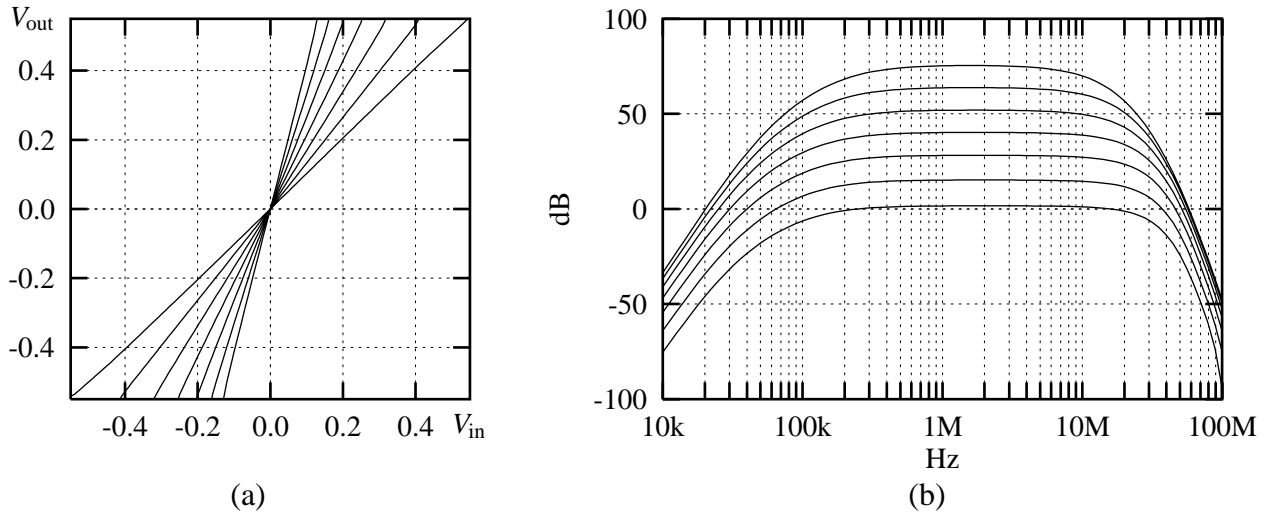


Figure 3: Simulated transfer function of one stage and overall gain of the 6-stage VGA

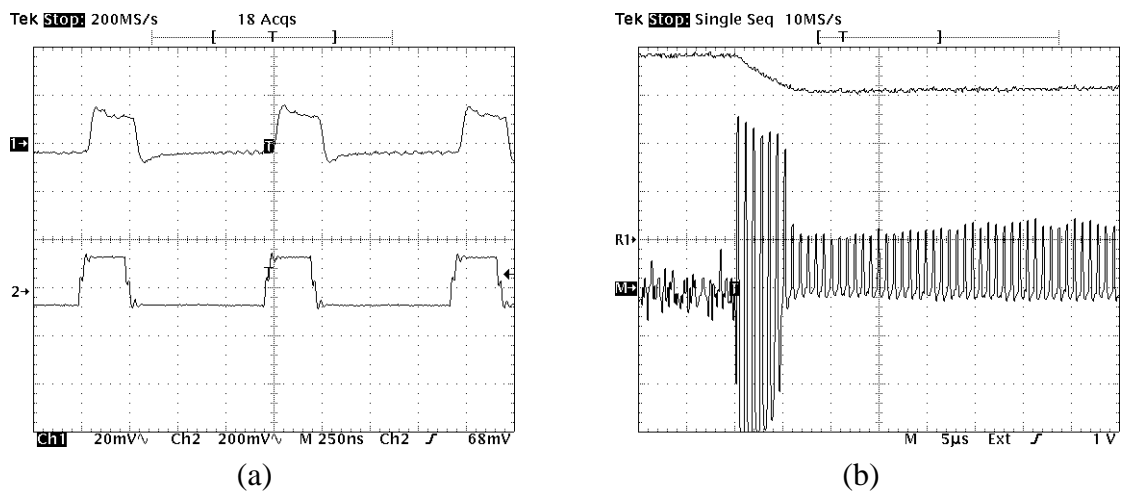


Figure 4: Measured output of the VGA and transient response of the AGC

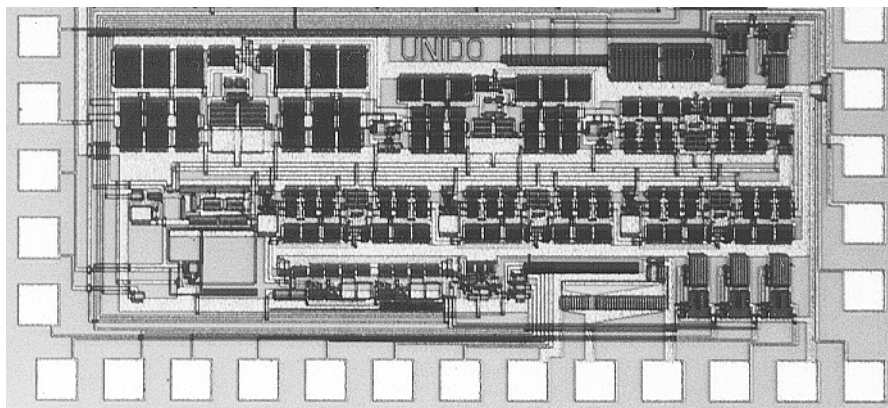


Figure 5: Microphotograph of the entire AGC