Mismatch Modelling for Large Area MOS Devices

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Abstract — Investigations were made on mismatch effects in a bit cell for an analog-to-digital converter, fabricated in a 1.6μ/45nm CMOS process. The cell was designed to yield in a given bit resolution, considering the mismatch effects described by the well known law of area. It could be shown that large area MOS transistors are subject to a matching accuracy saturation effect, which makes it necessary to extend the mismatch model. An enhanced mismatch model is presented, which allows statistical simulation and prediction for both large area effects and for long distance effects between devices. The model was successfully verified by measurements and implemented into the statistical simulator GAME[1].

1 Introduction

As large area devices are frequently used in analogue MOS circuits, e.g. in current mirrors with big transmission ratios, a modelling of large area and long distance mismatch is necessary for the design of precision applications. As measurements show, the standard mismatch law of area [1, 4] does not yield correct results for large devices and long distances between devices. In fact, the predicted accuracy is not reached, instead it becomes even worse when device areas increase over a specific amount. A similar effect can be observed for the matching error over distances between devices, which was stated to increase linearly for small distances in [2], but in fact does not grow beyond the global tolerance for long distances.

The mentioned effects were studied during the development of an analog-to-digital converter as described in the following sections.

[1] General Analysis of Mismatch Effects, available from
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2 Analog-to-Digital Converter with Bit Cells

A current mode analog-to-digital converter was designed using a variation of the bit cell principle introduced in [3] (figure 1). The converter consists of a chain with one cell per bit. Each cell amplifies the current for its successor by a factor of two, and substracts the full range current from its output when it detects a high bit.

The bit resolution of the converter is on the whole determined by the first bit cell, which has to take the MSB decision with a precision of at least one half LSB. For a given bit resolution and a given minimum yield of fabricated circuits, the standard deviation σ_{trans} of the MSB cell's low-high-transition is given by (1), where 1σ leads to a yield of ≈ 68 percent, 2σ to ≈ 95 percent and 3σ to ≈ 99 percent of usable circuits.

$$\sigma_{trans} \leq \frac{V_{max}}{2^{Res_{Bit}}} \tag{1}$$

The tolerance behaviour and thus σ_{trans} is mainly caused by local mismatch effects in the differential input stages of the first bit cell, which consists of five similar OTAs (figure 2). In order to achieve the given resolution, the areas of the input transistors M8, M9 and the load transistors M3, M4 were calculated regarding the mismatch law of area.

Two bit cells with different precision and thus different device geometries were designed and fabricated in an industrial $1.6\mu/45$nm CMOS process. Table 1 shows the transistor areas of the different layouts.

Geometries	M8, M9	M3, M4
Layout 1	35000 μm^2	90000 μm^2
Layout 2	5010 μm^2	15000 μm^2

Table 1: Device Geometries

3 Enhanced Mismatch Modelling

The mismatch law of area stated in [1] (eq. 2) describes the real device behaviour correctly only for small device areas, as well as the law of distance stated in [2] (eq. 3) is valid only for relatively small distances, with W and L given as the layout dimensions and D as the distance between corresponding (matching) devices. Both equations give a share on the standard deviation σ_P of a model parameter P.

$$\sigma_{P_{Area}} = \frac{A_P}{\sqrt{Area}} \tag{2}$$

$$\sigma_{P_{Distance}} = S_P \cdot D \tag{3}$$

The improved model (eq. 4), shows the same behaviour for small geometries W, L and D. For large areas $W \cdot L$ a slow transition is performed into a static final value, given by $\sigma_{P_{Wafer}}$. A similar transition happens for large distances D between corresponding devices.

$$\sigma_P = \left(\frac{A_P}{\sqrt{WL}} + \sigma_{P_{Wafer}}\right)\left(1 - \mathrm{e}^{-\frac{D+(W+L)\alpha}{D_0}}\right) \cdots + \frac{A_P}{\sqrt{WL}}\,\mathrm{e}^{-\frac{D+(W+L)\alpha}{D_0}} \tag{4}$$

$\sigma_{P_{Wafer}}$ is the standard deviation of P over the entire wafer excluding the share of local mismatching, D_0 is a measure for long distances, and α defines the ratio of the value for large device dimensions relative to D_0. A typical value for α is 1/3.

For making use of the proposed mismatch model, no new measurements are needed. A_P is the parameter for local mismatching of P, which is identical to the parameter in (2) and (3). D_0 can be calculated from the old S_P parameter ($D_0 =$

$\sigma_{P_{Wafer}}/S_P$), and P_{Wafer} is obtained from wafer statistics of the parameter P.

Figure 4 shows the statistics of the NMOS threshold voltage mismatch extracted from 60 measured samples increasing with the distance. The W/L device dimensions of the measured test structures are 25/16, 12.5/8, 5.5/8, and 4/4 μm. The test structures were fabricated in another industrial 1.6μ/40nm CMOS process. Predictions made with the improved model (dotted lines) correspond well with the measurement results. Similar behaviour was found for the MOS parameters K_P and γ, too.

Figure 5 depicts the threshold voltage statistics for NMOS transistors dependent on the device area only. For small area devices with dimensions $< 20\mu$m the simple statistical law of area corresponds with the proposed model. However, for devices with dimensions much larger than 20μm the difference becomes significant. The originally expected matching improvements by enlarging the device area (W, $L > 1000\mu$m) do not take place, instead the parameter mismatching increases.

4 Results

Table 2 shows the measurements of 45 samples compared with statistical simulations using the old mismatch model from [1] and the enhanced model for large area devices given by (4). The cells were designed for an input current range of 0–255μA.

Layout 1	σ_{trans}	Resolution
Measurement	1.76μA	7.2 bit
Old model	0.41μA	9.3 bit
New model	1.76μA	7.2 bit
Layout 2	σ_{trans}	Resolution
Measurement	1.07μA	7.9 bit
Old model	0.89μA	8.2 bit
New model	1.19μA	7.7 bit

Table 2: Comparison between Measurements and Simulation

It is obvious that the new model gives a much more realistic prediction of the mismatch behaviour, especially for the larger devices in layout 1 where the mismatch accuracy saturation can clearly be seen.

5 Conclusion

It could be shown that mismatch in large area MOS devices differs significantly from the law of area given in [1, 2]. An enhanced model was proposed which can be used with existing matching parameters. An accurate matching parameter extraction method is available [7]. The new model achieves a good correspondence between simulation results and measurements.

References

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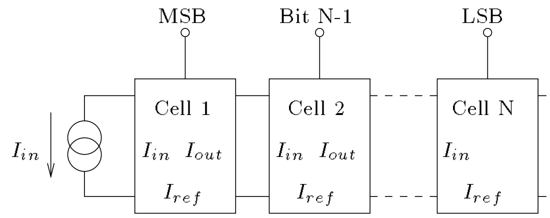

Figure 1: Current Mode A/D Converter with Bit Cells

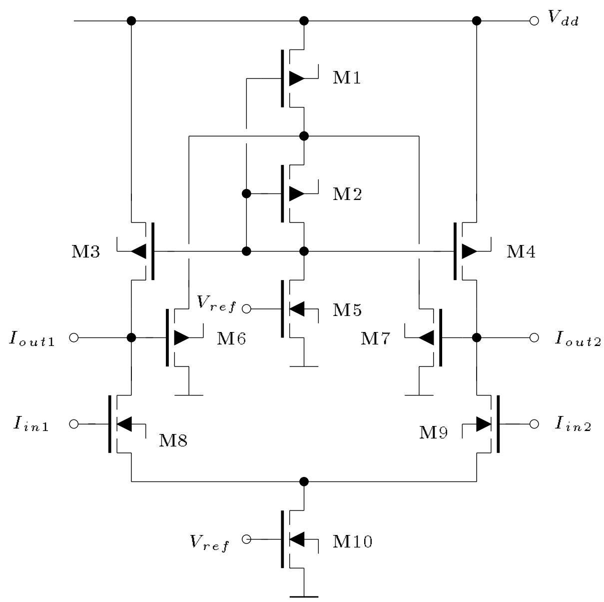

Figure 2: Differential OTA Circuit for Bit Cell

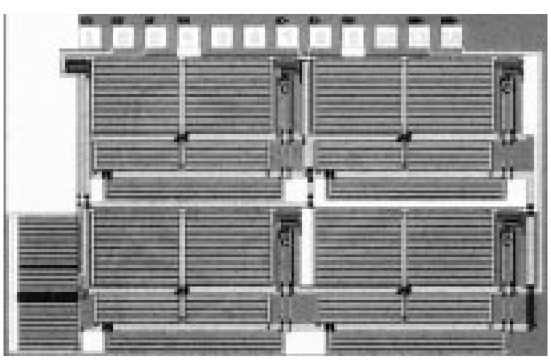

Figure 3: Chip Photograph of the Bit Cell, Layout 1

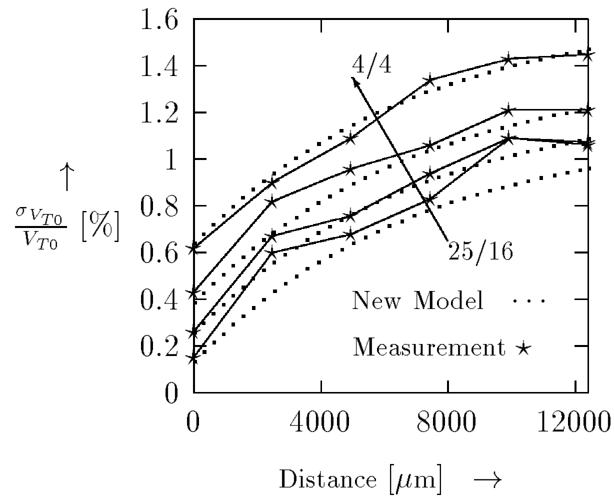

Figure 4: Long Distance Mismatch of NMOS Parameter V_{T0}

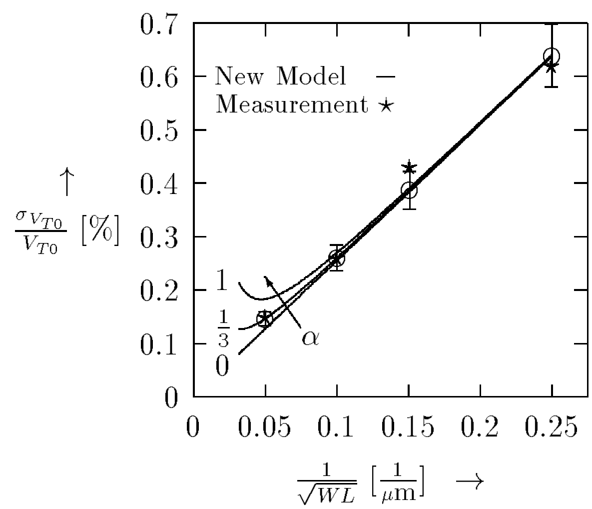

Figure 5: Short Distance Mismatch of NMOS Parameter V_{T0}