

# A ROBUST ANALOGUE INTERFACE SYSTEM FOR SUB-MICRON CMOS VIDEO DSP

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## ABSTRACT

*This paper describes the front-end architecture for a fully integrated low voltage CMOS video DSP function, including AGC, equalisation, clamping, sync and A/D conversion. Attention is paid to minimising the influence of substrate and power supply noise despite a large digital part with differing clock domains. The system maximises the available dynamic range in the 3.3V supply, with several high bandwidth rail-to-rail functions. A novel arrangement with high noise immunity level estimators is used to clamp the video in the middle of the dynamic range of the AGC input, hence minimising the amplification of unwanted DC components. Extensive mixed signal test facilities are also included in the design. The chip is fabricated in 0.5u CMOS, and operates from a single 3.3V supply.*

## INTRODUCTION

Modern consumer video products demand more and more DSP functions, and so TV integrated subsystems are moved rapidly into the most dense logic technologies. For the analogue interfaces there is a problem here, since as processes have moved to 0.5u and below, the analogue subsystems must be adapted for 3.3V supplies, whilst board level video signals remain at the traditional 1V nominal level. A further challenge is the need to maintain or improve the performance of the analogue interface function in the presence of increasing noise levels on the die, due both to the transparency of epi substrates, and to the large logic areas with many active digital interface ports.

In this paper we present an analogue interface system which addresses these problems, and shows good performance with little susceptibility to the activity of the large digital section of the full chip.

## SYSTEM LEVEL ISSUES

The basic requirements for the analogue interface and acquisition section are quite well defined. A normal composite video signal with a nominal 1V p-p amplitude must be clamped to a suitable reference and then digitised for digital processing. The -0.3V sync pulses must be located and timing information extracted. Because of the possible +/- 3dB variation in signal amplitude presented to the IC by different video IF systems, an AGC function is included so that the effective quantisation of the video information remains essentially constant. There is also a need for a small amount of equalisation. The signal is then acquired using a flash type A/D.

A major issue here is how to avoid digitising the large amount of substrate and power supply borne noise. Noise levels are high; in this application, a DRAM interface function is a major source, particularly due to the large number of highly active pad drivers. Further, many standard analogue cell architectures only work with reduced signal swing with a 3.3V supply, encouraging the use of signal attenuation at the CMOS IC input.

These issues have been tackled in two ways. First, we use a largely differential internal path right up to the A/D. Second, the analogue signal levels inside the IC are maintained as large as possible right up to the converter. The clamping arrangement ensures that the video information can be amplified without accumulating large unwanted DC components which can cause clipping. The overall architecture is shown in figure 1.

## INPUT AMPLIFIER

A differential variable gain stage is used at the input [1], with AC coupling from the video IF. Gain is set by programmable internal current feedback, giving a nearly constant bandwidth at all levels,

and a digital control loop is driven by the main A/D. An internal bias generator gives a process-independent reference voltage at the middle of the VGA input linear range.

### CLAMPING AND SYNC SYSTEM

Because of the AGC loop, the demands for the clamping system become quite significant. Most existing schemes use either the sync pulse or the black level as the baseline, but this approach would place the median value of the video information at a voltage unrelated to the signal range of the amplifier. The DC error resulting would be a function of process, supply and input signal strength, and would be amplified through to the ADC depending on gain setting. In this design, amplitude estimator circuits find the peak of the video information as well as the black level, and from the mean of these two, a clamp feedback signal is derived. A common problem with peak detection circuits is the trade-off between response time and noise immunity. If a long time constant is chosen for good noise rejection, then the detector may not reach equilibrium from a reset state before the end of a line. If the detector has a very fast response time, the final level may be approached quickly, but noise peaks can drive the estimate beyond the true value. Here, a two stage peak detector is used. If the incoming signal is greatly different from the stored reference, then the response is fast. When the error becomes small, the time constant is changed to a large value, restricting the noise bandwidth. The concept can be represented behaviourally as in figure 2.

Numbers of large capacitors are not needed as the integration and storage is performed digitally, with some simple digital filtering included to improve noise rejection. The analogue error feedback is via small D/A converters to a constant  $g_m$  rail-to-rail transconductor [2] whose output current is integrated on the input coupling capacitor in the usual way. The use of such rail-to-rail cells ensures that the clamp and sync circuitry behave consistently under all DC input conditions and start up can be assured. The reference for the clamp is derived from the VGA itself. The clamp system is shown in figure 3. Note that the decision threshold for the response time constant is actually performed by a fast dual output rail-to-rail asynchronous comparator [2], as shown in figure 4. Between the transconductor section and the current comparator, a small fixed current is added to one branch to give an input referred offset voltage, and two logic outputs are thus derived.

A similar scheme is used to find the optimum slicing level for the sync pulse. From the black level and an estimate of the bottom of the sync pulse, the median value is fed back via another D/A to an asynchronous rail-to-rail comparator.

### EQUALISATION AND FILTERING

Provision is made for filtering and equalisation of the video. The gain-controlled differential output of the VGA is passed to a programmable differential switched capacitor filter block. To get adequate clock to cut-off ratio with the system clock, double sampling is used. For adequate dynamic range and switch efficiency, common mode input and output levels are set close to mid supply.

### BUFFERING AND A/D CONVERSION

To interface the filter and VGA to the A/D, high impedance buffering is needed for the SC circuits. In addition, differential to single ended conversion and level shifting is needed to match the input range of the converter. A modified instrumentation amplifier configuration is used with three rail-to-rail video bandwidth op-amps [2] and a polysilicon resistor network. The converter itself is a conventional 7 bit flash architecture, with an input range starting close to VSS [3].

### DIGITAL CONTROL

The digitised signal is thence passed to the main DSP function, but is additionally used to drive the gain and equalisation control loops. The entire control logic block, including the peak detector gating, storage and filtering, is synthesised from a VHDL description.

### MIXED SIGNAL TEST FACILITIES

With a relatively complex analogue system test access is desirable both for evaluation and final testing. Two test monitor points are provided which allow many of the internal analogue signals to be examined via multiplexing switches. These cover not only the signal path itself, but also the analogue feedback signals from the clamp and sync system D/A converters.

## EXPERIMENTAL RESULTS

The complete chip is fabricated in a 3.3V 0.5 $\mu$ m 3 metal digital process. The analogue interface section of the complete DSP IC is shown in figure 5. Using the test access points, the behaviour of the clamp and sync systems can be monitored in real time, albeit without the full immunity to internal noise. Figures 6 and 7 show the dual time constant behaviour of the peak detectors as black and signal peak are determined. Figure 8 then shows the clamped video together with the mid range reference voltage from the VGA, confirming that the video information is positioned to allow maximum dynamic range through the internal signal path. Figure 9 shows the sync slice level output from the internal D/A with respect to the clamped video level. The noise immunity of the system can be seen by viewing the acquired digital stream via the main test bus. A composite video signal from a generator is applied whilst the remainder of the DSP functions are active, including the external memory interface ports. The noise level on the acquired signal can be seen to be at the one lsb level (figure 10). Adding large (0.5V) external noise signals to VDDA causes similarly low levels of corruption to the digital stream.

## CONCLUSIONS

A robust analogue interface for video DSP in low voltage submicron CMOS has been described. Good immunity to substrate noise has been demonstrated and a novel signal path and clamping strategy has been developed. Although nearly all completely new designs, the analogue circuits performed to specification on the first silicon.

## REFERENCES

- [1] J J F Rijns, "CMOS Low Distortion High Frequency Variable Gain Amplifier" IEEE JSSC, Aug 1996
- [2] W Redman-White "A High Bandwidth Constant gm and Slew-Rate Rail-to-Rail CMOS Amplifier Circuit for Embedded Low-Voltage Applications", Proc VLSI Symposium, June 1996, Hawaii, USA
- [3] M J M Pelgrom et Al, "A 25MS/s 8-bit CMOS ADC for embedded applications", IEEE JSSC, Aug 1994

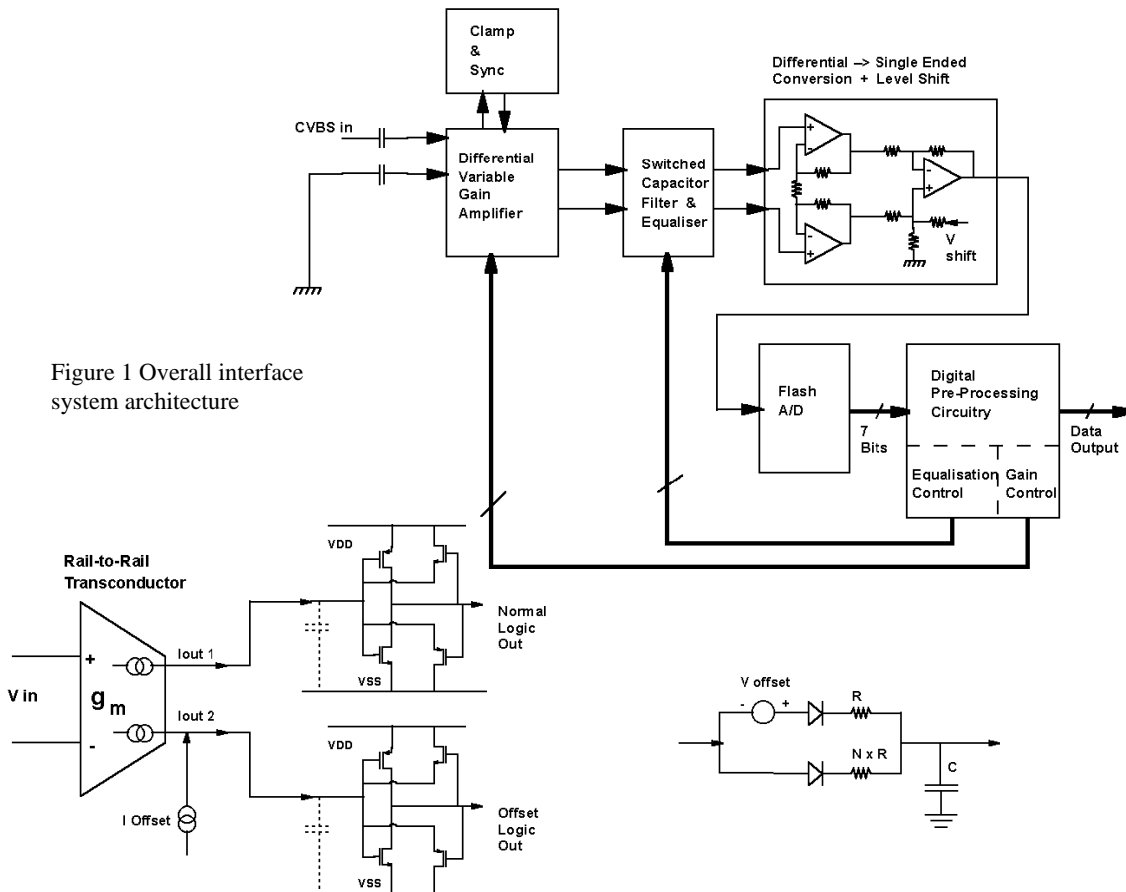


Figure 1 Overall interface system architecture

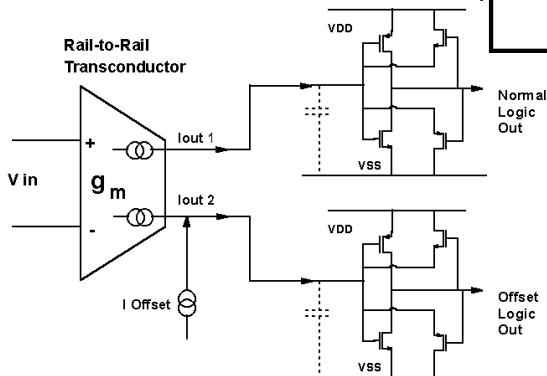


Figure 4 Dual output comparator

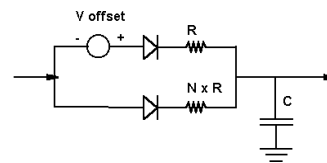


Figure 2 Peak detector behavioural model

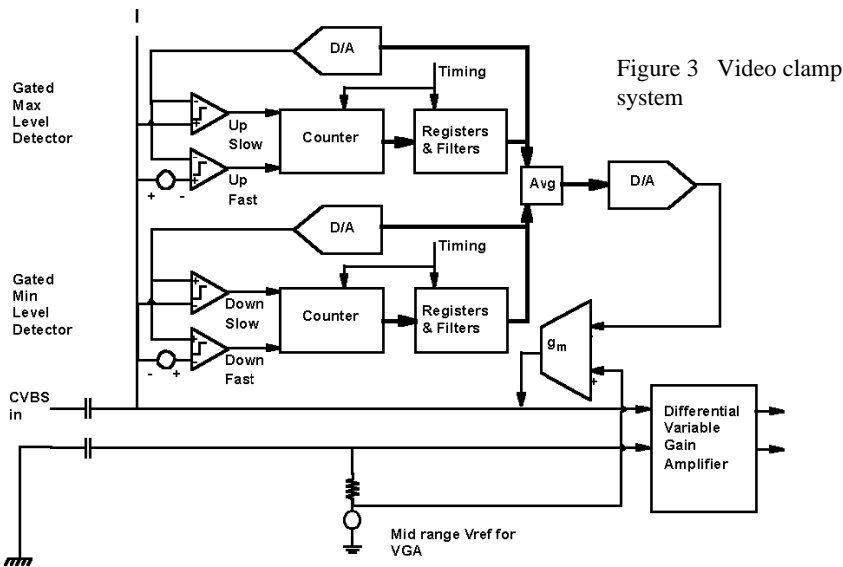


Figure 3 Video clamp system

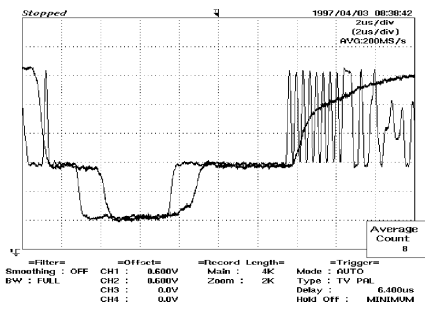


Figure 6 Peak detector D/A finding max video (via monitor ports)

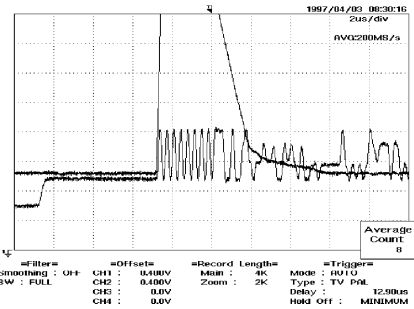


Figure 7 Peak detector D/A finding black level (via monitor)

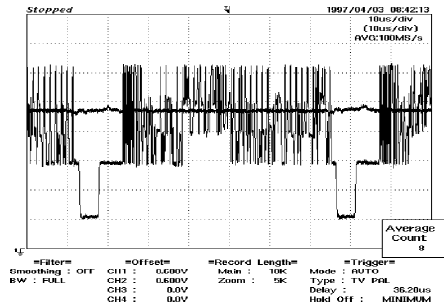


Figure 8 Clamped video and VGA mid-range reference voltage (via monitor)

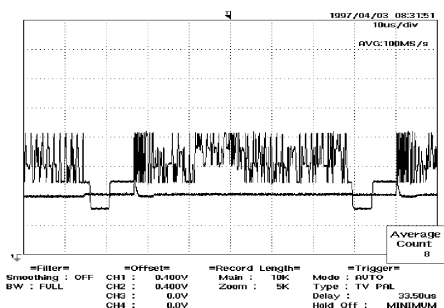


Figure 9 Clamped video and sync slice level D/A output (via monitor)

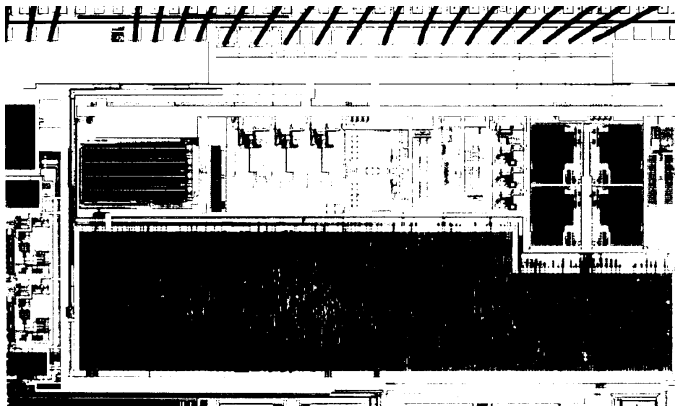


Figure 5 Analogue interface section of complete DSP IC

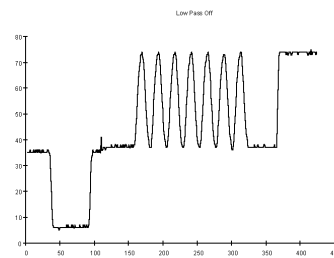


Figure 10 Digitised test signal from A/D, with DSP fully active (via digital monitor)