Multilevel Decoder-Decision Circuit for High Bitrate ETDM Transmission

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Abstract

An alternative to the classical binary format for ETDM transmission at high bitrate (over 20 Gb/s), the multilevel approach, is investigated. In this presentation, we deal with the reception end and compare different architectures for a multilevel decoder-decision circuit. Two designs are analysed in more details. A first realisation is presented, using an in-house InP/InGaAs 56 GHz DHBT technology; a comparison is done with a binary decision circuit processed at the same time. First conclusions about the multilevel format are presented.

1. Introduction

High bitrate transmissions are intensively studied to deal with the needs of multimedia applications. European Projects [1], such as SPEED and HIGHWAY, evaluate different solutions to achieve efficient **E**lectrical **T**ime **D**ivision **M**ultiplexing (ETDM) transmission at 40 Gb/s.

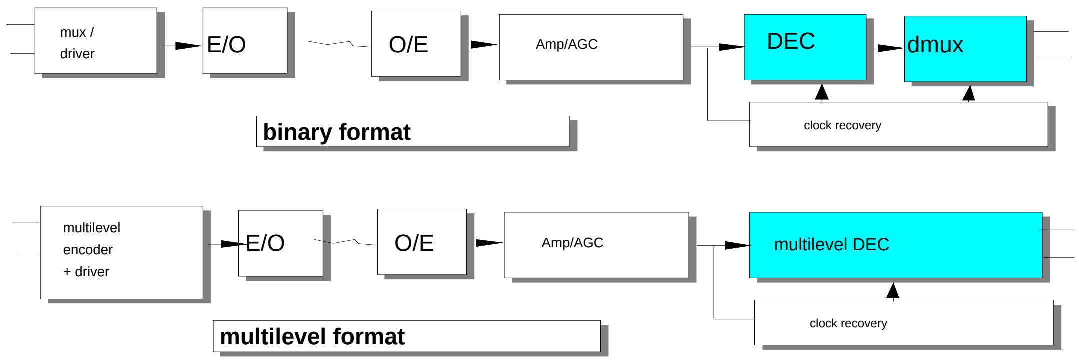


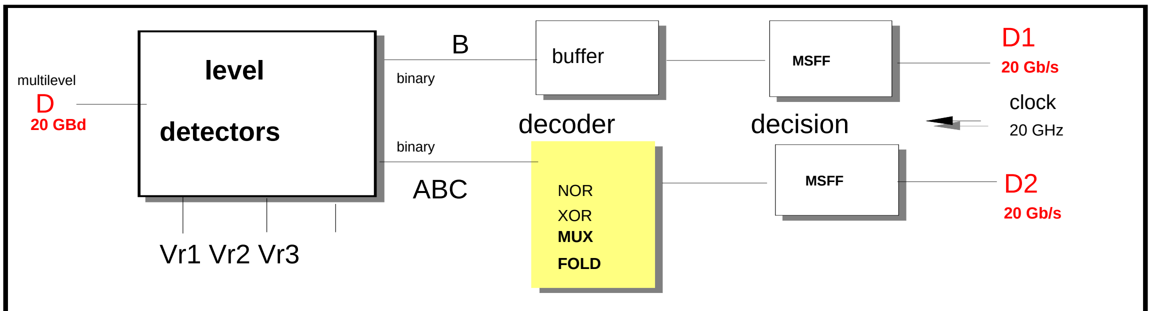
Fig.1 : ETDM Transmission Systems

Two of the most critical circuits for a **binary ETDM transmission** are the laser driver and decision circuit whose performance has been precedently discussed [2]. An alternative to the binary transmission consists in a multilevel amplitude coding, which is evaluated in the SPEED project. The most interesting one is the 4-level format, in which we transmit 2 bits in a period.

Fig.1 shows a ***4-level ETDM transmission***: at the transmitting end, the 2 binary streams are encoded on a 4-level (amplitude) signal while, at the reception, the binary streams are restored by a 4-level decoder-decision circuit (4L-DEC).
We will first present the principles and the architecture of the 4L-DEC, and compare 2 designs; we then describe the in-house technology used, and give the preliminary experimental results.

2. 4L-DEC architectures

At the transmitting end (Fig.1), two binary streams (D1 and D2) are encoded into a multivalued signal D, according to the truth table of Fig.2. This multivalued signal contains twice more information than the binary signal, for the same modulation rate. Or equivalently, the required clock frequency is twice lower for the same bitrate. This leads to an appreciable relaxation of both technological requirements and circuit layout design. On the other hand, the swing for adjacent transitions is a third of the total swing: the constraint on each level detector is then more severe. The 4L-DEC block diagram is given in Fig.2. Three differential pairs compare the signal D with 3 reference voltages, giving three binary signals (labelled A, B and C), according to the truth table of Fig.2. A logical combination of A, B and C then leads to D1 and D2.



D	A	B	C	D1	D2
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	1	1	0
3	1	1	1	1	1

Fig.2 : Multilevel Detector - Decoder- Decision Circuit

We compared four 4L-DEC versions, based on different logical building blocks; we explicit here D2 decoding, D1 being similarly decoded or more simply equated to B:

# 1 NOR: based on NOR gates: D2 = (A.NOR.Bb).NOR.Cb
# 2 XOR: based on 3-input XOR gate: D2 = A.XOR.B.XOR.C
# 3 MUX: based on MUX (the original idea, by B. Wedding [3], is to use B as the clock)
D2 = A.B + C.Bb
# 4 FOLD: based on a so-called FOLDing architecture (see [4] for details)
D2 = A + C + Bb (with an offset of 1)

4L-DEC version	Max Baudrate (GBd)	Power Dissipation (W)	Complexity (transistor #)
NOR	12	1.5	52
XOR	15	5.5	178
MUX	15	5.5	190
FOLD	16.7	1.2	30

Table 1 : Comparison between 4L-DEC architectures

Table 1 compares the four solutions [4] in terms of circuit complexity, power dissipation and (simulated) bitrate, using the same technology. The FOLD solution appears to be the leading one. XOR and MUX present similar performance but XOR is more sensitive to data delays. We concentrate on MUX and FOLD versions. The first approach uses a selector to multiplex A or C, according to the pseudo-clock B. The second approach is to use an ADC building block, the so-called folding circuit, where current addition is done on a same collector resistor.

3. FOLD and MUX 4L-DEC design

To achieve the high speed needed, we use E2CL logic. Special care has been taken for the layout, to minimize parasitic effects; so we kept the layout as symmetrical (Fig.3) and compact as possible. We used the methodology presented in [5].

Due to the multivalued nature of the input, we are confronted with problems well known in Analog-to-Digital Conversion: in particular, the differential pairs do not switch synchronously, causing glitches and jitter. We found that the MSFFs are capable to reduce the jitter and suppress the glitches. They also have a good retiming feature.

4. Triple Mesa InP / InGaAs DHBT technology and transistor design

The circuits have been processed in CNET in-house non self-aligned triple mesa InP/InGaAs DHBT technology [6]. The transistors used have an Emitter-Base area of 3x8 μm^2; the DC current gain is about 90 at a current density of 40 kA/cm^2; Ft = 56 GHz and Fmax = 43 GHz at Vce=2V; The breakdown voltage BVce0 is about 15V. The technology has two Ti/Au levels of interconnects, thin film resistors and MIM capacitors.

5. Experimental results

The preliminary measurements were done on wafer, and have been carried out with a 4-input (limited to 12.5 Gb/s) ANRITSU data generator whose output can be enhanced up to 25 Gb/s with a NEL selector. At this time, we do not have a 4-level signal generator to fully test the functionnality of the circuits; an encoder has been designed, to allow us to generate such a signal, from to binary streams. Every binary transitions (3-2, ..., 3-0, 2-1, ..., 1-0) present in a four level transmission have been tested. Results are given for the FOLD (Fig.4) and MUX versions, respectively at 16 and 15 GBd, that is 32 and 30 Gbit/s respectively. As it has been expected, it appears that the most critical transitions are 1-2 (D1 and D2 are both changing) and 3-0 (maximal swing). We plan to present more complete results, obtained with multivalued input, at the conference.

As a comparison, a MSFF serial decision circuit was designed and processed at the same time; it has been measured on the same wafer up to 24 Gb/s.

6. Conclusion

We have analysed the architectures for a multi-level decoder-decision circuit used for 4-level ETDM reception. First results were obtained with a Ft=56 GHz / Fmax=43 GHz InP/InGaAs DHBT technology: 16 GBd (ie 32 Gb/s) were achieved. Comparison with the binary format indicates the interest for a multilevel format at high bitrate.

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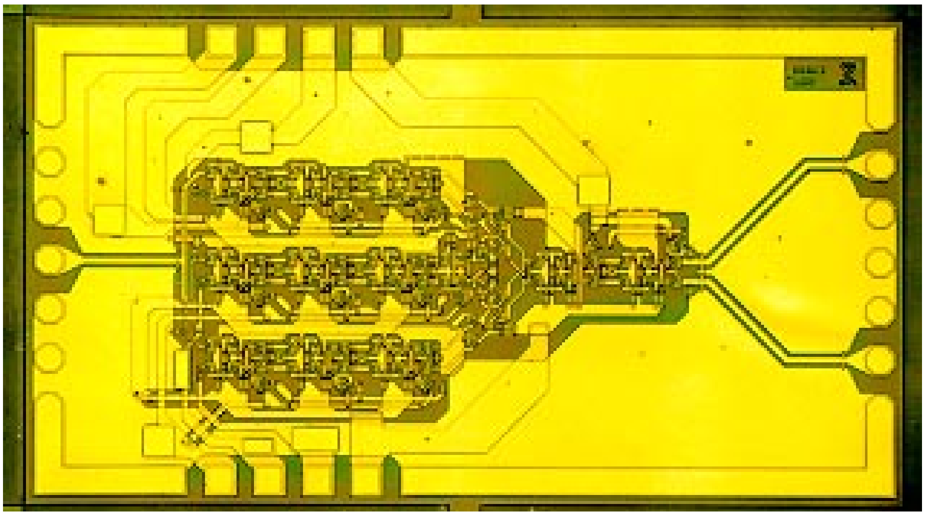
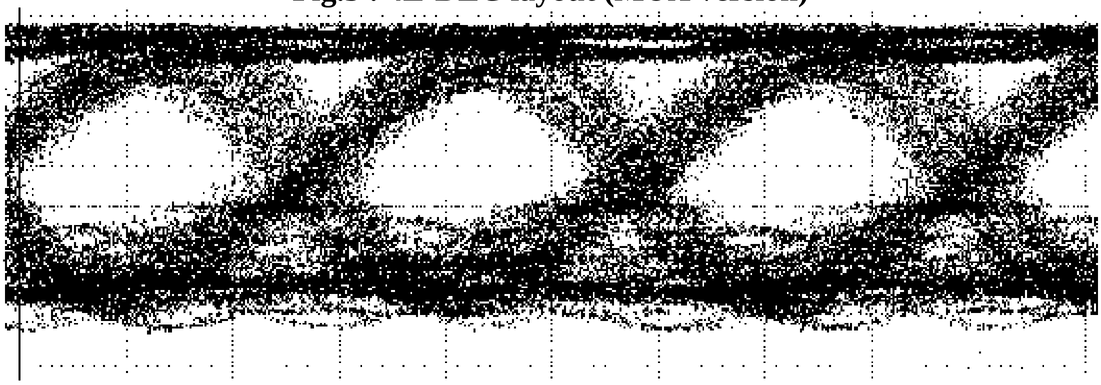


Fig.3 : 4L-DEC layout (MUX version)



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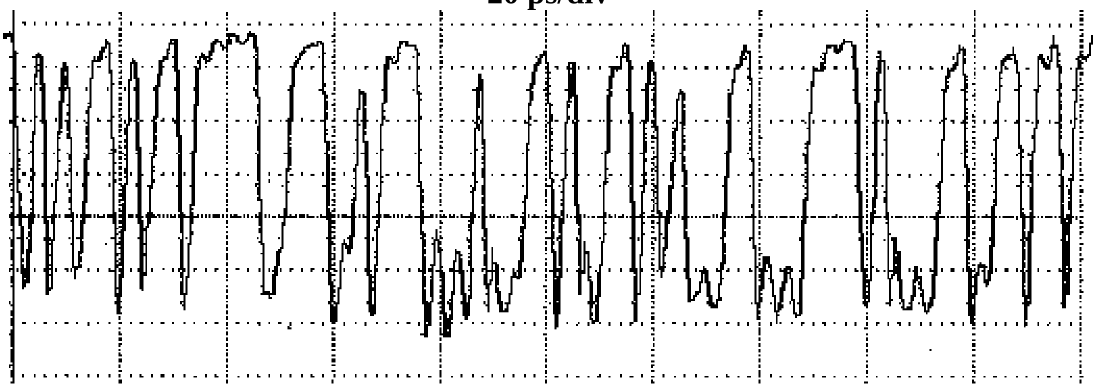

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Fig. 4 : FOLD 4L-DEC 2→1 transition at 16 GBd (output swing : 250 mVpp)