

# New Two Single-Port GaAs Memory Cell

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***Abstract:** This paper presents a new GaAs memory cell with separate read and write single-ports which mixes the principal advantages of the current-mirror and conventional cells implementation. From simulation results, an address access time of 1ns with 20  $\mu$ A/cell power consumption has been achieved. The cell can be operated with single supply voltage of 1V up to 2V.*

## 1. Introduction

With the development of portable telecommunication and multimedia systems, which demand high clock frequency, GaAs logic families are attractive, but low power is also mandatory. Some remarkable progress in power reduction, access time and temperature tolerance of GaAs SRAMs have already been obtained [1][2]. Some of the currently available GaAs MESFET static memories are restricted to small static memories [3][4]. On the other hand high-speed GaAs cache memories are being designed for high-speed GaAs microprocessors which use small amount of on-chip memory in order to exploit the memory hierarchy benefits.

Six transistors conventional memory cell has been usually used to implement static RAM, but this cell presents important limitations when used for GaAs SRAM. Due to the leakage currents, the GaAs memories can suffer destructive read. Several authors have proposed diode or ground shifting techniques to reverse bias the unselected access MESFET [1][5][6][7], in order to limit the leakage current flowing through the access transistors. Other have applied built-in redundancy [8] or current mirror [9][10] techniques to GaAs SRAM [3], but additional control logic or several voltage levels are required thus increasing the complexity and/or the access time.

In this paper a novel high-speed static cell is presented. Good performance and operational margin over a wide temperature range are its principal features. The cell structure and its operation are discussed. The final layout of a test-chip and some simulation results are presented. The basic cell can be used to implement cache memories in high speed systems with sub 1.5 ns requirements. The test-chip including a small memory array, the bit line precharge scheme, I/O circuitry and sense amplifier, was designed and is currently fabricated using Vitesse III - GaAs technology.

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## 2. Memory Cell Structure

The schematic of the proposed high-speed new cell is shown in Figure 1. The cell mixes the advantages of the conventional and current mirror [9,10] cells overcoming some of their respective drawbacks. Source-gate back biasing in the depletion transistors  $M1$  and  $M2$  are used as sub threshold current reduction circuit in order to reduce the power dissipation of the cell. The back biasing is obtained using  $D1$  and  $D2$  diodes. The depletion transistor and diode combination acts as a weak pull-up current supply and must be designed considering the pull-up time requirements, power reduction and the necessary current to compensate the sub-threshold leakage and Schottky currents through the enhancement devices in order to keep the high level in the respective node.

The weak current source formed by  $M1-D1$  must provide a larger current than the  $M4$  and  $M6$  gate to source and gate to drain Schottky inverse currents plus  $M3$  source to drain subthreshold current.. On the other hand, the weak current source formed by  $M2-D2$  must provide a larger current than  $M5$  and  $M4$  subthreshold currents (eq. 3) plus  $M3$  gate Schottky current (eq. 2). All currents depend on the transistor sizes and their biasing voltages. So, the transistor saturation region current (eq. 1) and both direct and reverse diode Schottky current expressions must be considered. The voltages variables in the equations below  $\{U, U_{ds}\}$  are normalised by thermal voltage.

$$I_{ds} = \beta(V_{gs} - V_T)^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (1)$$

$$I_{Sh} = W.L(C2.e^{-U_{ds}}) e^U \quad (2)$$

$$I_{sub} = C1.W.no(1 - e^{-U_{ds}})/L \quad (3)$$

where  $C1 = 2.L_B.q.Dn$   
 $C2 = q.N_D.V$

$no$  - equilibrium minority carrier concentration;  
 $L_B$  - the extrinsic Debye length;  
 $Dn$  - the diffusion constant;  
 $N_D$  - the doping concentration;  
 $V$  depends both drift and diffusion velocities.

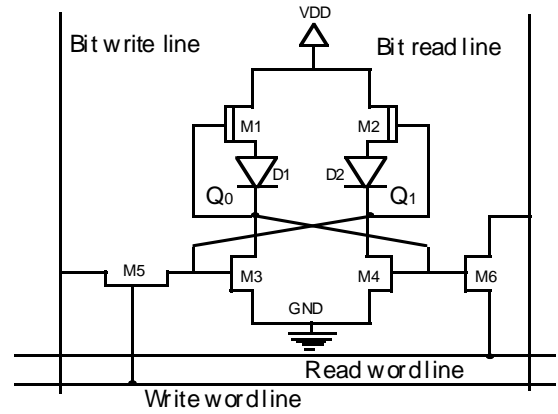


Figure 1. New cell diagram.

The latch formed by the cross-coupled transistors  $M3$  and  $M4$ , provides a robust storage element with reduced static power dissipation. Transistor  $M5$  implement one write-only port, while transistor  $M6$  acts as read-only port. The operation of the RAM is straightforward. The read and write cycles occur on opposite phases of a system clock. The write cycle begin on the rising edge of the clock and the read cycle on the falling edge.

### 2.1. Read operation

The cell is read by pulling down its corresponding read word line to 0V which is maintained at 1 V when no reading operation occur. The other non selected read word lines are held at 1V. In conventional cell during read operation, when the word line level is "low" and the memory cell store "low" data, the leakage currents flows through the access pass transistor, since the bit line level is higher. When the number of cells attached to a column is increased, leakage currents through non selected access transistor can overwhelm the active current of the selected cell. In the proposed configuration the gate-drain and gate-source diodes of the access transistors of non selected cells are reversed biased an appear just as additional capacitances to the storage node, so the above-mentioned conventional cell problem is solved.

Additionally, the access transistor of the selected cell cannot inject current into the storage nodes giving a non destructive read operation. Unlike conventional cell, the access transistor can be dimensioned independently of the transistor of the driver. If the cell stores a high value at the internal node  $Q_0$  and the read word line is lowered to 0v, a saturation current flows through  $M6$  transistor pulling down the bit read line which must be precharged at 1V before each read operation. If the cell

stores a low value at  $Q_0$ , no significant current appear through the access transistor and the precharged bit read line value is held.

## 2.2. Write operation

The write operation is similar to the one of a conventional six-transistor cell, data is placed on the bit write line and the write word line is raised, the cross-coupled transistors force the internal nodes to change to appropriated voltage levels maintaining the state of the cell. In order to obtain a high speed write operation, the access transistor  $M5$  must be dimensioned according to the  $M3$  pull down transistor. Usually, a ratio of  $M3 = 3 * M5$  is required. To write a low level, the low voltage bit write line is connected through the  $M5$  pass transistor to the cell storage node  $Q_1$  pulling that storage node low and causing the opposite cell storage node  $Q_0$  to be driven high. In order to write a high level, it must be guaranteed that  $V_G \geq V_i + V_T$  if  $V_{BL} > V_i$ , where  $V_G$  is the gate voltage of access transistor,  $V_{BL}$  is a bit line voltage level and  $V_T$  is the threshold voltage,  $V_i$  would be the internal storage node. Using the mentioned voltage levels the write operation is reliable.

Reading data from the cell involves discharging the bit read line through the  $M6$  access transistor. Transferring data from the bit write line to the cell involves discharging the storage node through the  $M5$  pass transistor. The resistance of the channel of a transistor is a non linear function of the drain source voltage and is given in the region of operation by:

$$r_{ds} = \cosh^2(aV_{ds}) / b.a. (V_{gs} - V_t)^2 \quad (4)$$

As the voltage drop across  $r_{ds}$  is reduced, a lower channel resistance is obtained. For cell currents between 10 and 20  $\mu A$ , this writing mechanism is faster than the writing mechanism used in full mirror cells [3]. Unlike the reported full mirror cell, no multiple diodes are present in the writing path, the cell grounds does not have to be driven so less control circuitry is required. In this new cell, only a single voltage supply of 1V to 2V is used. The memory cell designed presents good stability and access speed. Figure 2 shows the noise margins of the MESFET new cell.

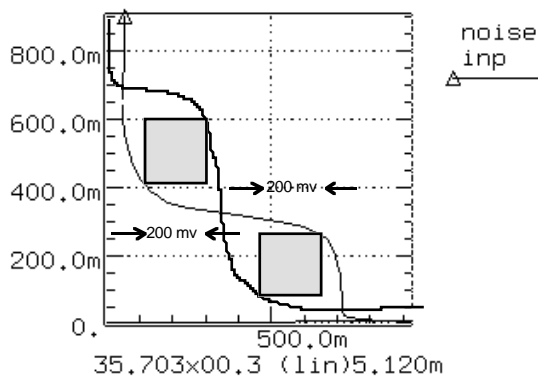


Figure 2. Noise margins

Table I. Memory cell performance.

Technology	0.6 $\mu m$ - GaAs
Cell Structure	8-devices, 2 single-port
Memory Cell Size	35.9 x 36.9 $\mu m^2$
Access Time	1 ns
Min. Write Pulse	150 ps
Power Supply	1 v
Cell Current	20 $\mu A$
Read Time	760 ps

## 3. Simulation results

From simulation results the total cell read and write access times were found to be 760 ps and 150 ps respectively. An active current of 20  $\mu A$  (at 1Ghz) was obtained so the total power dissipation of the 1 Kb core memory operated at 1V would be 20.5 mW. The cell area is 36 x 37  $\mu m^2$ . A global write and read access time of 1 ns was measured from the input to the output buffers. The read access time is longer than the write access time because of the regeneration process necessary to amplify the small bit line voltage difference to full voltage swing. A summary of the memory cell performance is given in table I. In figure 3, the test-chip layout is presented. In figure 4, the address input and data output waveform for a read cycle at different temperatures of the memory cell are shown.

## 4. Conclusion

A novel memory cell structure has been developed to implement static on-line RAMs in GaAs technology. The new cell present low power dissipation and high operating speed. The small RAM test-chip was designed and currently fabricated using Vitesse III - GaAs technology.

By the improvement of the structure an address access time of 1 ns with a power dissipation of 20  $\mu$ A/cell has been obtained. The cell operates at only supply voltage of 1V up to 2V. Using a low power address decoder DDM [11], the proposed cell can be easily used in implementing high-speed cache RAMs.

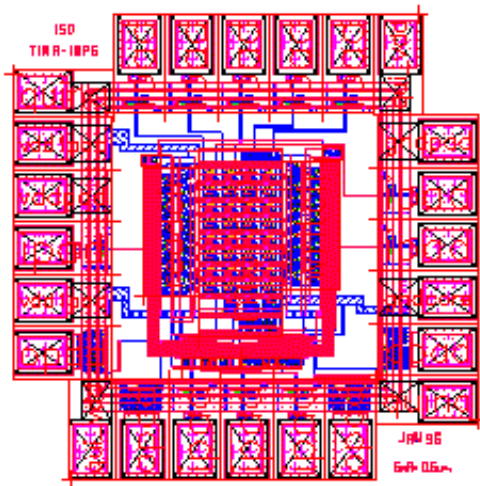


Figure 3. Test-chip layout.

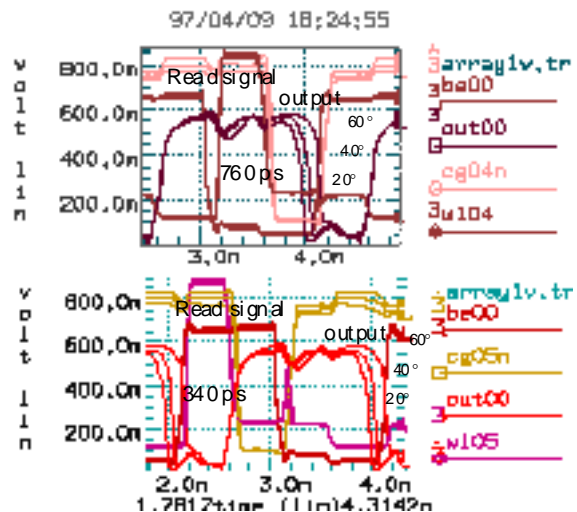


Figure 4. "0" and "1" logic read operations.

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