A 2.1 MHz Crystal Oscillator Time Base with a Current Consumption under 500 nA

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1. Introduction

For a very accurate low power time base, a 2.1 MHz ZT cut quartz crystal [1] offers drastically improved performance, with respect to standard 32 KHz quartz resonators used in watches. Improved features are: temperature stability better than ±2 ppm between -10 °C and 70 °C without compensation, shock sensitivity and long term drift reduced by at least an order of magnitude. The very low power time base using this quartz includes following features:

A micro-power circuit is encapsulated with a 2.1 MHz ZT-cut quartz in a vacuum package. The oscillator core has 2 complementary active MOSFETS and amplitude stabilization. New coupling and biasing circuits, and dynamic frequency dividers allow to achieve ±2 ppm frequency stability down to 1.8 V with a current under 0.5 µA.

- A vacuum encapsulation holds together the quartz and a high frequency chip, as in [1]. This module has only two pins and the case connection. It is powered by a 3 V lithium battery.

- A new circuit combines a systematic choice of minimum power techniques, including significant original contributions. This paper describes in more detail the means to achieve a current drain below 0.5 µA. The circuit comprizes oscillator, frequency dividers, frequency tuning with a resolution of ±3 sec/year (±0.1 ppm), and auxiliary circuits. A single output delivers a signal of 16384 Hz. The high frequency quartz works continuously, dispensing with an additional low frequency crystal and periodic calibration as in [1].

2. System

The main blocks are shown in Fig. 1. Oscillator current is minimized by amplitude control [2] and by using 2 active MOSFETs [3, 4]. Separate capacitive coupling with the n- and the p-inputs of the first frequency divider stage, as in [3], eliminates any active interface. A dynamic frequency divider by 4 is the best compromise for a minimum overall power consumption. An inhibition circuit is the front-end part of the digital tuning system. It removes a fraction of the transitions to obtain exactly the required average frequency. For a resolution of 0.2 ppm, a given number of pulses at 524 kHz must be suppressed within each period of 10 seconds. A buffer delivers a 16 kHz signal to the output pin. In order to save power consumption in the divider chain, this part of the circuit is powered by a reduced voltage, whose value tracks the process parameters. A current source controls the bias of these various sub-blocks. For the test circuit, the elements of Fig. 1, which are the most power consuming, have been integrated in a 2µm CMOS process. In a further development, the inhibition control circuitry and a bi-directional output interface will be added.

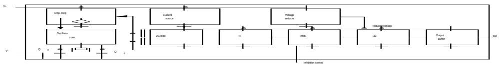

Fig. 1. Block diagram of the high frequency part of a low power time base.

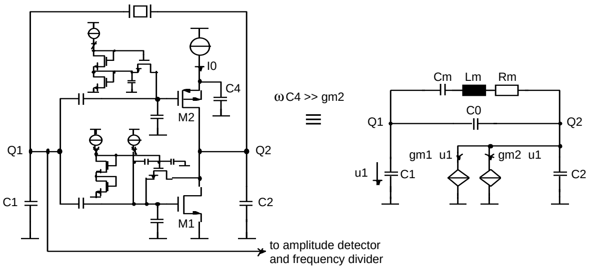

Fig. 2. Quartz oscillator diagram, and equivalent circuit.

3. Oscillator

The oscillator diagram is shown in Fig. 2. It is based on the well known Pierce structure [2]. MOS transistors M1 and M2 are biased by the same current I_0, while their transconductances add up. Capacitor C_4 smoothes the source voltage of M2. In the equivalent circuit of Fig. 2, the quartz has been drawn as a series resonant circuit, with series resistance R_m, and additional stray capacitance C_0. The critical transconductance needed to sustain the oscillation can be calculated with the following formula

$$g_{mcrit} \approx (2\pi f_0)^2 R_m \frac{(C_1C_2 + C_0(C_1 + C_2))^2}{C_1C_2} + \frac{C_2}{C_1} g_1 + \frac{C_1}{C_2} g_2$$

where f_0 is the resonant frequency, C_1 and C_2 are the branch capacitances, g_1 and g_2 their respective stray conductances (losses). To minimize the critical transconductance and thus the current consumption, all capacitances must be minimized. C_1 and C_2 are functional elements and also influence the exact operating frequency. Their values are typically 2.5 pF. The 2.1 MHz ZT quartz has a parasitic capacitor C_0 = 0.7 pF and its equivalent series resistance R_m ranges from 165 to 550 ½ (typically 210 ½). Accounting for the dispersion of all components and adding the contribution of realistic losses, the critical transconductance is in the range 0.5 to 2 µS (typically 0.75 µS). The vacuum package minimizes parasitic capacitances and conductances in parallel with C_1 and C_2, and thus contributes significantly to reduce the power consumption.

The oscillator bias current I_0 is a function of the peak voltage amplitude at node Q1. This peak amplitude has been chosen as 0.2±0.05V. It is well controlled by the amplitude regulator. The typical consumption of the oscillator core is about 60 nA and the maximum is 180 nA.

4. Frequency Divider

The sine wave delivered by the oscillator is separately coupled by capacitors [3] to both inputs of the frequency divider by 4 (Fig. 3). This technique eliminates any interface amplifier, which would consume at least 150 nA.

This frequency divider has separate DC biased p-MOS and n-MOS gate inputs. In absence of input signal, the circuit acts like a ring oscillator, whose frequency is controlled by the input DC levels. When this free running frequency is near the oscillator frequency, the divider synchronizes even for a small oscillation amplitude. A certain amplitude has to be guaranteed in order to allow for current and process variations (Fig. 4).

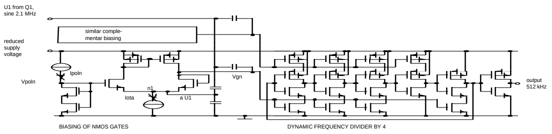

Fig. 3. Frequency divider first stage with input interfaces.

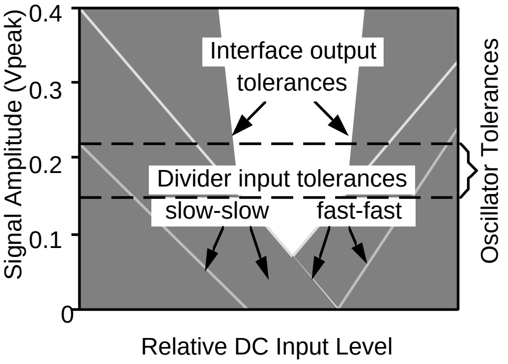

Fig. 4. Input and output tolerances for the interface.

The DC bias at the divider n-MOS input is provided by an original circuit (Fig. 3). Vpoln is the ideal DC level. By careful compensation of non-linearity, the amplifier delivers the same level at Vgn for large signal amplitudes. Capacitive coupling of node n1 provides dynamic compensation. A corresponding circuit provides the DC bias to the p-MOS input. These circuits are much better than high value resistors, with respect to area and stray capacitance. Correct frequency division is guaranteed in worst case situations with respect to process variations, in an amplitude range between 0.15 V at -10°C and 0.22 V at +70°C. This is compatible with the oscillator signal.

5. Circuit Realization and Results

This circuit has been integrated in a standard 2µm CMOS process. Table 1 summarizes the main measured results.

		Min.	**Typ.**	**Max.**	**Unit**
Current:	Total current consumption	390		455	nA
	oscillator with regulator	50		60	nA
	Freq. dividers and inhibition	295		340	nA
	biasing circuits	45		55	nA
Frequency:	Freq. sensitivity to supply voltage		0.04		ppm/V
	Resolution of digital tuning			0.19	ppm
Start-up:	Start-up time	26		48	ms

Table 1. Measured characteristics over the whole temperature and supply voltage range (-10 to +70°C and 1.8 to 3.5 V)

The total current consumption of the module is lower than 500 nA at 3 V. 75% of this current is used for frequency division, whereas the oscillator only consumes 15% of the current. Assuming extreme process parameter and temperature variations, the worst-case calculated current consumption is 650 nA. Despite this low power, the module exhibits excellent frequency stability. Temperature dependence of the output frequency is the same as the stand-alone quartz (Fig. 5). Frequency sensitivity to supply voltage is very low. A start-up time under 50 ms is observed.

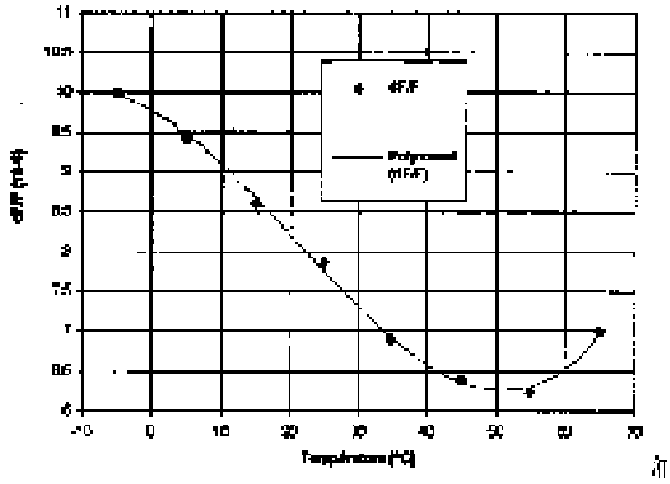

Fig. 5. Measured temperature-frequency characteristics of the oscillator working with a ZT-cut quartz crystal.

The active area of the chip is 0.41 mm^2 (Fig. 6).

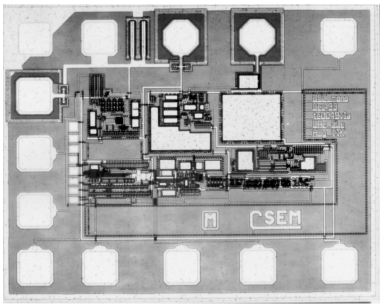

Fig. 6. Test chip photography. Active area of the chip is 0.41 mm^2.

In future developments, sub-micron technologies will allow further area and power savings, mainly for the frequency dividers. A higher crystal frequency would still be compatible with low power, leading to a smaller quartz and a smaller module.

This development shows that a highly accurate time base with sub-microampere current drain can be implemented in a single package.

References

[1] D. Lanfranchi et al., "A Microprocessor-Based Analog Wristwatch Chip with 3 Seconds/Year Accuracy", ISSCC’94, WP 5.6, pp. 16-18, February 1994, San Francisco.

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[4] L. L. Lewin et al., "CMOS Oscillator Subsystem Optimized for Minimum Power Consumption", ISCAS, 1983.