

MHITIC: 8-Channels, 1-ns, Multi-Hit Time-to-Digital Converter CMOS Integrated Circuit

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Abstract

A CMOS 8-channel, 1 ns bin size, 23 bit dynamic range multi-hit time-to-digital converter is presented in this paper. A new architecture mixing two previous TDC realizations has been adopted. The chip stores up to 32 events per channel with a double-hit resolution of 16 ns. A prototype of about 120 mm² has been integrated in a 1 μ m process. Test results show that performance, in particular linearity, better than those of comparable devices has been achieved.

Introduction

A TDC (time-to-digital converter) is a system which gives the timing of the occurrence of an event (hit) on a measuring channel. Usually, the measurement is relative to a reference instant, for example an event collected on a reference channel, so that the readout of the TDCs is the difference between two measured absolute values (common-start or common-stop operation). TDCs are widely used as precision time measurement instruments in many applications, such as laser ranging or high energy physics experiments, to measure drift time in drift chambers [1]-[4].

A way, more complex but less expensive than fast technologies such as ECL or GaAs to obtain a high resolution TDC, is the adoption of CMOS technology special circuits and techniques, such as phase-locked loops. CMOS TDCs with subnanosecond bin size have been reported in literature [1]. A TDC can be composed of a synchronous coarse counter working at a frequency f_{max} , the resolution of which is augmented by means of asynchronous networks, a 4 state interpolator in [2], or a 16 stage delay-locked loop of delay elements in [3].

The hit appearing on one of the measurement channels samples the content of this augmented-resolution counter, and the sampled value is stored together with other information (channel number, sign of the transition, etc.) in a FIFO, to be eventually processed and readout. The major theoretical drawback of this approach is that a new event cannot be recorded until the previous has been processed and the double-hit resolution (i.e. the capability of resolving two consecutive hits) is limited to a value independent of the bin size of the TDC itself [2].

An alternative approach to overcome this problem is exchanging the role of clock and input: a delay-locked chain, alike that of [3], is now used to generate a set of delayed signals, that sample the input in successive instants, each one delayed from the preceding $t_{min} = (1/f_{max})/2^M$, where 2^M is the number of the stages of the delay chain. In this way, a kind of “photograph” of the input signal during the clock period is taken and the double-hit resolution is thus theoretically equal to the bin size. On the other hand, this approach requires a huge amount of memory to store all the successive acquisitions of the input, even those with no interesting features [4].

The original solution we propose is mixing the two approaches. The second input sampling method is adopted, since it extracts more information from the signal, but the results of the sampling are immediately analyzed and the presence of one or more hits is recognized and encoded with the minimum number of bit. The aim of the work has been realizing a CMOS TDC capable of recording multi-channel multi-hits, on a wide dynamic range with a bin size equal or better than 1 ns.

The Architecture

Given the basic idea reported above, let us briefly describe the architecture of this TDC chip and the most significant parts of the design. The complete architecture is shown in Fig. 1.

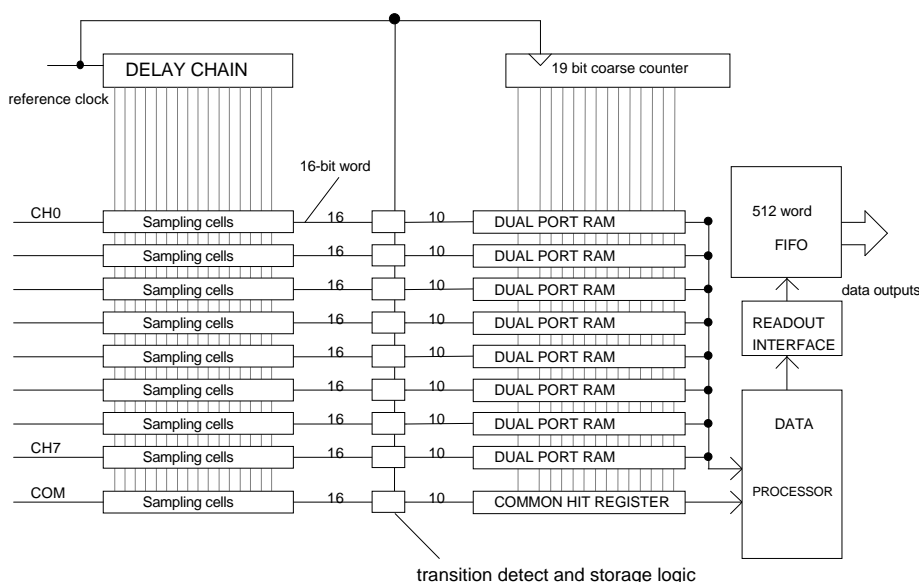


Fig. 1: Block scheme of the TDC architecture.

The input signals (coming from the 8 channels and from the common one) are sampled by the 16 clocks generated by the controlled delay-line and produce a 16-bit word. This word is the result of the 16 high-resolution samplings performed on the input signal and thus contains the information on the occurrence of a transition, within the main clock period. The sampled data then enter a block which extracts the information regarding the presence and the type of the transition (leading edge, trailing edge) revealed on the relevant channel. These data are encoded to minimize the number of bit used and then stored in a dual-port RAM, together with the content of the coarse synchronous counter, only if a hit has been detected. Therefore, each channel RAM only contains the data pertaining the occurrence of a hit on that channel.

The post-processing and read-out interface consists of a data processor where the data from the common hit register and the channel RAMs are subtracted each other, and a FIFO where valid data are stored, in order to be read from the outside. The sign of the result is chosen according to the operating mode, i.e. common start or common stop. The read-out sub-system implements the automatic zero skipping of the empty channels, by means of a priority encoding scheme. This

solution is extended to build a multi-chip TDC system, because only those chips with valid data are searched.

The controlled delay-line and the sampling system are the most critical parts of the design. They set the operation limit of the TDC and have therefore been designed with a careful full-custom analog-digital approach. The delay line consists of 16 buffers, the currents of which are regulated by a current-starving series transistor, like in [3]. A very accurate design, extensive electrical simulations and prototypes have been realized, in order to guarantee the correct behavior of this part in the whole range of temperature, process shift and supply voltage. It is worth stating that the delay can be controlled down to 500 ps per buffer, and the system can thus operate as a 2 Gbit/s sampler.

The channel RAMs and the coarse counter are more common blocks that must operate at f_{max} . They have thus been designed with a semi-custom approach, by taking into account the specifications on the maximum number of hit per channel (sets the RAM dimension) and the dynamic range of the TDC (sets the width of the counter). The rest of the circuit (read-out interface, etc.) does not present particular design problems and therefore consists of semi-custom logic and a FIFO, the dimension of which sets the maximum number of hits recorded per chip.

Test Results

An experimental prototype of this multi-hit TDC has been integrated with the ES2 CMOS 1 μm process and tested. The chip which size is $11.3 \times 10.5 \text{ mm}^2$ works up to a maximum frequency of 65 MHz (0.962 ns bin size).

A CAMAC board containing 4 chips (32 channels) connected in a daisy chain has been realized to measure the system performance. Some experiments to measure the differential non linearity (DNL), the integral non linearity (INL) and the standard deviation (Std. Dev.) have been performed at a reference clock of 62 MHz (1.008 ns bin size). The worst-case maximum power dissipation, during a continuous acquisition, has been 800 mW (100 mW/channel).

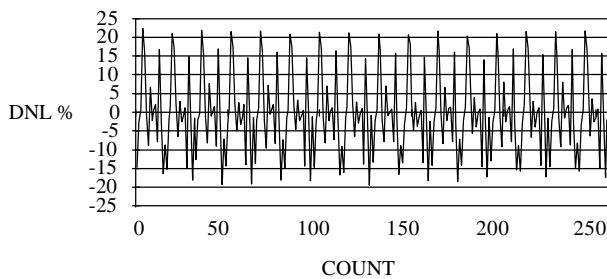


Fig. 2a: DNL measured with data processor disabled.

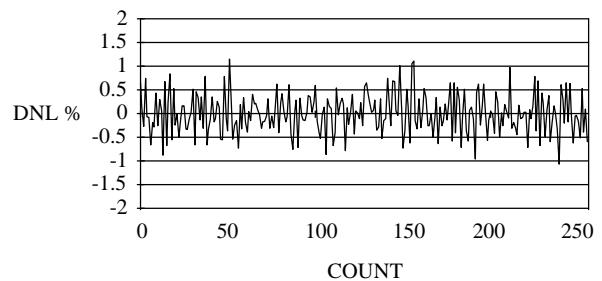


Fig. 2b: DNL measured with data processor enabled.

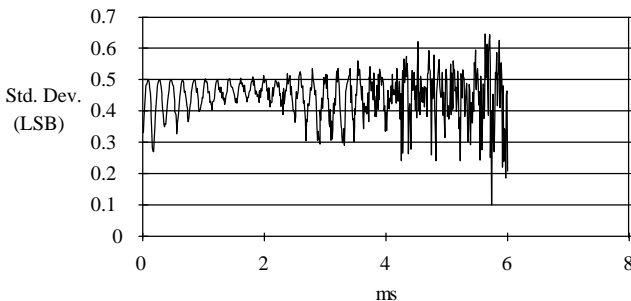


Fig. 3a: Std. Dev. measured with step of 1 μs .

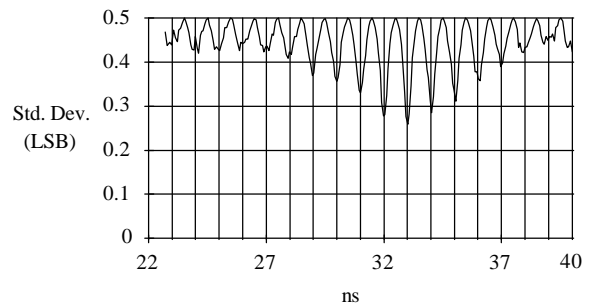


Fig. 3b: Std. Dev. measured with step of 70 ps.

The DNL is caused by the mismatch in the delay-line stages and by the different paths from the line itself to the sampling system, which produce a non uniform value of the bin size. DNL has been measured on a single channel, over a dynamic range of 8 bit in common start mode, with the channel hits and the start signal completely asynchronous each other. A statistical averaging method

has been used to obtain a detailed and accurate measurement of DNL, by sending for each time bin a very high number of hits (40,000÷50,000) not correlated to the system clock. The data read by the TDC has been plotted in a histogram, the flatness of which is a direct measure of the DNL.

Two experiments have been performed with the data processor disabled (no subtraction with the common start/stop register) or enabled. In the first case (Fig. 2a) DNL ranges from -20% to $+20\%$ and it shows, as expected, a periodical structure with period of 4 LSB (16 ns). This confirms that DNL is mainly due to the mismatch of the delay-line which produces just the 4 augmented LSB of the output word and its non uniformity is repeated every 16 counts (1 LSB of the coarse counter). Fig. 2b shows that the DNL value is from -1% to $+1\%$, when subtraction is enabled.

The INL has been measured over a dynamic range from 0 to 6 ms (almost the TDC full range) and it has been calculated using a least square fit method. A CAMAC programmable gate generator (CAEN Mod.C423) has been used to generate time intervals with step of $1\ \mu\text{s}$ and 2,000 measurements per interval have been performed. The INL ranges from -0.1 LSB to $+0.2$ LSB.

The theoretical value of the standard deviation only depends on the quantization error in an ideal TDC and ranges from 0 to 0.5 LSB. The Std. Dev. values are reported over two different time intervals: from 0 to 6 ms with step of $1\ \mu\text{s}$ (Fig. 3a) and from 22 to 40 ns with step of 70 ps (Fig. 3b). 2,000 measurements have been performed also in this case.

The results show that Std. Dev. is always within the theoretical limit of 0.5, except for intervals above 4 ms. This shows the excellent performance of the TDC on the whole dynamic range, specially if we mention that the experimental set-up introduces a non negligible error just above that value. Fig. 3b shows that Std. Dev. has a periodicity equal to the bin size, as expected and the time resolution defined as the standard deviation of the error distribution is 0.443 LSB, better than comparable devices [1], [2], [4].

Conclusions

A custom integrated circuit to be used as a multi-channel TDC has been described in this paper. This chip uses a novel architecture, that allows a significant improvement of the performance with respect to other solutions, in particular for linearity, double-hit resolution and dynamic range. The main features are: 8 channels per chip, wide dynamic range larger than 8 ms full scale, 1 ns least count, 500 ps RMS, 0.443 LSB time resolution, double-hit resolution better than 16 ns, differential non linearity less than 2%, integral non linearity less than 0.2 LSB, selectable common start or common stop mode, 32 hits per channel, leading/trailing (or both) edge recorded, 512 hit deep read-out buffer, and the sparse read-out of a multiple chip system.

The chip can operate at a frequency of 65 MHz with a bin size of 0.962 ns with a worst case power dissipation of 100 mW/channel and it is going to be produced and used by CAEN for the realization of commercial multi-channel measurement modules.

References

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