

# VHDL timing model for CMOS semicustom branch-based logic cells

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## Abstract

This paper presents a model for characterizing delay in semicustom CMOS logic cells that accounts for input slew rate and output capacitance loading. The logic cells are decomposed into branches of series connected transistors. A method for deriving the model parameters and VHDL modeling of the branches is presented. This method drastically reduces the number of model parameters required for delay characterization.

## 1 Introduction

Analog circuit simulators suffer from severe memory and execution time constraints and are hence unsuitable for VLSI circuits. Logic and timing simulators are much faster, but their accuracy depends upon the accuracy of the model for cell delay. In order to obtain a good accuracy, the dependence of CMOS cell delay upon both input slope (IS) and output load must be taken into account. A input slope dependent timing model for characterizing delay in CMOS logic gates was presented by Misheloff in [1]. In order to reduce the number of parameters for delay characterization, we decompose the CMOS cells into branches of series connected transistors, and characterize the branches rather than the entire cell. The concept of branch-modeling schematics is detailed in [2]. The main advantage is the construction of simulation models for the cells. As each cell is constructed with branches, it is possible to describe a model for each different branch to obtain the corresponding model of the complete cell. The number of models to develop is therefore drastically reduced and simplified: the different branches present 1, 2 or 3 transistors in series, for both n-branch and p-branch networks [2]. The very long work of designing dedicated models for each cell is therefore avoided.

Our characterization is based on piece-wise linear fitting of the delay model parameters to a number of Spice3 simulations. The model parameters for each branch are derived from Spice simulations of the netlist based on cell's layout using lateral interconnect capacitance. Level-3 transistor model is used. The number of transistors in series has been limited to 3 for both n- and p-branch type.

## 2 Input Slope Delay Model of the branch

Misheloff's characterization [1] is based on the observation that CMOS logic gates present two different modes of switching – named *FAST* mode and *SLOW* mode – which depend upon the relative values of the input slope and output capacitive load ( $C_L$ ). Our model is based on the observation that branches of p-transistors/n-transistors which charge/discharge a capacitive load also present fast/slow operation mode. In order to introduce the branch delay model we consider a circuit made of 2 branches, presented in Figure 1(a), and compare the output switching in both fast and slow cases.

Figure 2(a) plots the output slope (OS) versus the input slope (IS). The plot data were obtained from Spice3 simulation, the test circuit was implemented in Sea-of-Gates<sup>1</sup>.

From Figure 2(a) the following features are evident: 1) the critical input slope (CIS) separating the fast and slow regions depends linearly on the output load; 2) inside the slow region: for fixed load, OS is independent of IS; for fixed IS, OS depends linearly on load; 3) inside the slow region OS lines have all the same slope.

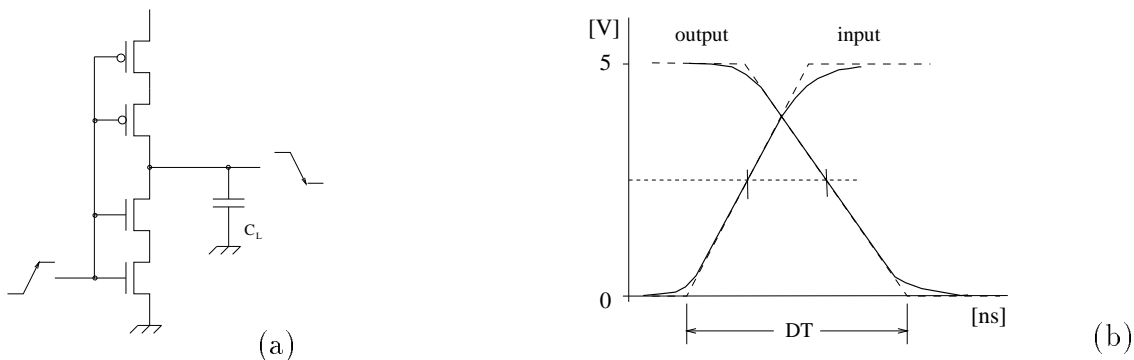


Figure 1: Test circuit made of branches (a), definition of DT (b)

The basis for the two modes of operation are explained as follows: the output is switching in a fast mode when the input is completely settled before the output starts switching. When this is the case, only one branch is conducting current while the output is changing. The OS and output delay depend only on the capacitive load and saturation current of the transistors, and are independent of the input slope. In the slow switching mode, i.e. long input transition time, the input is still changing when the output switches. In this case both branches are conducting current while the output is changing. For large input slopes the output voltage follows the DC characteristics of the circuit.

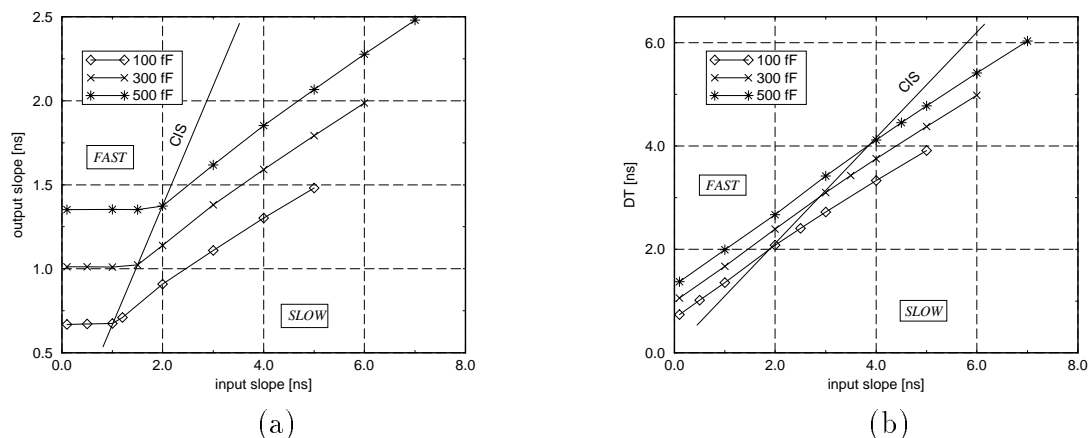


Figure 2: Output slope vs. input slope for 2n-branch (a), DT vs. input slope for 2n-branch (b)

Due to the fact that output delay plot is not linear inside the slow switching region, another geometric quantity named *delay time* (DT), represented in Figure 1(b), is selected for a piece-wise linear approximation. The 50% delay can be expressed from DT, IS and OS as

$$Delay = DT - \frac{IS}{2} - \frac{OS}{2} \quad (1)$$

Other delays than 50% delay can be as well derived, for example, the 40% delay would be  $Delay_{40\%} = DT - 0.4 \cdot (IS + OS)$ .

<sup>1</sup>Sea-of-Gates - 1.6  $\mu\text{m}$  semicustom CMOS process with two layers of metal used at TU Delft.

Figure 2(b) shows DT versus IS plots for 2n-branch for several loads equally distanced. Due to the fast and slow regions separation, OS and DT can be described by two linear functions, one for the fast region and the other for the slow region. The two functions are equal on the fast-slow boundary determined by CIS. Our model to estimate the OS is given by

$$OS = \begin{cases} a + b \cdot C_L & \text{when } x \leq x_p \quad (\text{fast mode}) \\ c + d \cdot C_L + m \cdot IS & \text{when } x > x_p \quad (\text{slow mode}) \end{cases} \quad (2)$$

where  $x_p$  is a linear function on the output load given by

$$x_p = \frac{a - c}{m} + \frac{b - d}{m} \cdot C_L \quad (3)$$

and  $a, b, c, d$ , and  $m$  are OS parameters.

The piece-wise linear approximation for DT is given by

$$DT = \begin{cases} a + b \cdot C_L + m_1 \cdot IS & \text{when } x \leq x_p \quad (\text{fast mode}) \\ c + d \cdot C_L + m_2 \cdot IS & \text{when } x > x_p \quad (\text{slow mode}) \end{cases} \quad (4)$$

where

$$x_p = \frac{a - c}{m_2 - m_1} + \frac{b - d}{m_2 - m_1} \cdot C_L \quad (5)$$

and  $a, b, c, d, m_1$ , and  $m_2$  are the DT parameters.

### 3 Branch Switching Particularities

Branch-logic schematics together with branch switching mechanism present some particularities which allows us to reduce the number of characterization parameters and to include the influence of the capacitive loading of the internal nodes into the cell delay. These characteristics are summarized below:

- 1) Due to the fact that the branch is made of series connected transistors, the branch maximum current is limited by the weakest conducting transistor (in semicustom design all transistors have the same size). In other words, the slowest input slope of the series transistors dominates.
- 2) Some delay parameters of the branches are independent of the branch size and depend only on the branch type and on the CMOS process. For example:
  - for OS:  $m$  parameter in eq. (2) is the same for all branches.
  - for DT:  $m_1$  and  $m_2$  parameters in eq. (4) are the same for all branches.
  - parallel connected branches switching in the same time behave like an equivalent branch which has the parameters  $1/a_{ech} = 1/a_1 + 1/a_2 + \dots + 1/a_n$  and  $1/b_{ech} = 1/b_1 + 1/b_2 + \dots + 1/b_n$  for both OS and DT equations (the same formula form parallel connected resistors).
- 3) A branch connected to an internal node adds a capacitive load to the node. When the top branch transistor is in cut off, the capacitance which is added is determined only by the drain capacitance. If the top branch transistor is in saturation and the adjacent one is in cut off, the added capacitance includes also gate-channel capacitance and source capacitance.

### 4 VHDL Implementation

Our VHDL simulator (*VantageSpreadsheet* version 5.015) simulator cannot handle signals of type record (a bug!), and consequently two separate signals – namely *value* and *slope* – have been used to model a physical wire in our VHDL descriptions.

The interface aspect of the 2n-branch is presented in Figure 3(a). Two auxiliary signals named *wcap* (wired-capacitance) and *ps* (parallel-switching) are added to the branch to capture the capacitance variation of the internal node and to adapt the branch parameters for simultaneous switching of parallel connected branches. All VHDL models are compilable with IEEE 1164 standard. A new function, called *resolve\_branch* is used to resolve the wiring together of the branch outputs. The diagram of the function strength states is presented in Figure 3(c).

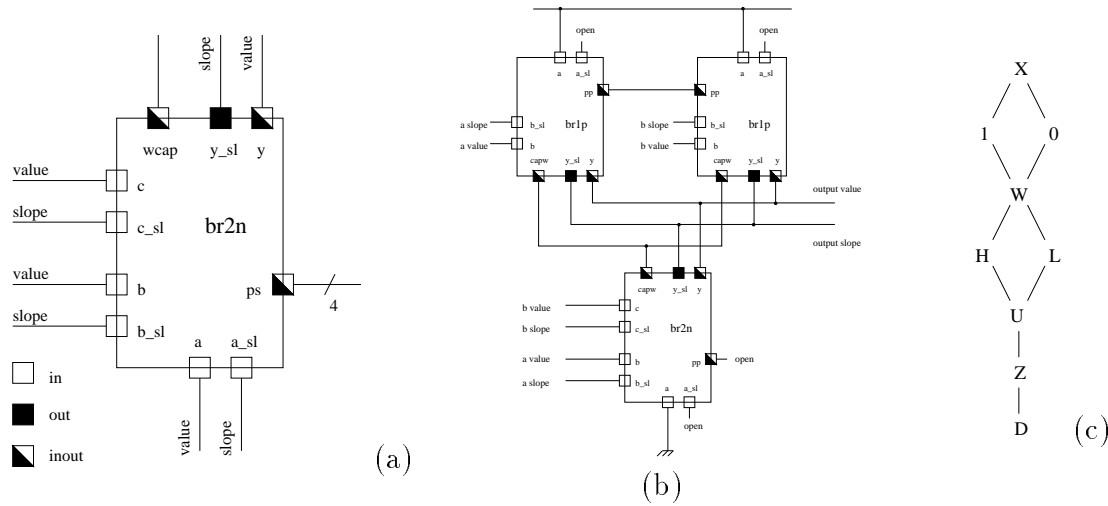


Figure 3: Interface aspect of 2n-branch (a), example of nand2 gate (b), resolving\_branch diagram (c)

## 5 Results and Conclusions

Table 1 presents the amount of CPU time needed to simulate a chain of 1000 nand2 gates on a HP 735/9000 machine. Two different models were used for the nand gate: a simple delay model (e.g.  $y \leq a \text{ nand } b \text{ after } X \text{ ns}$ ), and a nand gate modeled with branches.

	simple delay model	Branch modeling	Spice3
CPU time	0.15 sec	1.533 sec	55 min*

Table 1: VHDL simulation CPU time for a chain of 1000 nand2 gates (55 min\* - estimated time)

When branch-logic style is used to model the nand gate the simulation time increases, but remains negligible compared to Spice simulation time.

We have presented a method for characterizing delay in semicustom CMOS cell that accounts for input slope and output load. The method requires a low number of parameters for delay characterization, and allows delay simulations to be carried out at VHDL simulation speed.

### References

- 1). M.N. Misheloff, "Improved Modeling and Characterization System for Logic Simulation", Proc. of the IEEE Asic Intl. Conference, 1992.
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