A Current Mirroring BiCMOS Comparator for Low-Voltage, Low-Power Applications

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Abstract

A novel comparator, featuring 8bit resolution, 160Ms/s at 3.3V supply, was designed and tested. By the use of BiCMOS technology, it overcomes the limits of the conventional bipolar circuits, in terms of reduced power consumption and supply voltage. Test results, obtained with both classical and statistical techniques, are reported.

1 Introduction

The design of the latched comparator is a key element for the development of A/D converters (ADC) with high sampling frequency and analog bandwidth. The classical bipolar latched comparator [1], no longer seems the best solution in the perspective of reducing power consumption and supply voltage. This paper discusses the implementation, in a 1.2um BiCMOS technology [2], of a novel comparator featuring a maximum sampling frequency of 160MHz, 8 bit resolution on a ±0.5V differential input range, a supply of 3.3V ±10% and very low kickback noise. Test results obtained with both classical and statistical techniques, are discussed.

2 The Current Mirroring comparator

The classical bipolar latched comparator, widely used in high-speed, medium-high resolution converters, exhibits a significant kickback noise, since the bias current of the input transistors is periodically switched off. [3]. In a flash converter, this disturbance is injected into the resistive ladder, and thus degrades the effective resolution. In order to attenuate the disturbance, the inputs of the comparator are commonly buffered by followers. This, however, increases power consumption and is not compatible with the scaling down of the supply voltage (so much the more if differential input adapters [4] are required), since the designer is forced to use only npn BJTs in the input stages for offset and speed constraints. Moreover, analog bandwidth on one side and regeneration speed and output swing on the other pose conflicting requirements on the load resistance and the desired dynamic performances can be achieved only at the expense of the power consumption. Other low-kickback solutions, like the "high clocking" architecture [3], cannot be easily adapted to reduced supply voltages.

The proposed **current mirroring latched comparator**, fig.1, converts the differential input voltage into a difference of the currents flowing through M1-M2. By the action of mirrors M1-M3 and M2-M4, this current difference unbalances the latching stage which regenerates, for ck low, the initial output voltage, while the reset operation is granted by pass transistors MP1-MP2 for ck high. Since input transistors are biased during the entire clock period, this comparator exhibits a very low kickback noise. Fig.2 shows that, for equal supply voltage, clock frequency and input voltage, the kickback disturbance introduced by the conventional comparator, with emitter followers at its inputs, is much higher than the disturbance of the proposed comparator, even without input followers.

As for the latch, high speed and low power consumption are achieved thanks to the high small-signal resistance of the load and to the absence of any limitation of the discharging currents available at the outputs. A summary of specifications of the complete latched comparator is reported in tab.I. The supply current of 80μA should be compared with the 180μA required by the conventional comparator, with the same technology, for achieving the same sampling frequency. Fig.3 shows the simulated output of the proposed comparator, sampling at 200Ms/s a 100MHz input switching between 128LSB (0.5V) and ±1/2LSB (±1.95mv). Because of the performance degradation expected with worst-speed device parameters, a maximum usable sampling speed of 160Ms/s was estimated. Random MOST and BJT mismatches were taken into account, according to the indications from the foundry. The proposed architecture can also be adapted to current mode, folding A/D converters [5]; in which case the first stage may be shared between several latches. The comparator is interfaced to CMOS logic by a low-kickback CMOS flip-flop. Fig.4 shows a photograph of the comparator cell, whose area is about $160x90\mu m^2$.

3 Test method and Results

Fast comparators are commonly tested [6, 7] by applying to an input a square waveform (Vs), with a frequency $f_{Vs} = f_{ck}/2$, and to the other input a D.C. voltage (Vc). In a differential converter, when the differential input voltage switches between 128LSB and +/-0.5LSB, the comparator has to discriminate the smallest voltage (with respect to its resolution) after being driven to the largest possible overdrive. This is a quite severe test of regeneration and recovery operations, and it is, therefore, commonly used also for simulations. Test-bench setup is difficult, because pulse generators do not provide ideal waveforms, small line mismatches causing ripples of several tens of millivolts, i.e. several LSBs. In previous works [6, 7] the output of the comparator was monitored with an oscilloscope, while sampling the above described signals. Fig.5 shows the result obtained at f_{ck}=120MHz, the maximum frequency allowed by the available oscilloscope. Notice the PECL compatible output levels, to which the internal CMOS signals are converted for easier interfacing. This test procedure, however, allows neither estimating Bit Error Rate (BER), nor an accurate measurement of the comparator's input offset voltage, because of the unavoidable ringing occurring in the input waveform.

A different test setup was therefore devised, where instead of a D.C. voltage, a square waveform antisymmetrical to Vs is used for Vc, in order to minimize the board-level disturbances. A counter is used for estimating, over a time interval corresponding to about 10^9 clock cycles, the mean frequency f_{out} of the up transitions at the comparator's output. Fig.6 shows that, for f_{ck}=160MHz, f_{out} varies between 0 and 80MHz as the minimum difference ΔV between Vs and Vc is varied by a few mV; the measured values (triangles) were interpolated by the $erfc$ function, predicted by the theory. The measured σ is 0.55 mV, which corresponds, at the edges of a transition region of 4mV (6mV) to a BER of 1.3 10^{-4} (2.4 10^{-8}, respectively). Notice, however, that external noise sources and an identified negative feedback effect, arising from board parasitics, make this transition region surely wider than the intrinsic one of the comparator, and this should be considered therefore a pessimistic estimate.

Due to the unavoidable ringing, the centre of the transition region does not correspond to the comparator's input offset. Offset was measured at several values of f_{ck}, using D.C. input voltages. As shown in fig.7, the measured offset voltage of all samples is always within ±2mV, and it is therefore compatible with 8bit resolution, on a 1V range, up to 160MHz of clock frequency.

References

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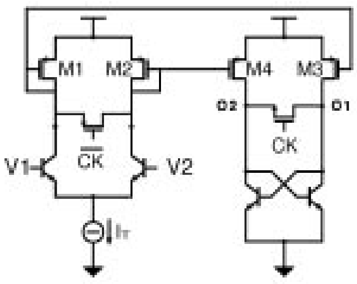

Fig.1: The Current Mirroring latched comparator.

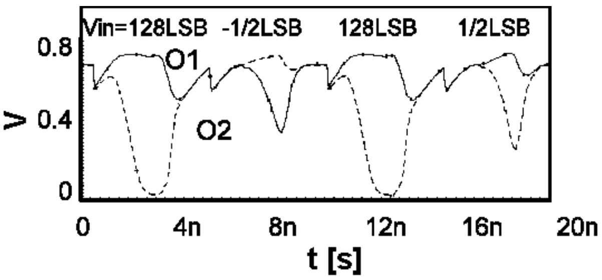

Fig.3: Simulated output waveform of the proposed comparator. The simulation was performed with an input waveform switching between 128LSB (0.5V) an ±1/2LSB (1.95mv) and taking into account the mismatches between MOSTs.

Table I: Specifications of the experimental comparator.

Technology	1.2µm BiCMOS
Comparator Cell Size	160 x 90 μm^2
Max. Sampling Freq.	160MHz
Max. Input Freq.	80MHz
Input Offset Voltage	2mV
Supply Voltage	3.3 ± 10%
Current Consumption at 160Ms/s: Comparator	80µA

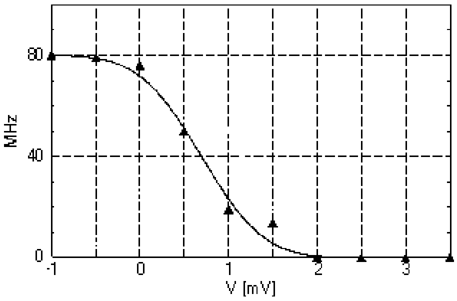

Fig.6: Mean frequency, measured at the output of a Current Mirroring comparator, as a function of the minimum differential input voltage *V*=Min(*Vs*-*Vc*). The test was performed at the maximum clock frequency specified for the comparator, i.e. 160MHz.

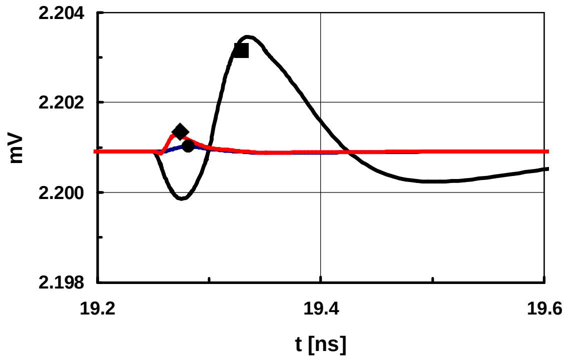

Fig.2: Kickback noise of the conventional comparator (■) and of the ***Current Mirroring*** comparator, with (●) and without (◆) emitter follower buffering. Source resistance: 200Ω.

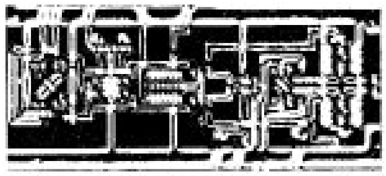

Fig. 4: Chip photograph.

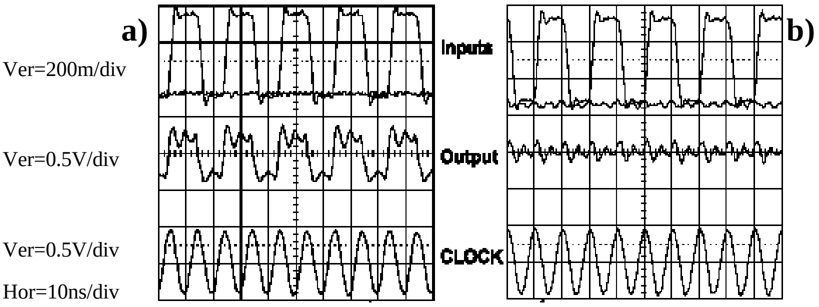

Fig.5: Oscilloscope's screen showing the input signals (*Vc* and *Vs*), the output signal (*Vout*) and the clock. Part a) and b) refer to a differential input voltage switching between 128LSB and -1/2LSB, 1/2LSB respectively.

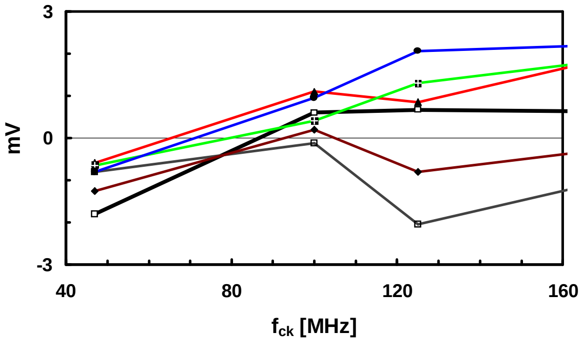

Fig.7: Input offset voltage of 6 samples, measured at several clock frequencies.