

A 10-bit 50MS/s 300mW A/D Converter using Reference Feed-Forward Architecture

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Abstract - This paper describes a 10-bit 50MS/s 300mW CMOS ADC employing time-interleaved, 4-stage pipelined configuration. To reduce power dissipation, Reference Feed-Forward architecture is introduced. In this architecture, resistive-load differential amplifiers (DifAMPs) are used between two pipeline stages instead of high-gain high-speed amplifiers. The gain matching of the reference voltage with the internal signal range is achieved by a reference generator (RefGEN) having the same characteristics as a DAC/subtractor (DA/subt) circuit. The offset voltages of the DifAMPs are cancelled by the offset cancellation technique. The front-end sample/hold (S/H) circuit is eliminated to reduce power dissipation. By introducing high-speed comparators based on source follower and latch circuit into the 1st-stage A/D subconverter (ADSC), analog bandwidth is not degraded.

1. Introduction

Low-power CMOS 10-bit ADCs which have a conversion rate of 30-50MS/s are required for high-definition video LSIs and digital demodulation LSIs. Although a 10-bit 50MS/s CMOS ADC has been reported [1], its power dissipation is as much as 900mW due to the front-end S/H and subtractors, which are constructed by high-gain high-speed amplifiers. On the other hand, low-power (85mW) 10-bit 40MS/s ADC has been reported [2]. However, its -3dB bandwidth is limited to 1/2 of the Nyquist frequency due to its averaged parallel sampling.

This paper describes a low-power 10-bit 50MS/s pipelined CMOS ADC without using the high-gain high-speed amplifiers. Furthermore, the front-end S/H is eliminated to reduce power dissipation by introducing a high-speed comparator based on source follower.

2. Reference Feed-Forward Architecture

In the conventional pipelined ADC, the reference voltage of each stage is applied from external terminals as a constant voltage. In order to obtain the gain matching of the internal signal range with the reference voltage, the high-gain high-speed amplifiers are used in forms of feedback circuits in the front-end S/H and the subtractors.

In this architecture shown in Fig.1, the resistive-load low-gain DifAMPs (Dif1a, Dif2a,...) are used instead of the high-gain high-speed amplifiers. The gain matching of reference voltage with the internal signal range is achieved by introducing the RefGEN having the same characteristics as the DA/subt circuit. The power dissipation of the DifAMP is very small (18mW) compared with high-gain high-speed amplifiers. Therefore, in this architecture, power

dissipation is reduced even though two DifAMPs are used in each stage. The required linearity for the DifAMP is seven-bit, and it is obtained by restricting the input range to +/-50mV. Furthermore, the offset voltages of the DifAMPs are cancelled in following ADSC and DAC/subt circuit as described in section 3.

3. Circuit Operation for Offset Cancellation

3.1 Subtractor in first stage Figure 2 shows an operation of the subtractor in the signal-side path. The subtractor operates in 2 phases (the sampling and the subtracting phases). In the sampling phase shown in Fig.2(a), the subtractor samples input signal V_{in} . Furthermore, the Dif1b simultaneously feeds its output offset voltage $V_{in2_{off}}$ to the second stage because the same bias voltage V_b is applied to both of its input terminals. In the subtracting phase shown in Fig.2(b), output voltage of the DAC V_{da} is subtracted from sampled input voltage, and a residue $V_{in2}(=V_{in2_0}+V_{in2_{off}})$ is fed to the second stage, where V_{in2_0} is the residue when the offset voltage is zero. The phase of the subtractor in the reference path is the opposite of this subtractor. Therefore, the reference voltage $V_{r2}(=V_{r2_0}+V_{r2_{off}})$ and its offset voltage $V_{r2_{off}}$ are fed by Dif1a alternately. Each offset voltage ($V_{in2_{off}}$ and $V_{r2_{off}}$) is cancelled independently by the comparator and the DA/subt as shown in Fig.3. The timing diagram of these operations is shown in Fig. 4.

3.2 Comparator The comparators shown in Fig.3 have 2-pair of coupling capacitors (C1~C4) for differential-voltage comparison. This comparators operate in two-phases shown in Fig.4. The reference voltage V_{r2} and the offset voltage $V_{r2_{off}}$ fed by Dif1a are divided by a resistor-ladder to generate ladder-tap voltages $V_{r2(n)}(=V_{r2(n)_0}+V_{r2(n)_{off}}$, $n=1, 2, ..$) and their offset voltages $V_{r2_{off}(n)}$, respectively, where $V_{r2(n)_0}$ is the n-th ladder-tap voltage when the offset voltage is zero. In the auto-zeroing period of the comparator, the ladder-tap voltage $V_{r2(n)}$ and the offset voltage $V_{in2_{off}}$ of Dif1b are sampled on capacitors C1, C2 and C3, C4, respectively. In the comparing period, the offset voltage $V_{r2(n)_{off}}$ of the ladder-tap and the residual signal $V_{in2}(=V_{in2_0}+V_{in2_{off}})$ are applied to the capacitors C1, C2 and C3, C4, respectively. Therefore, the output voltage of the comparator is obtained as follows.

$$\begin{aligned} V_{out(n)} &= -(A/2) \{ (V_{in2} - V_{in2_{off}}) - (V_{r2(n)} - V_{r2(n)_{off}}) \} + V_{bc} \\ &= -(A/2) \{ V_{in2_0} - V_{r2(n)_0} \} + V_{bc} \end{aligned} \quad (1)$$

where V_{bc} and A are the auto-zeroed bias voltage and the total gain of amplifiers in the comparator, respectively. Therefore, the differential-voltage comparison without the offset voltages of Dif1a and Dif1b is achieved.

3.3 DA/subt circuit In this ADC, resistor-ladder of the ADSC is used as the internal DAC with transmission gates (TGs). Each ladder-tap offset voltage $V_{da(n)_{off}}$ fed by the Dif1a is sampled on each capacitor C during the sampling phase of the DA/subt circuit. In the subtracting phase, the TGs selected by the conversion result from the encoder are still turned on, the others are turned off. Therefore, the offset voltage of the selected ladder-tap is cancelled. The offset voltage of Dif1b in the signal path is cancelled in a way similar to that of the comparator. Therefore, the output voltage of the DA/subt circuit is obtained by

$$\begin{aligned} V_{dif(n)} &= -(Adif/2) \{ (V_{in2} - V_{in2_{off}}) - (V_{da(n)} - V_{da(n)_{off}}) \} + V_b \\ &= -(Adif/2) \{ V_{in2_0} - V_{da(n)_0} \} + V_b \end{aligned} \quad (2)$$

where $V_{da}(n)$, $V_{da}(n)_{off}$ and $V_{da}(n)_o$ are the selected-tap voltage, its offset voltage and its tap-voltage when the offset voltage is zero, respectively, V_b is a auto-zeroed bias voltage and $Adif$ is the gain of the $Dif2b$. Therefore, the subtraction without the offset voltages of $Dif1a$ and $Dif1b$ is achieved in this DA/subt circuit.

The reference voltage for the next stage is generated by the RefGEN connecting to the specific ladder-taps “ a, b” shown in Fig.3. The same technique is also used in the second and the third stages to cancel the offset voltages.

4. Elimination of front-end S/H

By using the digital error correction, the skew of the sampling clock between the first ADSC and the first subtractor is relaxed. The target delay is 200psec in case of the 4-bit accuracy, 50MHz input frequency and error correction of 1b-overlap configuration. Therefore, the input S/H is eliminated shown in Fig.5. The high-speed comparators constructed by the source followers and latch circuit, shown in Fig.6, are used in this stage. Because the comparator has little propagation delay (simulated result of 100psec), the 1st-stage ADSC can sample the input voltage within the target delay.

5. Experimental Results

The ADC is fabricated in $0.5\mu m$ double polysilicon, double metal CMOS technology. Figure 7 shows a photomicrograph of the ADC and the active area is $3.2mm \times 3.4mm$. Figure 8 shows reconstructed waveforms at the conversion rate of 50MS/s. Figure 9 shows differential non-linearity. The high-speed conversion has been achieved with low-power dissipation of 300mW ($V_{dd}=3.0V$). The characteristics of the ADC are summarized in Table 1.

References

- [1] M.Yotsuyanagi, T.Etoh and K.Hirata, "A 10Bit 50Msample/sec Pipelined CMOS A/D Converter with S/H", CICC'92, pp.16.7.1-16.7.4, 1992
- [2] K.Nakamura, M.Hotta, R.Carley and D.Allstot, "A 85-mW,10-bit 40-Ms/s ADC with Decimated Parallel Architecture", CICC'94, pp.23.1.1-23.1.4, 1994

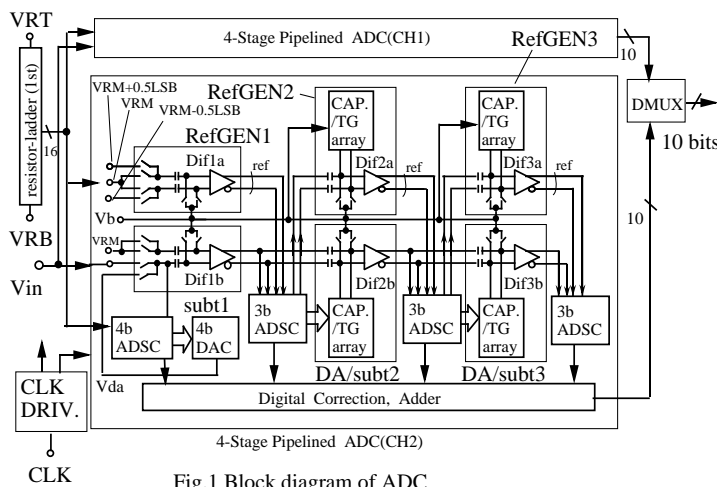


Fig.1 Block diagram of ADC (4-stage pipeline, 2-interleave)

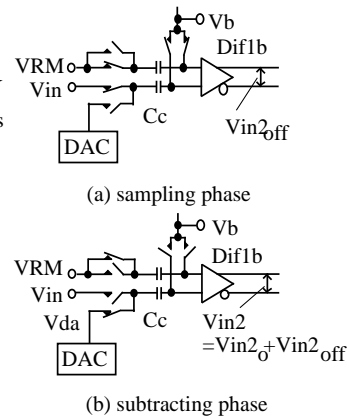


Fig.2 Operation of 1st subtractor (subt1)

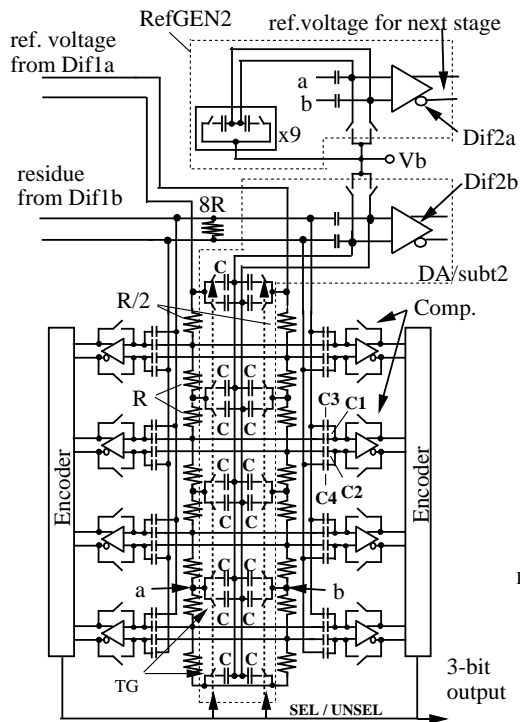


Fig.3 Simplified Block Diagram of 2nd stage

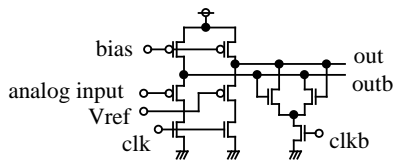


Fig.6 Comparator of 1st stage

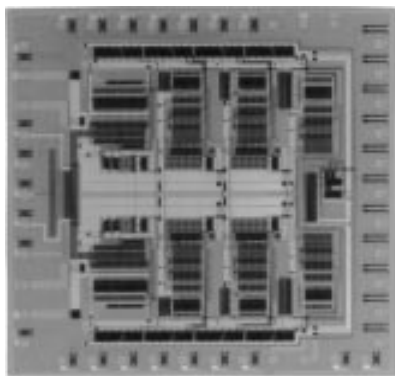


Fig.7 Photomicrograph of ADC

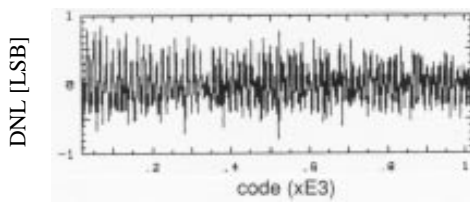


Fig.9 Differential Non-Linearity (static)

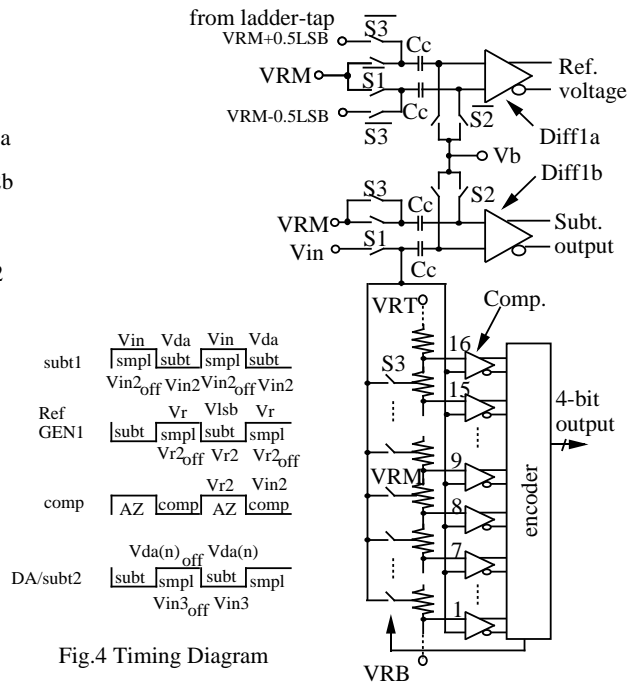


Fig.5 Block Diagram of 1st stage ADSC

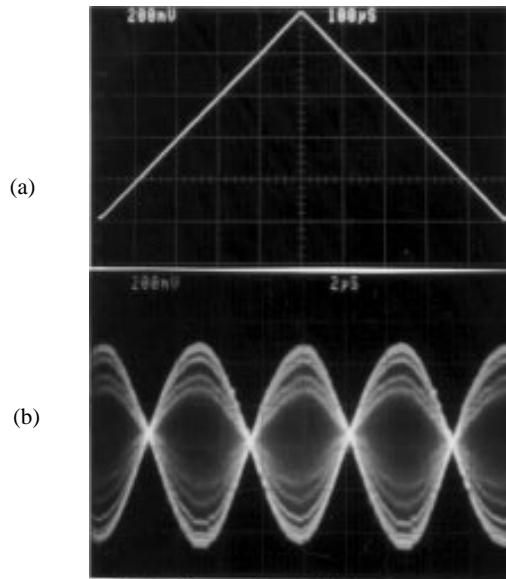


Fig.8 Reconstructed Waveform
fsc=50MS/s, (a)fin=1kHz, (b)fin=24.9MHz

Table 1 Chip characteristics

Resolution	; 10-bit
Conversion Rate	; 50MS/s
Power Consumption	; 300mW(Vdd=3.0V)
Chip size(active area)	; 3.2mm x 3.4mm
Linearity (INL/DNL)	; ± 2 LSB / ±1LSB
Distortion (2-5th)	; -58.4 dB (fin=48.8kHz, fsc=50MS/s)
Process Technology	; 0.5µmCMOS(2poly,2Al)