

14 bit $\Sigma\Delta$ Modulator with Multi Bit Feedback

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Abstract

This paper presents a first order $\Sigma\Delta$ Analog to Digital Converter for current measurement in motor controls. The converter consists of a time continuous differential integrator at the input with external capacitors and a four bit pulsewidth modulator in the feedback branch. Highly symmetrically switching inverters are used to couple the differential feedback signal back to the input of the converter. The circuit is implemented in a 1.2 μm CMOS N-Well Process and requires 2 mm^2 for the analog and digital parts of the modulator. Power consumption is about 20 mW. Measurements show the feasibility of this structure for a resolution of 14 bit.

Introduction

The actual current value measurement, the calculation of control parameters and the activation of the motor driver for digital motor controls are done on a time slot base as shown in Fig. 1. For most control algorithms it is not the actual value of the AC-motor current at time t_1 which is important, but the mean value during period T_1 . Using the integrating analog to digital conversion method of a $\Sigma\Delta$ modulator, averaging and digitizing are achieved at the same time. Digitizing errors caused by switching and power noise on the signal are strongly reduced by the averaging method. A low offset and gain error is achieved by a simple differential first order modulator structure. Increased conversion speed is reached by a four bit digital to analog conversion in the feed back structure of the modulator. Changing the time slot period of modern control systems dynamically is supported by the possibility of the $\Sigma\Delta$ ADC to trade off resolution and conversion speed. The next section describes the architecture of the modulator and different aspects of implementation and layout. Finally, measured results of an integrated version of the modulator are shown.

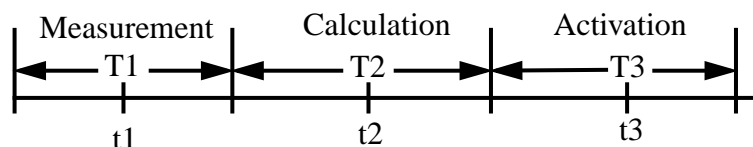


Fig. 1 : Time Base in Digital Motor Control Systems

Architecture

The modulator structure is depicted in Fig. 2. The well-known first order $\Sigma\Delta$ modulator configuration is recognizable by the integrator, the following low resolution ADC structure and the DAC in the feedback path. In this particular case, the ADC in the forward path consists of a parallel structure with a single bit decider and a window comparator followed by a digital integrator.

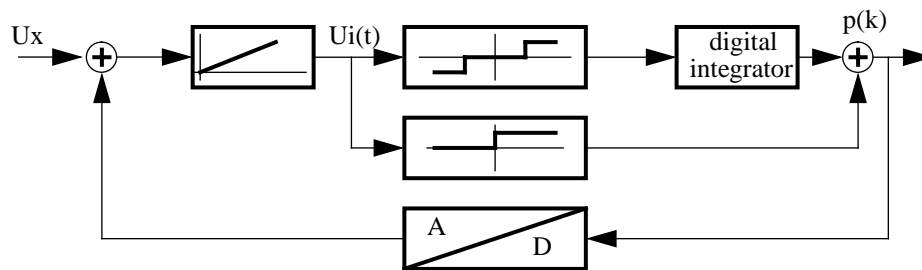


Fig. 2 : Structure Diagram of the $\Sigma\Delta$ Modulator

In static operation, the digital integrator contains a value that represents a coarse quantification value of the analog input signal. The remaining difference between the actual analog input voltage and the corresponding coarse quantification voltage level is converted like in a single bit $\Sigma\Delta$ Modulator using the single bit decider only. Thus, the feedback signal $p(k)$, which is the sum of the digital integrator output and the single bit comparator, changes between the two digital values closest to the analog input.

The output of the analog integrator is observed by a window comparator for an upper and a lower limit. If the input signal changes too much, the difference between the analog input value and the corresponding feedback value represented by the content of the digital integrator will cause the integrator output to leave its limits. This is detected by the window comparator. The digital integrator changes its value until another stable operating point is reached. The accuracy of the feedback DAC, which has a resolution of 4 bit in our application, determines the linearity of the whole $\Sigma\Delta$ ADC. One possible way to achieve a high accuracy of more than 12 bits is to use pulsewidth modulation signals. Since the analog integrator output is sampled by the $\Sigma\Delta$ clock, it is sufficient to reproduce the voltage time area of the feedback signal $1/f_s$. For a fast optimized symmetrical on- and off-switching of the pulse drivers and for a stable reference, voltage nonlinearity is mostly caused by the pulsewidth timing which is derived from the quartz based system clock. The linearity of the system is further improved by a differential feedback of two PWM signals which produce bipolar voltage time areas from one reference voltage. The sampling time of the digital integrator is derived from the system clock by a factor of 20 which is $1\ \mu\text{s}$ for a 20 MHz clock in our system. The one to fifteen step pulsewidth signal, shown in Fig. 3, is centered in the sampling period of $1\ \mu\text{s}$, giving the analog integrator a settling time of at least three system cycles. For higher resolution the four bit MSB at the output $p(k)$ of the modulator are summed up and averaged by dividing the sum of $p(k)$ by the number of added values in a chosen acquisition period.

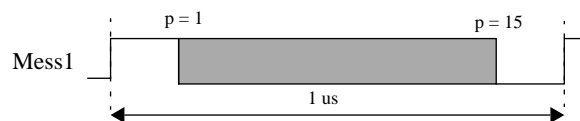


Fig. 3 : Pulsewidth Modulated Feed Back Signal

Circuit Design

A modulator blockdiagram is given in Fig. 4. The integrator consists of an operational amplifier with integrated input resistors R_f and two external capacitors C_{ex} . The OP-Amp has a p-mos differential input stage and a class AB output structure. The cell which is shown in Fig. 5 is optimized for a high and equal slewrate in both switching directions.

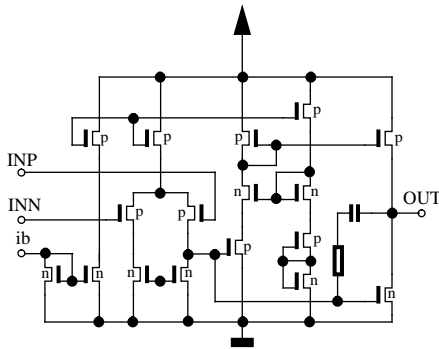


Fig. 5 : Operational Amplifier

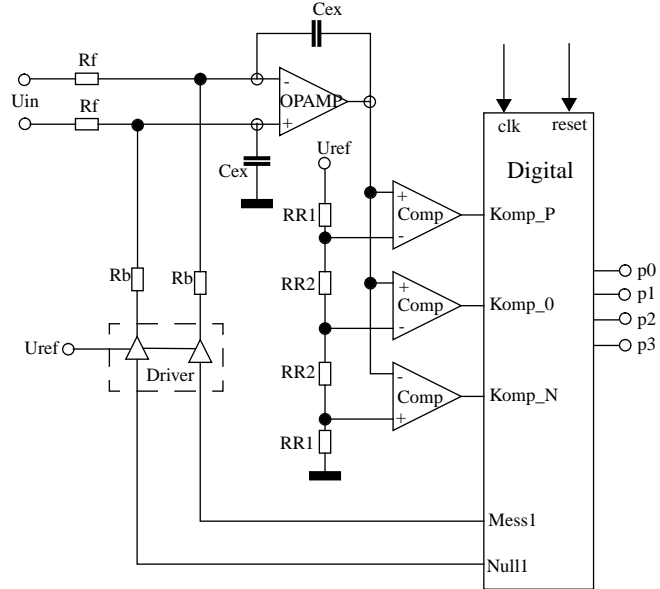


Fig. 4 : Schematic Block Diagram of the Modulator

The internal modulator clock frequency is derived from the system clock by a factor of 20. Fig. 6 shows the simulated output signal of the integrator for a modulator frequency of 1 MHz. The integration error is low if the overshots at the upper and lower turning points are symmetrical. Simulation analysis showed that the resulting error caused by the integrator is lower than 1 LSB for 14 bit resolution. The comparator output signal Komp_0 which is sampled by the modulator clock toggles the digital feed back value by one step. The integrator output voltage range is observed by the comparators Komp_P and Komp_N, adjusting the coarse quantification step by increasing or decreasing the digital integrator. The value of the digital integrator is represented by a pulswidth voltage signal generated by low ohmic drivers which are optimized for fast switching in both directions. The power rail of the drivers is connected to the voltage reference. Mismatching of the resistors in the forward and backward path will cause offset and gain errors only. With a precise reference, the linearity of the D/A-conversion depends mostly on the accuracy of the pulswidth timing. That is derived from the quartz based system clock. Extensive simulations with HSPICE and ELDO showed that the structure is good for a linearity of more than 14 bits.

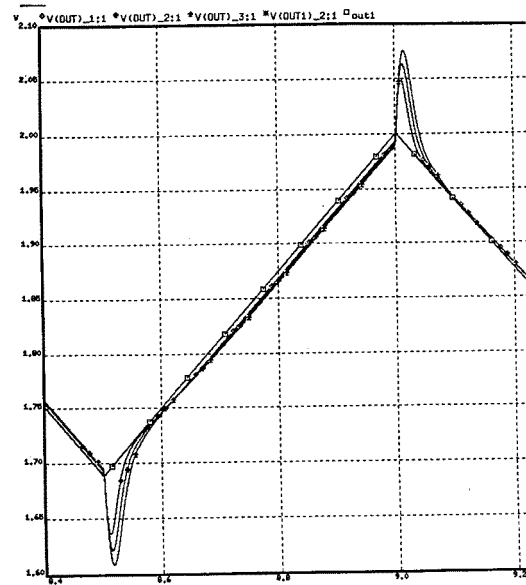


Fig. 6 : Integrator Output Signal

Layout

Two identical $\Sigma\Delta$ converters have been implemented on a chip. A photograph of the device is shown in Fig. 7. The analog part and the digital part of one converter without pads occupy an area of 1.0 mm^2 each. The remaining digital logic implements a serial interface for the parallel 4 bits. On the device, there are additionally integrated a power on reset structure, a clock generator and a buffered voltage reference cell.

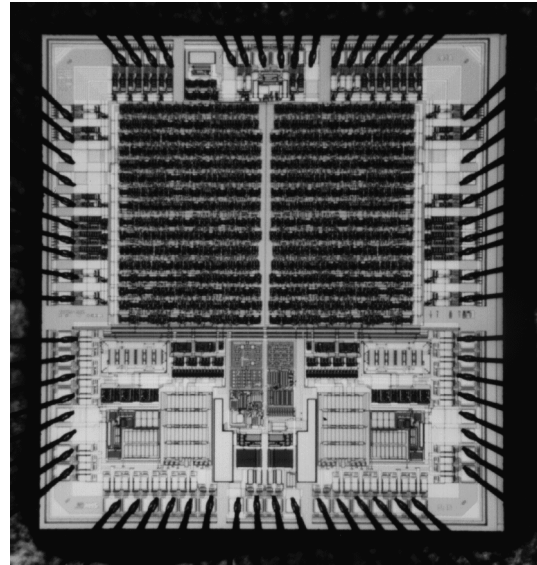


Fig. 7 : Chip Microphotograph

Measurements

The measurements were done with a dedicated test setup implemented to characterize ADCs. The number of least significant error bits, including offset and gain errors over an ambient temperature range of -40 deg C to 120 deg C are shown in Fig. 8. Differential nonlinearity and fitted integral nonlinearity, shown in Fig 9, are lower than $\pm 1 \text{ LSB}$ for 13 bits resolution.

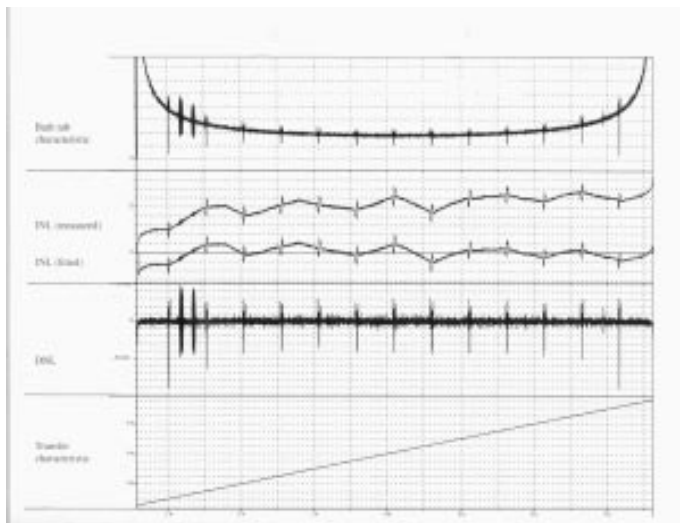


Fig. 9 : Measurement of INL and DNL

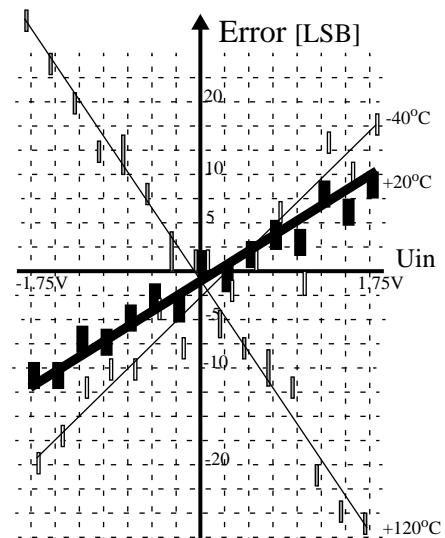


Fig. 8 : Temperature Characteristic

Summary

An integrated multi bit feedback $\Sigma\Delta$ modulator has been presented which is used for current measurement in motor control systems. High linearity is achieved by having the accuracy of the feedback structure depending mostly on the timing of the quartz based clock. Further implementations using switched capacitor technique will eliminate the necessity of external integration capacitors.

References

/1/ F.Maloberti , G.Torelli, C.Vacchi, „Multi bit oversampled DAC with dynamic matching of current sources“, Proceedings of Int. Conference on ADC and DAC, 1991, Swansea, UK