

A CMOS Optical Sensor System Performing Image Sampling on a Hexagonal Grid

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Abstract

An integrated CMOS image acquisition system suitable for retinal information processing in bionic vision systems or product inspection has been developed and tested. It supports the readout of arbitrarily user-defined subregions. The test chip incorporates 32x32 random addressable active sensor cells arranged on a hexagonal grid and on-chip control and readout electronics. It has been designed and fabricated in a standard 1.5 μm n-well CMOS process. The size of a single sensor cell is 38.8 μm x 33.6 μm and the total chip area is 7 mm². The sensor cells show a logarithmic response in illumination and are capable of detecting illumination variations with frequencies well above 1 MHz.

1. Introduction

The function of retinal image acquisition and processing as part of biologically inspired technical vision systems can be described by the convolution of an input image with so called receptive field functions. Due to the radial symmetry of these functions a sampling scheme is desired that ideally supports sampling on concentric circles centered around an arbitrary position on the sampling grid. The fact that among all periodic sampling schemes hexagonal sampling provides the highest degree of circular symmetry led us to implement this scheme in our system. In addition, for signals that are bandlimited over a circular region of the Fourier plane, hexagonal sampling is also optimal in the sense that exact reconstruction of the waveform requires 13.4% fewer samples than the alternative rectangular sampling scheme [Mer79]. Physiological studies concerning the assembly of receptor cells in the foveal region of the human retina have further shown that parts of the cone mosaic form a hexagonal structure [Per85].

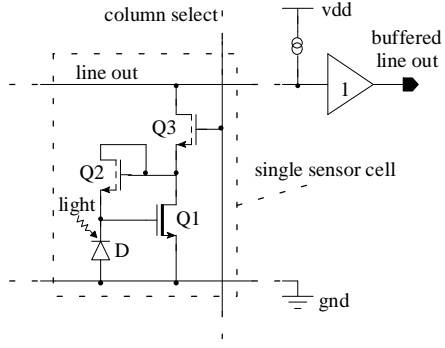


Figure 1: Schematic of the sensor cell

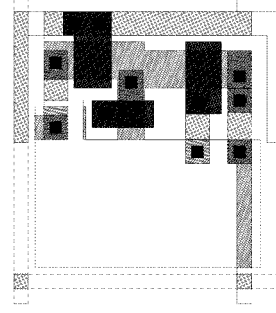


Figure 2: Layout of the sensor cell

In addition to the proper choice of the sampling grid the major requirements for our image acquisition system have been random access to each sensor cell, low fixed pattern noise, high speed readout, and a logarithmic response of the sensor output to illumination. Implementing a logarithmic response characteristic offers great advantages because on the one hand it helps realization of the high dynamic range for illumination in natural environments (about 5-6 decades) and, on the other hand, extraction of the relevant information from the image becomes easier since the difference of two pixel outputs only depends on the contrast ratio and not on the level of the absolute illumination.

2. Sensor Cell Design

Schematic and layout of a single sensor cell are shown in Figs. 1 and 2, respectively. Aiming at a small sensor pitch we kept the sensor circuit as simple as possible and avoided PMOS transistors requiring n-wells. The sensor is realized using a photodiode D formed by a n+ diffusion in the p-substrate. In usual illumination conditions the generated photocurrent is in the order of pA to nA so that feedback transistor Q2 always operates in weak inversion and, therefore, exhibits a logarithmic dependence of its drain-source voltage V_{DS} on the photocurrent I_D . According to [Vit94] the drain current in weak inversion can be approximated by

$$I_D = I_s \exp\left(\frac{V_G - V_{T0}}{nU_T}\right) \left(\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right) \right)$$

with I_s denoting the specific current of the transistor that is in the order of $100 \text{ nA} \cdot \frac{W}{L}$. For $V_D - V_S \gg U_T$ the gate potential is then given by:

$$V_G = V_{T0} + nV_S + nU_T \ln \frac{I_D}{I_s} = V_{T0} + nV_S + nU_T \ln 10 \log \frac{I_D}{I_s}.$$

In a logarithmic representation the slope of the above function is about $100 \text{ mV} / \text{decade}$. Transistors Q1 (native NMOS, $V_T = -0.2 \text{ V}$) and Q2 keep the cathode of the photodiode at approximately constant potential. The voltage across the diode is controlled by the bias current injected from the output line. This enables a photodiode short circuit operation and, therefore, yields a short response time since no charge has to be transferred onto or from the diode

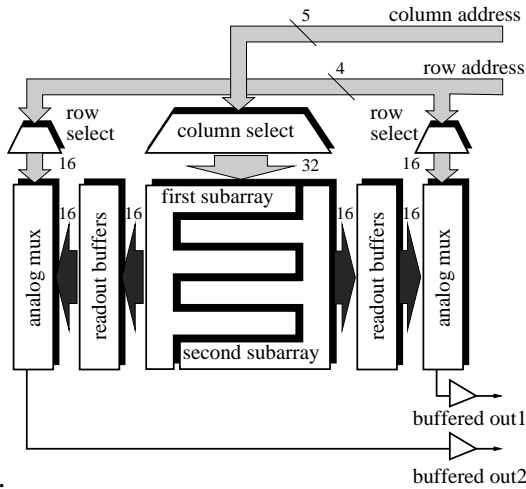


Figure 3: Block diagram of the sensor chip

Figure 4: Chip microphotograph

capacitance when the illumination changes. Transistor Q3 enables the column select and conducts the bias current to the output line passing the sensor cell.

3. Readout Electronics

Fig. 3 shows a block diagram of the testchip consisting of the hexagonal sensor array and dedicated readout electronics. To avoid using a hexagonal addressing scheme, we have logically divided the hexagonal sampling grid into two comb-like intermeshed rectangular subarrays consisting of 32 columns and 16 rows each. An advantage of this concept is the possibility of addressing and reading out both subarrays of sensor cells in parallel. Random access to each sensor cell is provided without column or row serial scan. In our preliminary test system both subarrays are accessed using identical row- and column addresses, so that two diagonally adjacent sensor cells can be read out in parallel.

4. Measurements

Fig. 5 shows the output voltage of a single sensor cell vs. the normalized light intensity. It can be seen that the desired logarithmic response characteristic is achieved for more than 6 orders of magnitude of incoming light intensity. The measurement was carried out by attenuating a laser beam with neutral density filters of variable light transmittance.

Fig. 6 shows the normalized signal amplitude at the sensor output vs. the light intensity modulation frequency. An attenuation of the sensor output signal of more than 3dB is given for frequencies above approximately 300 kHz. The characteristic was determined by measuring the output signal amplitude while modulating the light intensity of a laser beam.

With regard to sensor cell mismatch we found that between the outputs of separate sensor cells there exists a considerable voltage offset of up to 60 mV or 10% of the dynamic range of a single sensor cell. The slope of the logarithmic sensor output characteristic however shows far better matching properties. The relative variation of the output signal amplitude between

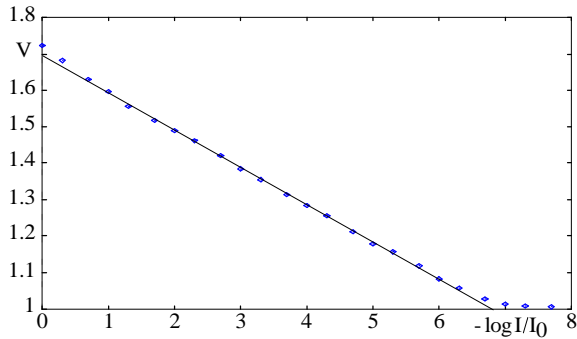


Figure 5: Sensor output vs. normalized light intensity

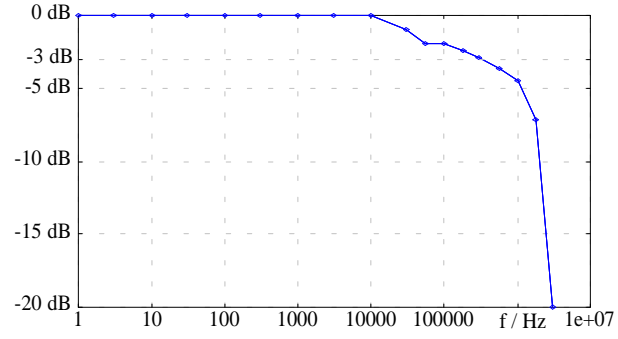


Figure 6: Normalized sensor output vs. light modulation frequency

separate sensor cells is in the order of only 1%. Hence simple offset compensation may lead to satisfactory matching properties as they are required for image acquisition tasks.

5. Conclusion

In this paper a new CMOS image acquisition system consisting of 32x32 random addressable active sensor cells arranged on a hexagonal sampling grid together with on-chip control and readout electronics has been presented. The system supports the readout of arbitrarily user-defined subregions. As measurements have proven, the single sensor cells show a logarithmic output characteristic for more than 6 orders of magnitude of incoming light intensity. Due to short-circuit operation of the photodiode the sensors are capable of detecting intensity modulation frequencies well above 1 MHz. Since the slope of the logarithmic sensor output characteristic shows very good matching properties the problem of fixed pattern noise may be solved by implementing an offset compensation for each sensor cell.

Number of pixels	32x32	Sensor 3dB-frequency	300kHz
Pixel pitch	38.8 μ m x 33.6 μ m	Sensor dynamic range	10 ⁶
Chip area	7mm ² (1.5 μ m CMOS)	Sensor offset mismatch	10%
Power dissipation	5mW (5V)	Sensor gain mismatch	1%

Table 1: Electrical and optical parameters of the sensor chip

References

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